

Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality

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We have studied the effect of hydrogen annealing on the surface roughness of germanium (Ge) layers grown by chemical vapor deposition on silicon using atomic force microscopy and cross-sectional high resolution scanning electron microscopy (HR-SEM). Our results indicate a strong reduction of roughness that approaches 90% at 825 °C. The smoother Ge surface allowed for the fabrication of metal-oxide-semiconductor capacitors using germanium oxynitride (GeO_xN_y) as the gate dielectric. Electrical quality was studied using high frequency capacitance–voltage characteristic of epi-Ge showing negligible hysteresis. We discuss the results in terms of Ge–H cluster formation, which lowers the diffusion barrier, allowing for higher diffusivity and surface mobility. The temperature dependence shows tapering off for temperatures exceeding 800 °C, indicating a barrier reduction of ~ 92 meV. © 2004 American Institute of Physics.
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Recently, germanium has emerged as a viable candidate to augment silicon for CMOS and optoelectronic applications.^{1,2} First, germanium has superior transport properties since its electron and hole mobility are two- and fourfold larger than those in Si, respectively. Second, germanium has a smaller absorption coefficient, which makes it attractive for integration of monolithic photodetectors for the ultimate use in optical interconnects. In addition, successful growth of Ge on Si allows subsequent growth of optically active material such as GaAs since Ge and GaAs have the same lattice constant,³ but for Ge to become mainstream, heterogeneous integration of crystalline Ge layers on Si must be achieved. This is not straightforward because of the large lattice mismatch (4%) between Ge and Si, which limits the quality of the heteroepitaxial growth. First, above the critical thickness, the layer will have many misfit dislocations making it unusable for any practical applications. The growth of Ge on Si results in island morphology, or the so-called “Stranski–Krastanow” (S-K) growth. Such growth is associated with large surface roughness, causing difficulties in process integration, such as bonding for Ge-on-insulator (GOI). This can lead to degradation in device properties.

It has been shown that hydrogen annealing enhances surface diffusivity of silicon, which results in an enhancement of the surface mobility. For instance, using after etched bonded SOI wafers, Sato and Yonehara demonstrated that an hour of hydrogen annealing at 1150 °C significantly reduced roughness of SOI layers to near bulk values.⁴ Moreover, there is some evidence to the effect of hydrogen on the direct path diffusion barrier of metals. For instance, the diffusion barrier of Pt–H molecule is reduced by 90 meV compared to the barrier of Pt diffusion.⁵

In this letter, we report the results of a study on the effect of hydrogen annealing on the surface roughness of Ge films

grown by chemical vapor deposition (CVD) on silicon using atomic force microscopy (AFM) and cross sectional high resolution scanning electron microscopy (HR-SEM). A roughly 90% reduction of surface roughness is achieved at 825 °C, while the temperature dependence exhibits a tapering off effect for temperatures exceeding 800 °C. The results are explained in terms of Ge–H cluster formation, which lowers the diffusion barrier, ~ 92 meV at 800 °C, allowing for higher diffusivity and surface mobility. In addition to surface roughness measurements, smoother surfaces allowed for the fabrication epi-Ge metal-oxide-semiconductor (MOS) capacitors using germanium oxynitride (GeO_xN_y) as the gate dielectric. Electrical quality of the layers was studied by high frequency capacitance–voltage (C – V) characteristics.

We grew by CVD 200 nm of epitaxial germanium layers on standard bulk silicon wafers with resistivity 1–5 Ω cm. The wafers were dipped in dilute 50:1 H_2O :HF (hydrofluoric acid) for 30 s and immediately loaded in the ASMTM epitaxial reactor. A hydrogen bake at 950 °C was carried out to insure no native oxide remained on the surface. The epitaxial Ge was grown at 400 °C at reduced pressure of 10 Torr. Following the previous work,⁴ five different hydrogen anneals were carried out for 1 h immediately following the epitaxial growth (600, 700, 725, 763, and 825 °C), at a pressure of 80 Torr, and one wafer was left unannealed for comparison. In addition, one sample was annealed in nitrogen to show the effect of hydrogen more clearly. We studied the surface roughness by using a 10 μm \times 10 μm AFM scan and by using cross section high resolution scanning electron microscopy (HR-SEM).

Figures 1(a) and 1(b) are a tilted HRSEM cross section of the unannealed sample along with the 825 °C annealed sample, showing a reduction in surface roughness. Clearly visible on the unannealed surface (a) are large Ge islands with cross section of ~ 200 nm as expected from the S-K growth model due to lattice mismatch ($R_{\text{rms}} \sim 25$ nm). However, in the annealed sample (b), the islands have flattened to

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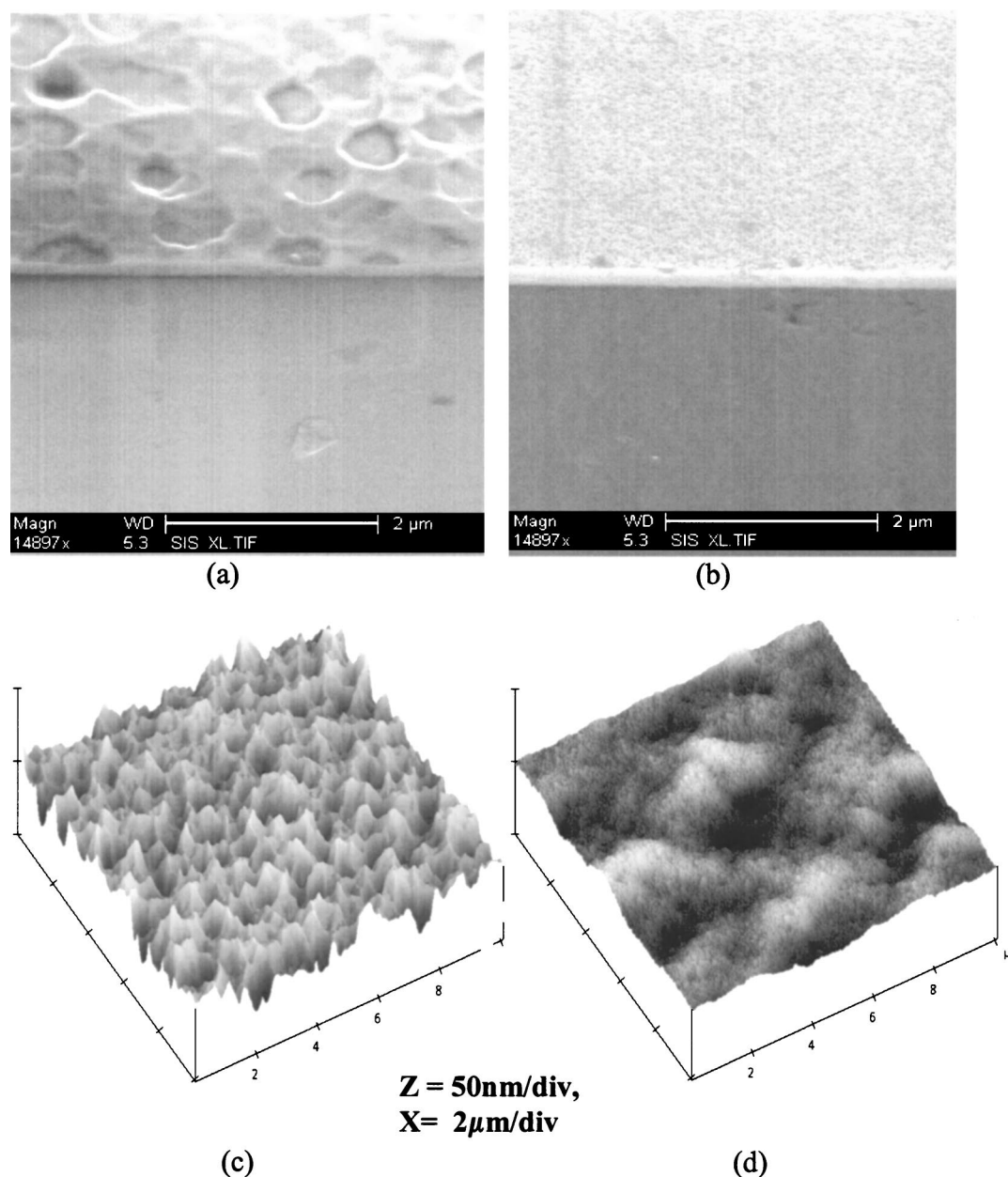


FIG. 1. Top: Cross section high resolution-SEM image (45° cut) (a) no hydrogen anneal; (b) 825 °C; Bottom: Topographical AFM image (10 $\mu\text{m} \times 10 \mu\text{m}$) of epi-Ge layer; (c) no hydrogen anneal (d) 825 °C

the point where the islands no longer exist or appear as tiny droplets ($R_{\text{rms}} \sim 3 \text{ nm}$). This flattening effect, we believe, is a result of increased surface mobility. This effect can also be seen in the topographical AFM images of the samples shown in Figs. 1(c) and 1(d). In addition, direct plan-view transmission electron microscope images confirmed the epi-Ge layer is crystalline but has crystal defects due to a 4% lattice mismatch. The sample annealed in nitrogen at 825 °C exhibited no reduction in surface roughness.

Figure 2 (left y axis) shows absolute rms roughness (R_{rms}) versus anneal temperature for the five different anneals. As seen in the graph, surface roughness reduction is clearly seen with an 88% reduction at 825 °C. The R_{rms} at 825 °C was measured from AFM to be 2.947 nm compared to 24.964 nm to the unannealed case. The temperature dependence of the R_{rms} reduction is shown in Fig. 2 (right y axis) which plots the change of R_{rms} vs temperature, where change was defined as the difference of R_{rms} at annealing

temperature and R_{rms} of the unannealed case. The temperature dependence of the R_{rms} yields a tapering off effect where a large reduction exists in raising the hydrogen bake temperature from 600 to 700 °C, while a much smaller drop occurs in a further temperature increase from 700 to 800 °C. The change of R_{rms} shows a peak at around 800 °C where further increasing the temperature no longer increases the reduction of the R_{rms} but rather the reduction remains constant. We note in the case of silicon one needs to anneal at 1150 °C to reduce the surface roughness to near bulk level.⁴ Thus it is interesting to note that the ratio of optimal annealing temperatures of Si and Ge turns out close to the ratio of their melting points. The surface roughness reduction can be explained in terms of the Ge diffusion barrier as compared to the Ge-H cluster. Inferred from the Si (Ref. 4) and Pt (Ref. 5) cases, the effect of attaching H to Ge reduces the diffusion barrier and increases the surface mobility by increasing the local density of states (LDOS) at the

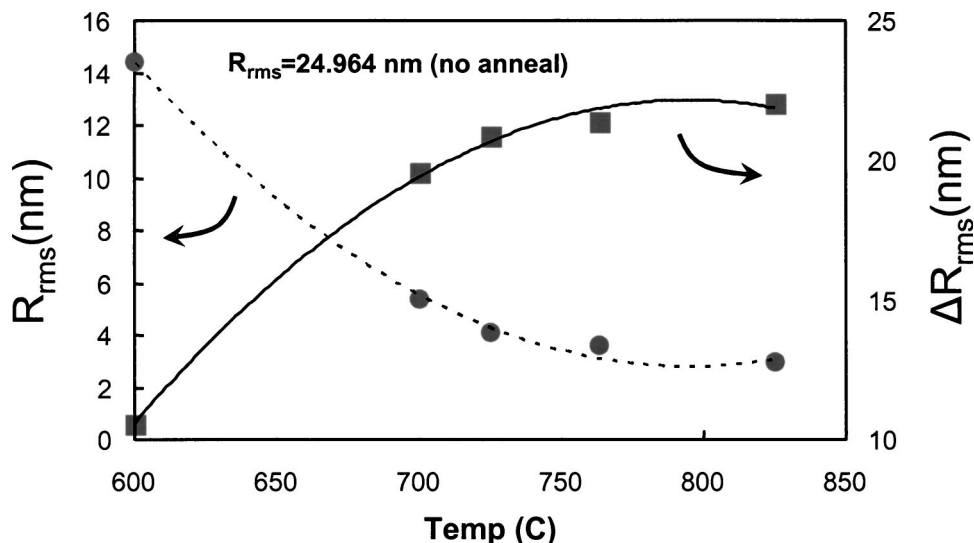


FIG. 2. (Left axis data) rms of epi-Ge layers as a function of hydrogen annealing temp for 1 h measured by AFM ($10 \mu\text{m} \times 10 \mu\text{m}$); (right axis solid) change in rms [rms (no anneal)-rms (anneal)] vs Temp.

Fermi level.⁵ However, there appears to be an upper limit to the amount of diffusion barrier reduction. We can estimate diffusion barrier height which is proportional to $\sim kT$ from basic diffusion kinetics. In the case of Ge it occurs around 800°C which corresponds to $\sim 92 \text{ meV}$ reduction of barrier height. The results indicate that Ge and Si (Ref. 4) behave similarly when annealed in hydrogen.

The smoother Ge surface enables us to evaluate the electrical quality of the epi-Ge layer. MOS capacitors using GeO_xN_y as the gate dielectric with tungsten (W) gate electrode were fabricated. The epi-Ge layer was *in situ* doped *n*-type during the deposition followed by cyclic rinsing between 50:1 $\text{H}_2\text{O}:\text{HF}$ (hydrofluoric acid) solution and DI water.⁶ GeO_xN_y was grown directly on the 825°C annealed epi-Ge substrate in a rapid thermal processing (RTP) system using ammonia and 500 \AA of W electrode was deposited by the room temperature *e*-beam evaporation through a shadow mask. We examined the electrical quality of both the epi-Ge substrate together with the $\text{GeO}_x\text{N}_y/\text{epi-Ge}$ interface using $C-V$ measurements. We deduced the $C-V$ hysteresis of these MOS capacitors, which is an indicator of the level

of interface states (through interface charge trapping) that can eventually degrade the MOSFET mobility. Figure 3 shows the bidirectional high frequency $C-V$ characteristics (100 kHz and 1 MHz) showing negligible hysteresis. From the 100 kHz sweep, however, we observed two kinks near inversion that suggests the presence of a finite amount of interface states. They were originated either from the $\text{GeO}_x\text{N}_y/\text{epi-Ge}$ interface or the epi-Ge layer. Further improvements of both the interface and epi-Ge layer are certainly required to perfect this material system for future Ge MOS device applications.

In conclusion, we have demonstrated surface roughness reduction approaching 90% of epitaxial germanium on silicon by hydrogen annealing after epitaxial growth. We found by studying the temperature dependence, the R_{rms} reduction becomes independent of temperature: the roughness reduction leveled off and reached a peak at around 800°C . We believe Ge-H clusters have a smaller barrier height as compared to Ge diffusion thus increasing the surface mobility. The maximum barrier height reduction in the Ge-H may be set at $\sim 92 \text{ meV}$. In addition we have demonstrated epi-Ge based MOS capacitors with low hysteresis $C-V$ characteristics on the after annealed layers. This hydrogen annealing technology may lead to subsequent bonding of Ge to Si/SiO₂ needed for the fabrication of germanium-on-insulator (GOI) substrates using epitaxial Ge.

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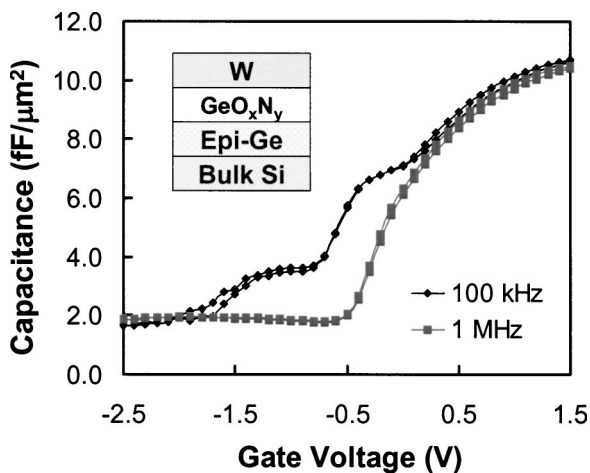


FIG. 3. Bidirectional $C-V$ characteristics of epi-Ge MOS capacitor structure using GeO_xN_y gate dielectric and W gate electrode: 100 kHz and 1 MHz.

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