Ultrathin High-κ Gate Dielectric Technology for Germanium MOS Applications

Chi On Chui, Shriram Ramanathan[1], Baylor B. Triplett[1], Paul C. McIntyre[1], and Krishna C. Saraswat

Department of Electrical Engineering, Stanford University, Stanford, CA 94305, U.S.A.
[1]Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305, U.S.A.
Tel: (650) 725-3612, Fax: (650) 725-6278, E-mail: chion@stanford.edu

Abstract

For the first time, we have successfully demonstrated the use of a high-κ gate dielectric material ZrO_2 for CMOS applications on a pure germanium substrate. Using a low-temperature formation technique, we achieved excellent C-V characteristics with hysteresis of 1.5mV and a capacitance-based equivalent SiO_2 thickness ($t_{ox,eq}$) of about 5Å. Additionally, excellent device uniformity and very high device yield were attained.

Introduction

The higher carrier mobility [1] and dopant solubility of Ge allows for more aggressive MOS device scaling. However, the unstable native oxide hinders the passivation of Ge surface [2]. Inspired by the success of high-κ deposition techniques on Si [3,4], we have investigated the possibility of applying high-κ to Ge. In this work, we focus on the electrical characteristics of the MOS capacitors using ZrO_2 as the gate dielectric, and the effects of surface treatments intended to remove the GeO_2 interface layer.

Experiments

To compare the effect of different ZrO_2-to-Ge interface layers, various surface preparations on <100> oriented lightly doped n- and p-type Ge substrate were performed (Table 1). Sample #1 and #2 contained native germanium oxide while #3 and #4 were oxide-free. Only Sample #1 was thermally oxidized in dry O_2, while the others had ZrO_2 films grown on them. Zirconium oxide was formed using a low temperature method in order to minimize any possible reactions between Ge and the dielectric [4]. Platinum was sputtered and etched as the top electrode for capacitors. Finally, all the samples were subjected to a forming gas annealing at 410ºC.

Results and Discussions

For capacitors with only germanium oxide (native and thermal) dielectric, noisy C-V characteristics are observed (Fig. 1). Together with ~0.2V of hysteresis, frequency-dependent accumulation capacitance is found, and at 1.5V gate bias, the accumulation leakage current is $146A/cm^2$.

The high-k gate stack of $Pt/ZrO_2/GeO_2/Ge$, on the other hand, shows a C-V characteristic with large hysteresis (Fig. 2). The extracted value of $t_{ox,eq}$ without any QM correction is ~13Å. While, the kink near inversion indicates some "slow" surface states near the Ge conduction band, which is consistent with the symmetrically high inversion leakage current as in accumulation (Fig. 3) and also the frequency-dependent capacitance.

Fig. 4 shows the C-V for the gate stack in which an attempt was made to remove GeO_2 by DI water rinse. Hysteresis of 22mV is seen and a kink is observed near accumulation as explained before. Equivalent oxide thickness ($t_{ox,eq}$) is ~8Å and J_g is about $5A/cm^2$ at 1.5V gate bias, however the V_T varies from device to device. Vapor HF etch was also used in an attempt to prepare an oxide-free Ge <100> surface (Sample #4). Fig. 5 shows the high-resolution cross-sectional TEM image of this sample. From Fig. 6, the C-V has extremely small hysteresis (1.5mV) and minimal dependence on frequency. The $t_{ox,eq}$ measured is 4.6Å prior to any QM correction.

Measurements from Sample #3 and #4 suggest that in the absence of the poor-quality and relatively unstable GeO_2 interface layer, hysteresis becomes negligible. More importantly, they indicate an additional high-quality interface layer between the ZrO_2 and Ge is not a prerequisite for excellent electrical characteristics, contrary to previous results for Si high-κ [5]. The current results imply that high-κ dielectric compatibility can be achieved more easily in Ge MOS devices. Excellent device uniformity from die center to periphery is exhibited as shown in Fig. 7. The gate leakage current is low ($5.3A/cm^2$) and the device yield is close to 100%. Lastly, after constant-current stressing with $664C/cm^2$, only a small 1.24mV shift of V_{FB} is observed.

Conclusions

Using high-κ materials on pure Ge, excellent capacitor C-V and J_g-V_g characteristics have been demonstrated. Small hysteresis and extremely small $t_{ox,eq}$ have been achieved using this low-temperature formation technique. By eliminating the interface layer requirement, high-κ dielectrics for Ge MOS devices should be more practical than Si. This technology should allow fabrication of high performance transistors needed in sub-20nm regime.

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References

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Table 1 Different surface preparations for different interface layers (between ZrO_2 and the Ge substrate) and dielectrics stacks.

Sample	Doping	Native Oxide	Thermal Oxidation	ZrO_2 Deposition
#1 (W3)	N	Kept	500°C, 2mins	-
#2 (W8)	P	Kept	-	~35Å
#3 (W7)	N	Stripped in DI water	-	~35Å
#4 (W6)	N	Stripped in vapor HF	-	~35Å

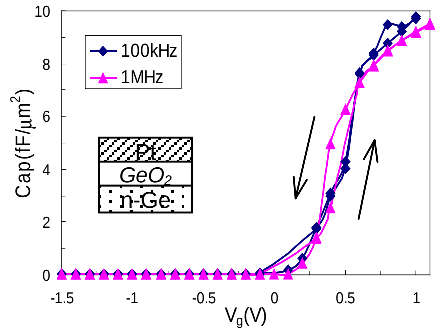

Fig. 1 Bi-directional HF C-V curves for the Pt/GeO_2/Ge structure (#1). Slight frequency dependence and hysteresis is observed.

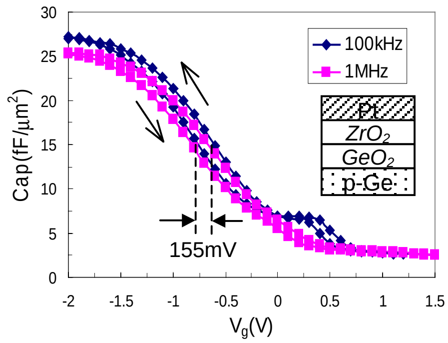

Fig. 2 HF C-V curves for the Pt/ZrO_2/GeO_2/Ge structure (#2). Large hysteresis and high density of interface state near inversion; $t_{ox,eq} \approx$ 13Å.

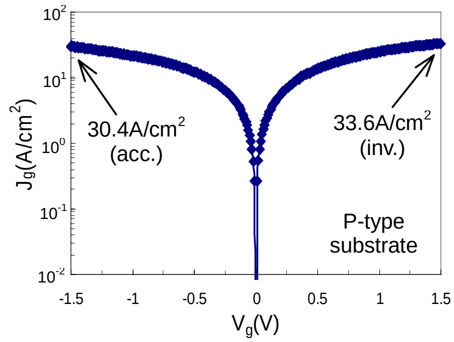

Fig. 3 Corresponding J_g-V_g curves from Sample #2. The leakage current density is similar for different gate polarities.

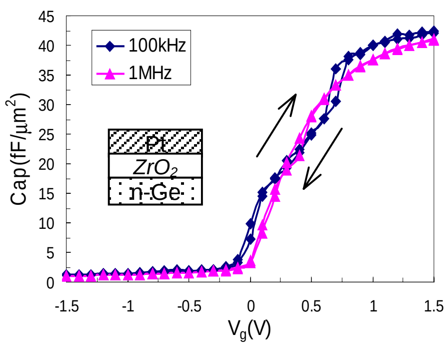

Fig. 4 HF C-V curves for the Pt/ZrO_2/Ge stack with DI water treatment (#3). Very small hysteresis (22mV) obtained. $t_{ox,eq} \approx$ 8Å.

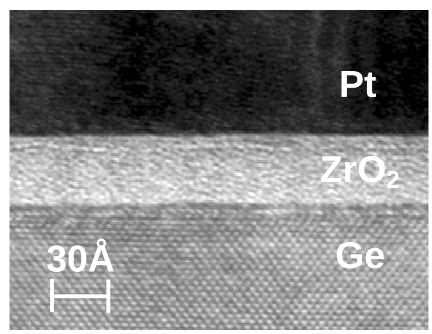

Fig. 5 HRTEM image of Pt/ZrO_2/Ge (#4). The physical thickness of ZrO_2 film is 36Å.

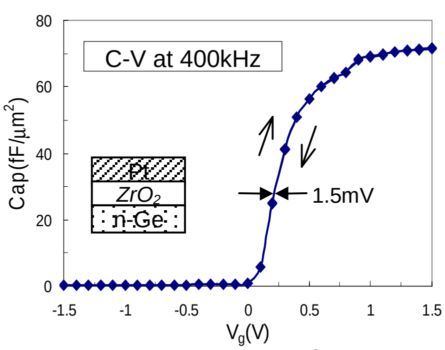

Fig. 6 Hysteresis estimation from bi-directional C-V measurement on Sample #4. Data for 400kHz is arbitrarily chosen.

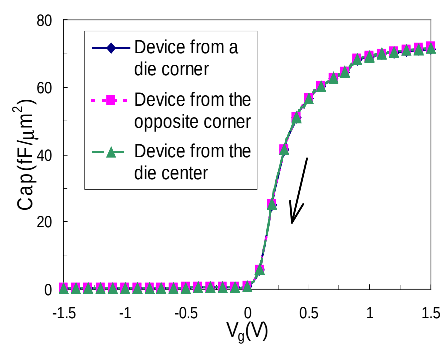

Fig. 7 C-V data from devices at one die corner, the die center and the opposite die corner. Excellent uniformity demonstrated.