Student paper

High Mobility Ge pMOS Fabricated using a Novel Heteroepitaxial Ge on Si Growth Method

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Abstract

Using a novel multi-step *in-situ* growth and hydrogen annealing process heteroepitaxial-germanium layers have been grown directly on silicon, with defects confined near the Si/Ge interface, thus not threading to the surface as expected in this 4.2% lattice mismatched system. The results achieved are fully-relaxed smooth single crystal Ge layers on Si with defect density reduced to ~ 1 x 10^6 cm^{-2} without a graded buffer layer or CMP step. To demonstrate the quality of the Ge layers, pMOSFETs have been fabricated using a sub-500 ^{o}C process with low field mobility of ~250 cm^2/V-sec.

Introduction

Recently Ge has emerged as a viable candidate to augment Si for CMOS applications [1]. However, for Ge to become main-stream, heterogeneous integration of crystalline Ge layers on Si must be achieved. This is not straightforward due to the large lattice mismatch (4.2 %) between Ge and Si, which limits the quality of the heteroepitaxial growth. Such growth is associated with large density of defects and surface roughness, causing difficulties in process integration, (Fig 1). People and Bean have calculated that to grow 10nm of Ge_xSi_{1-x} film without dislocations, one has to limit the Ge content to less than 50% [2]. In this work, we report a novel method to reduce the surface roughness and confine the threading segments of misfit dislocations near the Si/Ge interface using an *in-situ* multi-step growth of Ge and hydrogen annealing process. To demonstrate the crystal and interface quality, pMOS transistors were fabricated using a sub-500^{o}C process.

Heteroepitaxial Ge on Si Growth Process

We grew 155 nm epitaxial Ge layers on (100) Si at 400°C at a reduced pressure of 10 Torr. A hydrogen annealing were carried out for 1 hr immediately following the epitaxial growth, at 825°C at a pressure of 80 Torr reducing the surface roughness to 2.9 nm from 24 nm. [3] It was shown that hydrogen atoms attach to the Ge atoms reducing the diffusion barrier for Ge and thus increasing Ge surface mobility [3]. After the first growth, an additional layer of Ge was grown using the same growth conditions as before and a hydrogen annealing at 700°C and 80 Torr was carried out. Figure 2 is a cross sectional TEM of the double annealed sample (400 nm). The threading segments of misfit dislocations have been deposited at the Si/Ge interface leaving a high quality Ge layer. The RMS roughness after the second growth was about 0.2 nm from a 1 μm x 1μm scan and was on the order of 3 nm from a 10 μm x 10 μm scan. We discuss the results in terms of misfit stress-and thermal expansion mismatch stress-driven threading dislocation glide and Si-Ge interdiffusion during the high temperature hydrogen annealing. These separate processes act to relieve the misfit strain as confirmed by XRD (Fig 3). The hydrogen ambient avoids formation of a surface oxide, allowing for Ge surface diffusion to reduce the large surface roughness of the initial thin epi-layer. In order to measure the threading dislocation density, we grew thicker 4.5 μm epi-Ge layers. After the first growth and anneal as above, the temperature was increased to 430 °C for 15 min and then 500 °C for 15 min followed by a1 hour hydrogen anneal at 700 °C. A chemical etch treatment consisting of- CH3COOH (67 ml), HNO3 (20 ml), HF (10 ml) and I_2 (30 mg) was performed. Figure 4 is a plan view optical micrograph showing etch pits on a 4.5 μm thick Ge epi-layer using the MHAH method. The defect density was counted to be around 1 x 10^6 cm^{-2}, thus not readily detected by cross section TEM imaging. RBS measurements indicated the thin ~155nm Ge layer was 91% Ge while the ~400nm Ge layer was 96% Ge and the 4.5 μm epi-Ge layer yielded 100% Ge.

p-MOS Fabrication

Using the double growth 600 nm epi-Ge as the starting substrate pMOS transistors were fabricated. Field isolation was done first by rapid thermal nitridation (RTN) of Ge in NH_3 at 600ºC followed by LPCVD SiO_2 (LTO) deposition. After active area opening, gate dielectric was formed by GeO_xN_y was growth by RTN followed by LTO deposition. An *in-situ* boron doped SiGe gate was grown by CVD at 500°C, the highest temperature of the process. After gate definition and self aligned source drain B implant, a 450°C RTA was used to activate the dopant. Contacts were defined by LTO/Aluminum. A 400°C FGA anneal concluded the process. Figure 5 is a schematic cross section of the final device fabricated and a high resolution cross sectional TEM image showing the high quality interface. Figure 6 is the I_s-V_d characteristic of the device while figure 7 is the I_d-V_d of the device. Additional leakage from the drain side is evident. Figure 8 is the I_{sub}-V_d and the I_g-V_d, showing the leakage being the drain to substrate leakage from either junction leakage or electrostatic interaction between drain and defect- confined region due to thin epi-Ge layers used in the fabrication.

Mobility Extraction

Effective mobility (μ_{eff}) versus effective field for pMOS Ge devices was extracted using the simple I_d-V_d method according to

$$\mu_{eff} = \left(\frac{2L}{W}\right) \times I_d \times \frac{1}{C_{ox}\left(V_g - V_t\right)} \text{ and } E_{eff} = \frac{V_t - V_{fb} - 2\psi_B}{4t_{ox}} + \frac{V_g - V_t}{12t_{ox}} \quad [4].$$

μ_{eff} was calculated at two points to be ~ 250 cm^2/V-sec at effective field of 0.15 MV/cm and 95 cm^2/V-sec at effective field of 0.21 MV/cm. This corresponds to 2× enhancement at low effective field and a 3× enhancement at high effective field compared to Si pMOS university mobility.

Conclusion

A novel multi growth and *in-situ* hydrogen annealing has been developed to grow heteroepitaxial-Ge layers on silicon with low surface roughness and threading dislocations. These high quality epi-Ge layers are achieved without a graded buffer layer or additional CMP steps greatly reducing the complexity of the process. We fabricated pMOSFETs that gave high effective mobility of ~250 cm^2/V-sec. This technology will simplify heterogeneous integration of Ge and Si, and fabrication of GOI substrates using epi-Ge.

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References

[1] Chui *et al.*, *IEEE EDL*, vol. 23, p. 473, 2002.
[2] People *et al.*, *APL*, vol. 47, p. 322, 1985.
[3] Nayfeh *et al*, vol. 85, p. 2815 2004
[4] Y. Taur *et al*, *Fundamentals of Modern VLSI devices*, 1998 (132-135)

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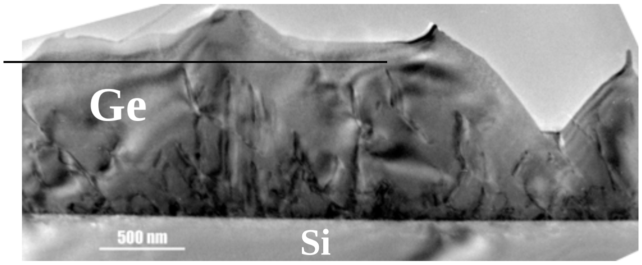


Figure 1. As Grown CVD Ge on Si (at 400 °C and 10 Torr). Surface Roughness and Misfit/Threading Dislocation dominate the growth making it unsuitable for electrical devices.

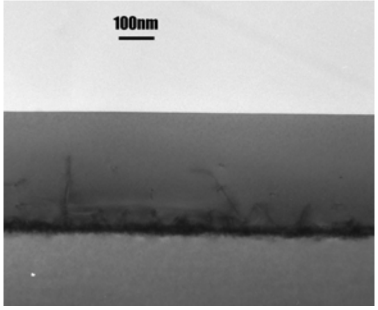


Figure 2. Cross Sectional TEM of Heteroepitaxial-Ge on Si using in-situ multiple growth and hydrogen annealing process. *(Growth: 400C and 10torr, H_2 80 Torr bake 1: 825 °C-1hr and bake 2: 700 °C 1hr.* Threading Dislocations are confined to Ge/Si interface.

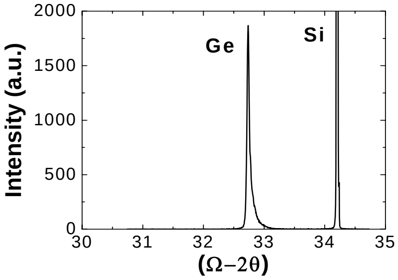


Figure 3 X-ray Scattering intensity for epi-Ge layer on Si using XRD *(same conditions as figure 4)* The epi-Ge is single crystal and fully-relaxed.

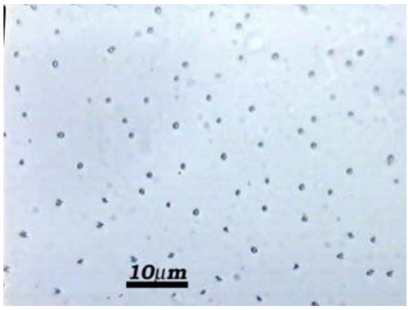


Figure 4 Optical Microscope 100× plan view image after defect etch: Threading Dislocation Etch Pits (EPD): 1×10^{-6} cm^{-2}

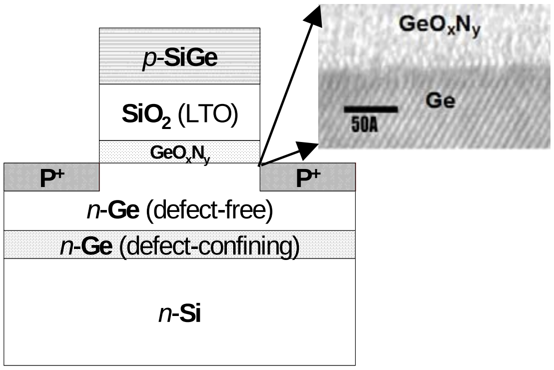


Figure 5. Cross Sectional Schematic of pMOS epi-Ge transistor fabricated; inset: High Resolution Cross Sectional TEM of GeOxNy/Ge stack showing the Ge single crystal lattice and high quality interface.

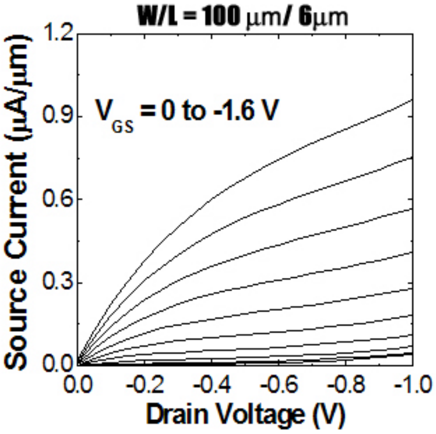


Figure 6 I_s-V_d characteristics

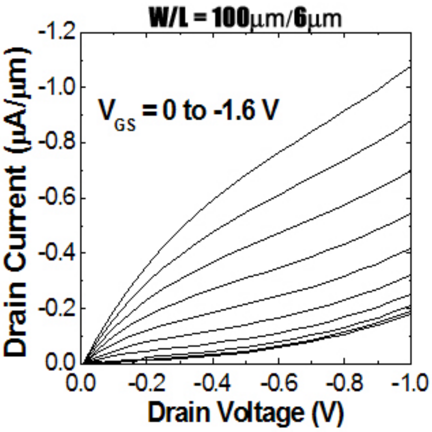
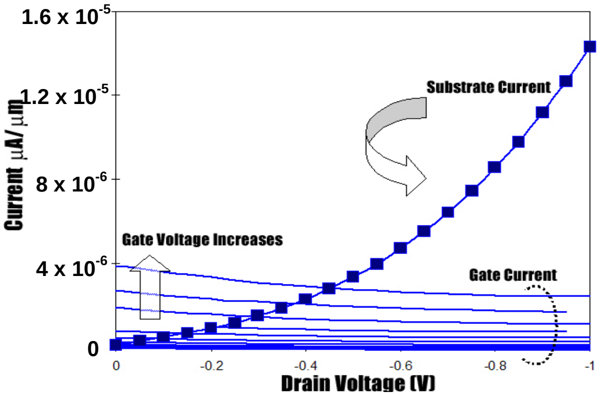


Figure 7 I_s-V_d characteristics



Fiure 8. **I_{sub}/I_{gate}-V_d** characteristics; I_{sub} is independent of V_g