

Low Thermal Budget Ge MOS Technology

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ABSTRACT

A simple and novel low thermal budget self-aligned gate-last MOS process integrating metal gates and high- κ dielectrics on Ge has been demonstrated. Dopant incorporation in Ge has been studied using rapid thermal annealing of various commonly implanted ionic species and diffusion from doped oxides. We have demonstrated symmetrically high levels of electrical activation of both p - and n -type dopants in germanium. T-SUPREMTM simulations were used to fit the experimental profiles and to extract the diffusion coefficient of various dopants. Improved surface passivation for excellent gate dielectric technology and field isolation and dopant incorporation with high surface concentration and shallow junctions have been developed.

INTRODUCTION

The saturation of Si MOSFET drain current upon dimension shrinkage may limit the prospect of future scaling of the MOS devices. To scale the MOSFETs into sub 20 nm regime a structure like shown in Fig. 1 will be needed. A combination of high mobility material like Ge to enhance the transport, a double gate structure to alleviate the problem of poor electrostatics in the channel region and high- κ gate dielectric to minimize the gate leakage appears to be a very promising solution.

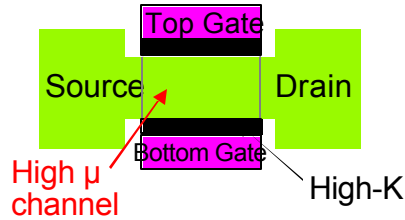


Fig. 1. Schematic of a MOSFET structure scalable to below 20 nm.

The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, v_{inj} , [1-2], which translates into higher drive current, I_{DS} ,

$$I_{DS} = W \times Q_{inv} \times v_{inj}$$

and smaller gate delay,

$$\frac{C_{LOAD} V_{DD}}{I_{DS}} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$

where Q_{inv} is charge induced in the channel, W and L_{gate} are the channel width and length, respectively, V_{DD} is the supply voltage, V_T is the threshold voltage, I_{DS} is the drain current, and C_{LOAD} is the capacitance being driven by the transistor.

However, surface passivation for gate dielectric and field isolation, and n -type dopant incorporation are the two classic problems that obstruct CMOS device realization in Ge. The recent success of high- κ gate dielectrics to passivate Ge surface [3-5] led to the demonstration of Ge p -MOSFETs [6-8]. Most of these efforts used simple structures with large geometries not appropriate for nanometer scale VLSI devices where Ge would be useful. In this work we present two techniques for dopant incorporation for shallow

junctions in Ge: 1) rapid thermal anneal (RTA) of ion-implanted dopants and 2) diffusion from doped oxide. We also demonstrate a low thermal budget technology for Ge MOSFETs with both HfO_2 and ZrO_2 and metal gates using a simple self-aligned low thermal budget gate-last process.

N-TYPE DOPANT INCORPORATIONS

Previous experimental results on both p - and n - type dopant activation and diffusion in Ge are not applicable to advanced CMOS. For p -type dopants, most reports are on furnace annealing of ion-implanted B, [9-10] which show only medium-to-high levels of activation that are lower than the ITRS requirement. Prior data on n -type implantation doping with P, As, and Sb were either at a very high implant energy [11] or used furnace annealing [12]. Hattangady *et al.* reported both RTA and FA data on As as well, although the implant dose range and level of activation were low for futuristic device applications [13]. In this work, we demonstrate symmetrically high levels of activation on both p - and n -type dopants in Ge, at concentrations directly applicable to advanced CMOS.

In the first set of experiments [14] room temperature implantation of various ionic species at a fixed dose of $4 \times 10^{15} \text{ cm}^{-2}$ were carried out at energies corresponding to a similar projected range (R_p) in germanium with substrate $\langle 100 \rangle$ orientation. $^{49}\text{BF}_2$ ions with 20 keV were used to form p^+ junctions in n -Ge, while 18 keV ^{31}P , 30 keV ^{75}As , and 45 keV ^{121}Sb ions were employed to make n^+ junctions in p -Ge. The ion beams were tilted by 7° to the substrate surface normal to minimize channeling.

RTA was then performed in a N_2 ambient at temperatures of 600-850 $^\circ\text{C}$ for 1-300 secs to activate dopants and remove the implantation damage. The chemical concentration profiles were examined with Secondary Ion Mass Spectroscopy (SIMS) and the electrically active dopant depth profiles were measured by Spreading Resistance Probe (SRP). The details of this work are described in [14]. The SRP results are shown in Fig. 2.

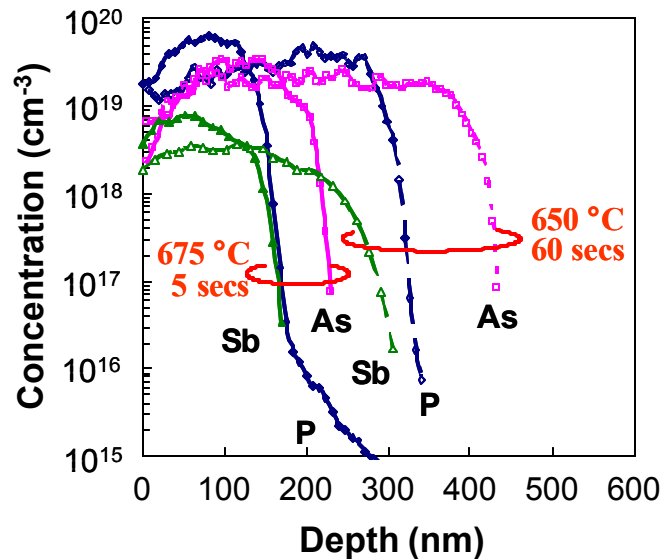


Fig. 2. SRP profiles of various n -type dopants in Ge after two different RTA treatments (675 $^\circ\text{C}/5$ secs and 650 $^\circ\text{C}/60$ secs). Implantation of various ionic species at a fixed dose of $4 \times 10^{15} \text{ cm}^{-2}$ were carried out at energies corresponding to a similar projected range [14].

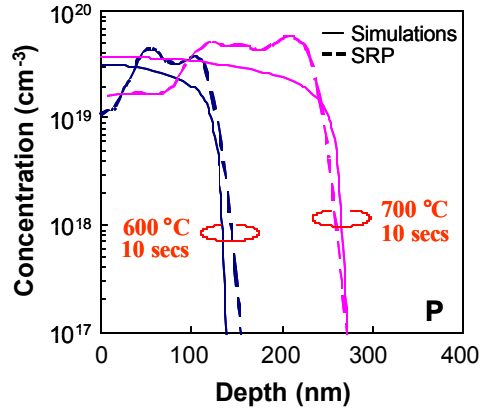


Fig. 3. T-SUPREMTM simulation fits (solid lines) with SRP profiles (dashed lines) for 10 secs RTA at 600°C and 700°C on phosphorus implanted Ge [14].

The experimentally obtained activated and diffused profiles were simulated and fitted using T-SUPREMTM for As, Sb, and P as shown in Fig. 3. From the simulations, we have extracted the diffusion coefficients of various dopants in Ge. The results are shown in Table 1. These results indicate that ion implanted junctions result in slow *p*-type but fast *n*-type dopant diffusion.

Table 1. Extracted diffusion coefficients and the associated model for various *n*-type dopants in Ge [14].

Dopants	Model	E_A (eV)	D^0 (cm ² /sec)
P	$(n/n_i)^2$	2.07	4.38×10^{-2}
As	$(n/n_i)^2$	3.32	1.45×10^6
Sb	n/n_i	2.28	1.189×10^1

Conventional ion implanted junctions result in fast *n*-type dopant diffusion in Ge due to effects like transient enhanced diffusion (TED) from implant damage. To prevent this, extensive studies on solid source diffusion (SSD) from phosphorus-doped SiO₂ (PSG) were launched as an alternative. PSG was deposited by low pressure chemical vapor deposition (LPCVD) in a hot wall furnace from a mixture of SiH₄ and PH₄. No observable out-diffusion from PSG into Ge occurred below 800 °C even after 10 hours. This could be attributed to the very low P diffusivity in PSG. To avoid significant P diffusion in Ge while maximizing the peak concentration, high temperature (below the Ge melting point) RTA was adopted. The standard SRP depth profiles for RTA at 850°C are presented in Fig. 4, demonstrating peak concentrations are always at the Ge surface.

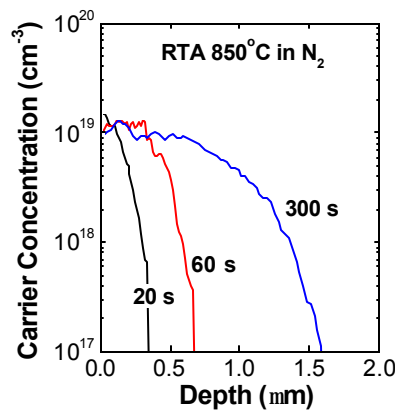


Fig. 4. SRP data showing electrically active junction doping profiles after RTA at 850°C for different times.

SURFACE PASSIVATION AND GATE DIELECTRIC TECHNOLOGY

The poor quality Ge native dielectrics for gate insulator and field isolation have been one of the classic problems that obstruct VLSI CMOS device realization in Ge. For instance, a mixture of Ge oxides (GeO and GeO_2) would form on the surface upon air exposure with the former desorbs at 420°C [15] and the latter dissolves in water. In order to obtain a more stable native passivation layer, either thermal or plasma anodic nitridation was applied to transform the Ge oxides to Ge oxynitrides (GeO_xN_y) [16-17]. However, from a scaling standpoint, employing the Ge oxynitride alone would not be sufficient for gate leakage suppression required beyond the 32 nm technology node. Instead the use of high- κ dielectric directly [3,18] or high- κ on oxynitride [5] on Ge has shown some promises. Among other deposition techniques, atomic layer deposition (ALD) is particularly attractive in terms of precise thickness control and near-perfect conformality for ultrathin high- κ formation. In this work, we have investigated the effects of different Ge surface preparations prior to ALD high- κ deposition on an optional Ge oxynitride interlayer.

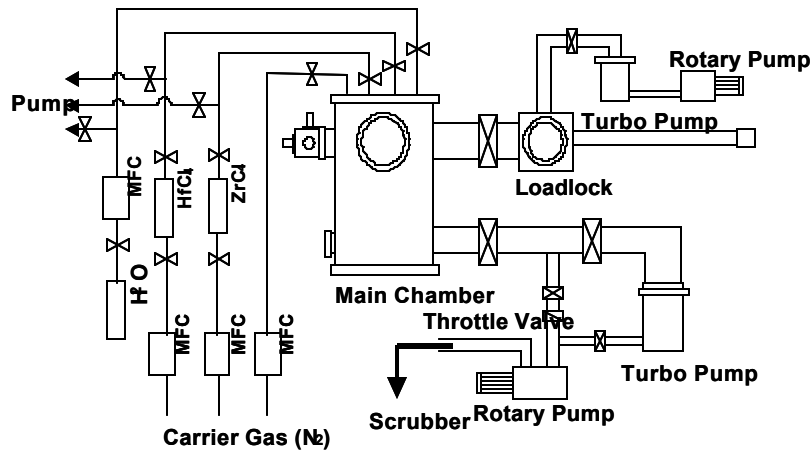


Fig. 5. Schematic diagram of the ALD system.

The high- κ dielectrics (HfO_2 or ZrO_2) used throughout this work were deposited in a cold-wall high vacuum ALD system (Fig. 5) at 300°C , using alternating surface-saturating reactions of metal tetrachloride and H_2O precursors [18]. Metal gate MOSCAPs were fabricated using 30 \AA ALD high- κ dielectrics on Ge substrate with various surface preparations. The gate leakage currents measured (Fig. 6) were similarly low for different splits except the one with thick Ge oxynitride (GeO_xN_y), which gave an even lower leakage.

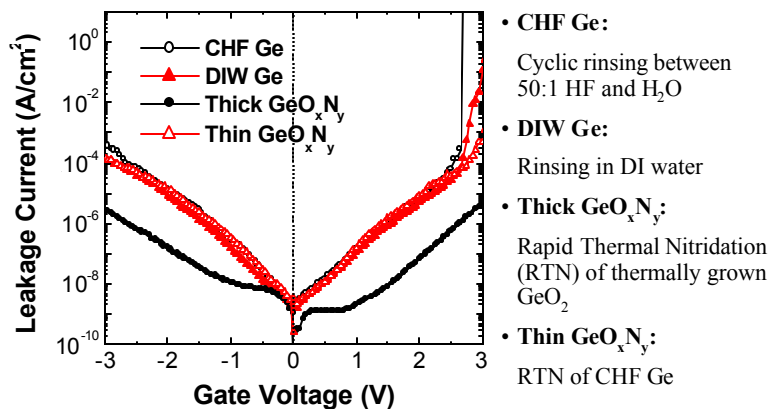


Fig. 6. Leakage current density vs. gate voltage for various surface passivations followed by ALD of high- κ films.

Equivalent SiO₂ thickness (EOT) and C-V hysteresis were also extracted (Fig. 7) from these MOSCAPs indicating that the best electrical result could be produced by rapid thermal nitridation (RTN) of cyclic HF (CHF) cleaned Ge. On the optimum GeO_xN_y film, wet processing stability was investigated and the film was shown to be much less soluble in H₂O but soluble in HF. In brief, the optimum dielectric stack could be attained by RTN of CHF cleaned Ge at 600 °C followed by ALD high-κ. Fig. 8 shows a high resolution cross-sectional TEM of this sample. Excellent C-V characteristics were obtained from MOSCAPs on both Ge substrate types (Fig. 9) with low leakage (Fig. 6).

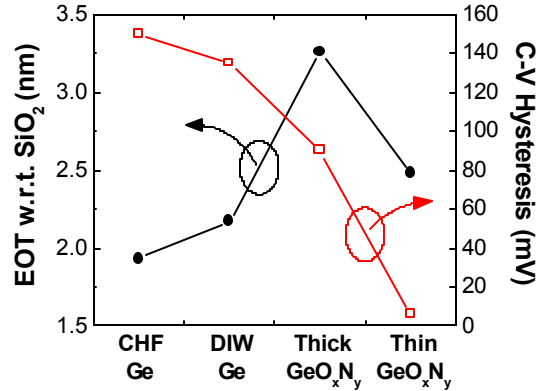


Fig. 7. EOT and C-V hysteresis obtained from Ge MOS capacitors with different Ge surface passivation prior to ALD of high-k dielectric.

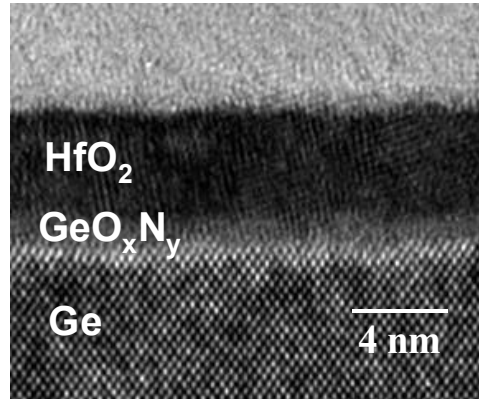


Fig. 8. High resolution cross-sectional TEM image of ~45 Å ALD HfO₂ on ~11 Å GeO_xN_y interfacial layer grown on Ge.

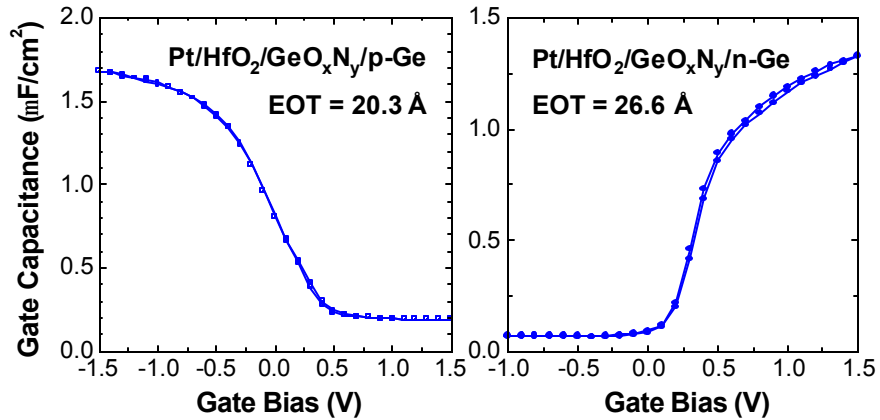


Fig. 9. C-V characteristics at 800 kHz of Pt gate MOS capacitor with HfO₂ on oxynitrided Ge substrates.

TRANSISTOR FABRICATION PROCESS

N-channel Ge MOSFETs with 1-2 μm gate length and conventional field isolation were fabricated using a self-aligned gate-last novel process [19-20] with ALD high- κ gate dielectrics and metal gates and optimum source/drain shallow junctions by diffusion from doped oxides.

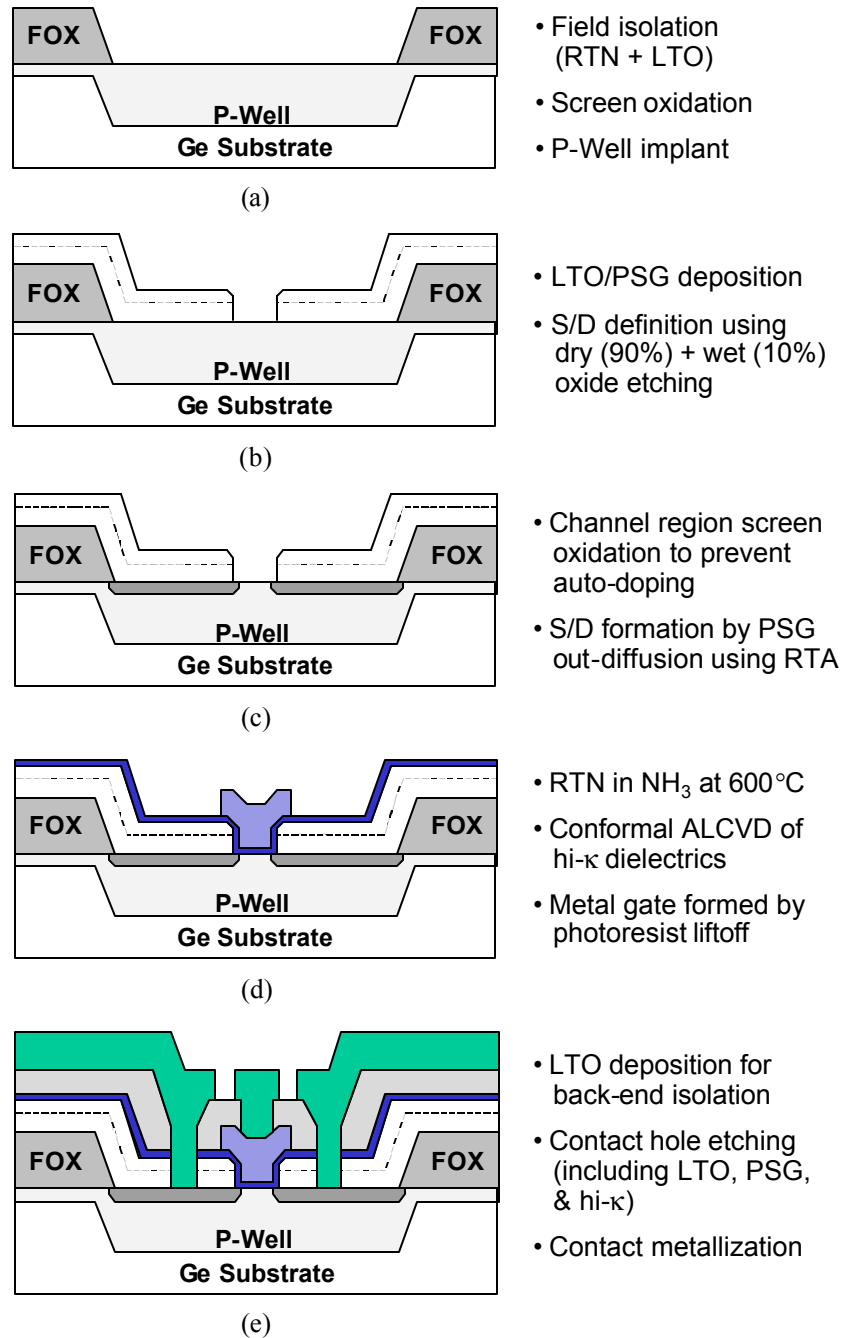


Fig. 10. The simple and novel self-aligned gate-last Ge MOSFET process flow using diffusion from doped SiO_2 .

The novel self-aligned gate-last process is summarized in Fig. 10. The starting substrates were very lightly doped $\langle 100 \rangle$ oriented Ge wafers. Field isolation was done first by RTN at 600°C and then LPCVD SiO_2 (LTO) deposition. After active area opening, a screen oxide on the Ge surface was thermally grown followed by *p*-well implant (Fig. 10(a)). 8 wt% PSG was then deposited before the LTO capping. The source/drain regions were defined by etching the LTO/PSG above the channel (Fig.

10(b)). To further prevent auto-doping from the PSG sidewall, another screen oxide was grown prior to source/drain formation by diffusion from PSG using RTA (Fig. 10(c)). RTN of Ge was then performed at 600 °C followed by ALD of about 30 Å of ZrO₂ or HfO₂. Pt gate electrodes overlapping the source/drain were formed by photoresist liftoff (Fig. 10(d)). The gate-last process was completed by LTO back-end passivation, contact hole etching, and Al + 1% Si metallization (Fig. 10(e)).

With this simple process, the stringent thermal stability requirement on the metal gate/high- κ stack during dopant activation is relaxed, while serving a similar purpose as the more-involved replacement gate process. In addition, a selective etch of the gate electrode metal versus high- κ , and high- κ versus Ge is no longer essential due to the presence of thick buffer LTO/PSG underneath (Fig. 10(d)). Extension of this process to make lightly-doped drain (LDD) is trivial by incorporating lower wt% PSG spacers inside the channel open region in Fig. 10(b). CMOS could simply be made by etching off the PSG from the PMOS areas followed by a blanket BSG deposition. Lastly, heavily-doped Ge could be employed in place of PSG and thus also act as automatic elevated source/drains. However, a highly selective etch is then required.

CONCLUSIONS

Dopant incorporation in Ge has been studied using rapid thermal annealing of various commonly implanted ionic species and diffusion from doped oxides. We have demonstrated symmetrically high levels of electrical activation of both *p*- and *n*-type dopants in Ge. Improved surface passivation for excellent high- κ gate dielectric technology and field isolation has been demonstrated. A simple and novel low thermal budget self-aligned gate-last MOS process integrating metal gates and high- κ dielectrics on Ge has been developed.

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