

Gate Dielectrics for Ge MOS Technology

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Historically, Ge had been one of the most important semiconductors in the past as the first MOSFET and the integrated circuit were fabricated in Ge. On the other hand, its inferior properties of GeO₂ as compared to SiO₂ makes this dielectric unsuitable for Ge MOSFET gate insulation and field isolation, which has therefore obstructed very large-scale integration (VLSI) realization in Ge for decades. Efforts to use materials like SiO₂ on a thin Si cap, Ge₃N₄, etc. have been only marginally successful. Inspired by the recent successes of the high-k dielectrics on Ge has emerged as a viable candidate to augment Si for CMOS applications. However, for Ge to become main-stream, heterogeneous integration of crystalline Ge layers on Si must be achieved. In this paper we present a review of our recent work on the heteroepitaxial growth of Ge on Si and surface passivation with its native oxynitride (GeO_xN_y) and high-permittivity (high-k) metal oxides of Zr and Hf.

Heteroepitaxial growth of Ge on Si is not straightforward because of the large lattice mismatch (4%) between Ge and Si, which limits the quality of the heteroepitaxial growth. First, above the critical thickness, the layer will have many misfit dislocations making it unusable for any practical applications. Second, the growth of Ge on Si results in island morphology. Such growth is associated with large surface roughness, causing difficulties in process integration. Using a novel multi-step growth and hydrogen anneal process we have grown heteroepitaxial-germanium layers directly on silicon, with defects confined near the Si/Ge interface, thus not threading to the surface as expected in this 4.2% lattice mismatched system [1]. The results achieved are defect-free fully-relaxed smooth single crystal Ge layers on Si without any graded buffer SiGe layer.

Surface passivation was studied using two different techniques: (1) growth of Ge oxynitride and (2) atomic layer deposition (ALD) of high-k metal oxides of Hf and Zr. The oxynitride formation was studied by an initial rapid thermal oxidation (RTO) in dry O₂ at 500-600°C followed by *in-situ* RTN at 500-700°C in NH₃ ambient to convert the Ge oxides into GeO_xN_y [2]. Optimum process temperature for both RTO and RTN was found to be 600°C. The degree of nitridation in GeO_xN_y should be optimized for best results. Over-nitridation led to excessive carrier generations near the nitrided GeO_xN_y/Ge interface, increased interfacial charge trapping and positive oxide fixed charge generation which may ultimately degrade channel mobility. The RTN technique was also employed to passivate the Ge surface prior to the deposition of SiO₂ for field isolation [3].

HfO₂ and ZrO₂ were deposited in a cold-wall atomic-layer deposition (ALD) system at 300°C, using alternating surface-saturating reactions of metal tetrachloride and H₂O precursors. ALD of ZrO₂ films on Ge exhibited local epitaxial growth without a distinct interfacial layer [4]. However, C-V measurements showed significant C-V hysteresis and frequency dispersion, possibly due to metal diffusion in Ge [5] and surface defects. Effect of different surface preparations prior to high-k ALD was studied. To study the effect of different surface preparations prior to high-k ALD, gate leakage currents, equivalent oxide

thickness (EOTs) and hysteresis from the corresponding MOS capacitors were fabricated and characterized. Among them cyclic rinsing between HF and H₂O (CHF) for cleaning Ge and rapid thermal nitridation (RTN) in NH₃ gave the best results. The optimum dielectric stack could be attained by RTN of CHF Ge at 600°C followed by hi-κ ALD [3,5,6]. Excellent C-V curves were obtained from MOS capacitors on both Ge substrate types with low leakage. In the absence of GeO_xN_y it was found that metal from high-k dielectric diffused in the Ge substrate [5].

Efficacy of heteroepitaxial growth of Ge on Si and surface passivation have been demonstrated through fabrication of Ge *p*-MOSFETs [3,7] using three different gate dielectric schemes: (1) GeO_xN_y, (2) ZrO₂ and (3) HfO₂ on GeO_xN_y and 2 different metal gates: (1) Pt and (2) W using a low thermal budget process. Best mobility results were obtained with either GeO_xN_y or HfO₂ on ultrathin GeO_xN_y. Low gate leakage could be obtained only for HfO₂ on ultrathin GeO_xN_y. *n*-MOSFETs have been also demonstrated but need improvement in performance [3].

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References

- [1] A. Nayfeh, C. O. Chui, K. C. Saraswat and T. Yonehara, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality," *Appl. Phys. Lett.*, Vol. 85, No. 14, pp. 2815-2817, 4 Oct. 2004
- [2] C. O. Chui, F. Ito and K. C. Saraswat, "Scalability and Electrical Properties of Germanium Oxynitride MOS Dielectrics", *IEEE Electron Dev. Lett.*, Vol. EDL-25, pp. 613-615, Sept. 2004.
- [3] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "A Germanium NMOSFET Process Integrating Metal Gate and Improved Hi-k Dielectrics," *IEEE Int. Electron Dev. Meet. 2003 Technical Digest*, Washington, DC, (2003) 437-440.
- [4] H. Kim, C. O. Chui, K. C. Saraswat and P. C. McIntyre, "Local epitaxial growth of ZrO₂ on Ge (100) substrates by atomic layer epitaxy," *Appl. Phys. Lett.* 83, 2647, (2003).
- [5] H. Kim, P. C. McIntyre, C. O. Chui, K. C. Saraswat and M. H. Cho, "Interfacial characteristics of HfO₂ grown on nitrided Ge (100) substrates by atomic-layer deposition," *Appl. Phys. Lett.*, Vol. 85, No. 14, pp. 2902-2904, 4 Oct. 2004
- [6] C. O. Chui, H. Kim, P. C. McIntyre and K. C. Saraswat, "Atomic Layer Deposition of High-k Dielectric for Germanium MOS Applications – Substrate Surface Preparation," *IEEE Electron Dev. Lett.*, Vol. 25, (2004) 274-276.
- [7] A. Nayfeh, C. O. Chui, T. Yonehara and K. C. Saraswat, "Fabrication of high-quality *p*-MOSFET in Ge grown heteroepitaxially on Si," *IEEE Electron Device Lett.*, Vol. 26, pp. 311-313, May 2005.