Interface Layers for High-k/Ge Gate Stacks: Are They Necessary?

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Dimensional scaling of MOSFETs has created a new “golden age” of electronic materials, as a growing variety of insulators and conductors are required to minimize power dissipation and isolation problems in nano-scale circuits. Recently, attention has focused on the possible replacement of Si itself as the channel material in high-performance MOSFETs. Interest in semiconductors which have higher intrinsic carrier mobilities than Si for field-effect devices has been prompted by the difficulty of improving Si MOSFET performance while also shrinking dimensions to 10s of nm. Fabricating such devices on Ge channels has become possible because of 1) the development of approaches for integration of single crystal Ge layers on large-area Si substrates; [1-4] 2) the demonstration of new device structures which reduce pn junction leakage and band-to-band tunneling;[5] and 3) the discovery of deposited metal oxide dielectrics which appear, under some circumstances, to produce reasonably well-passivated gate insulator/channel interfaces.[6-9]

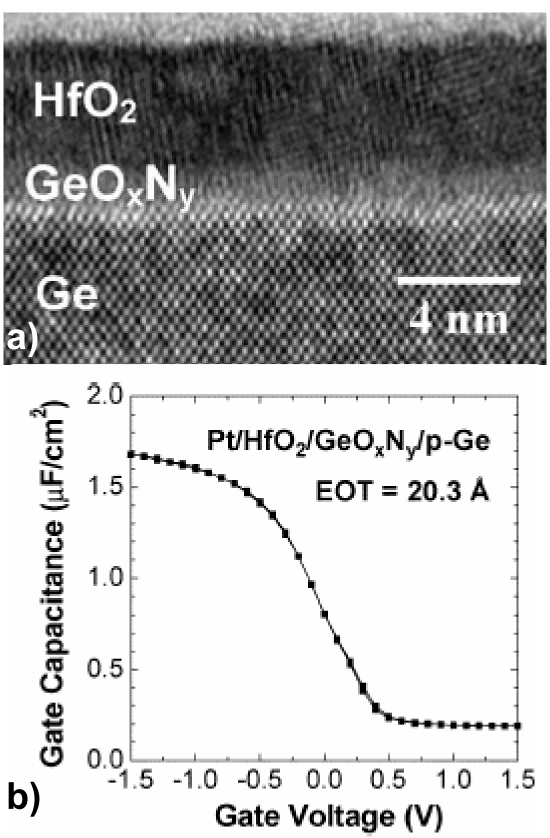

Fig.1. a) Cross-sectional TEM micrograph and b) capacitance-voltage data (800 kHz) for a Pt/ALD-HfO_2/GeO_xN_y/p-Ge MOS capacitor.[10]

The present understanding of the nature and control of defects at gate insulator/Ge interfaces is rather primitive. In many instances, intentional addition of interface layers between the high-k film and the Ge substrate surface has proved to be beneficial to gate stack electrical performance. Figure 1 shows a case in point: preparation of a GeO_xN_y interface layer by rapid thermal nitridation of Ge prior to atomic layer deposition (ALD) of HfO_2 was found to suppress CV hysteresis and reduce the frequency dispersion of the dielectric response of high-k/Ge MOS capacitors that did not include an intentional interface layer.[11]

The underlying reasons for these effects, and whether interface layers (either intentionally added or unintentionally formed) are required for fabrication of stable and reliable high-k/Ge devices, are not well-understood. Interface layers may be important as diffusion barriers, preventing undesirable interface reactions between high-k metal oxides and the Ge substrate. They may also produce an advantageous gradation in chemical bonding between the covalent semiconductor substrate and a relatively ionic, high oxygen coordination number, metal oxide insulator. Understanding the conditions under which interface layers improve electrical performance is very important because the permittivity and band gap of interface layer materials may limit future EOT scaling of Ge MOS devices.

In this paper, we will review experimental findings from our laboratory and others related to interface layer formation and electrical characteristics of high-k/Ge gate stacks. To the greatest extent possible, we will attempt to correlate the presence of interface layers and the nature of chemical bonding in them with observations of fixed charge, charge trapping and interface states. The problem of interdiffusion of species across the gate insulator/channel interface will be analyzed in some detail. Current prospects and the remaining challenges for engineering high-k/Ge interfaces will be summarized.

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