Germanium MOS Capacitors Incorporating Ultrathin High-κ Gate Dielectric

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***Abstract*—For the first time, we have successfully demonstrated the feasibility of integrating a high-permittivity (κ) gate dielectric material zirconium oxide into the MOS capacitors fabricated on pure germanium substrates. The entire fabrication process was essentially performed at room temperature with the exception of a 410 °C forming gas anneal. After processing steps intended to remove the germanium native oxide interlayer between the zirconium oxide dielectric and germanium substrate, an excellent capacitance-based equivalent SiO_2 thickness (EOT) on the order of 5–8 Å and capacitance–voltage (C–V) characteristics with hysteresis of 16 mV have been achieved. Additionally, excellent device yield and uniformity were possible using this low thermal budget process.**

***Index Terms*—Germanium, high-permittivity dielectric, MOS devices, surface passivation, zirconium oxide.**

I. Introduction

As THE scaling of classical bulk Si CMOS transistors approaches its fundamental limits, innovative device structures and new materials [1] must be considered to continue the historic progress in information processing and transmission. One such promising material is Ge due to several of its attractive properties including higher carrier mobility [2] for larger drive current, smaller mobility bandgap for supply voltage scaling, and smaller optical bandgap to broaden the absorption wavelength spectrum. Unlike silicon, however, the lack of a sufficiently stable native oxide hinders the passivation of Ge surfaces. During the last four decades, dielectric materials like SiO_2 [3], [4], SiO_2 on a thin Si cap [2], [5], GeO_2 [6], [7], Ge_3N_4 [8], [9], Ge oxynitride [10], [11], and Al_2O_3 [12], [13] have been attempted, although none of them would likely offer an EOT of less than 10 Å to advance beyond the sub-20 nm regime [1]. Inspired by the recent successes of the high-κ dielectric deposition technique on Si [14], [15] and the thermodynamically unstable nature of the common hexagonal phase of GeO_2, we have investigated the possibility of applying high-κ dielectrics to Ge without a native oxide interlayer. In this letter, we demonstrate Ge MOS capacitors with an ultrathin zirconium oxide gate dielectric fabricated using a low temperature growth technique.

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II. Device Fabrication

MOS capacitors were fabricated on the (100) oriented lightly doped Ge substrates using a one-mask level process. To compare the effect of the presence of an interlayer between the zirconia dielectric and Ge substrate, the Ge native oxides were either kept (Sample #1a on p-Ge and Sample #1b on n-Ge) or removed using DI water (Sample #2 on n-Ge) or HF vapor (Sample #3 on n-Ge) prior to the zirconia deposition. Due to the limited substrate availability, DI water and HF vapor treatments were not performed on p-type Ge.

In brief, zirconia was grown by the UHV sputtering of $\sim$ 20 Å Zr precursor films on the pre-treated Ge surfaces. The samples were transferred to the loadlock and oxidized *in situ* by room temperature UV ozone technique at 600 torr oxygen partial pressure for 60 min [15]. The samples were subsequently transferred back to the main chamber for deposition of $\sim$ 500 Å Pt as the top electrode layer. Circular capacitor structures were then defined by lithography and etching. Finally, all samples were subjected to forming gas anneal at 410 °C for 30 min.

III. Characterization and Discussion of Results

Fig. 1(a) and (b) show the gate capacitance–voltage (C–V) characteristics for samples with zirconia on native oxide on both p- and n-type Ge, respectively (Sample #1a and #1b). The EOTs extracted from the accumulation capacitances at 1 MHz C_g-V_g measurement are $\sim$ 13-14 Å prior to any quantum mechanical correction. From the bidirectional C_g-V_g sweeps, large hystereses of 155–300 mV together with kinks near the inversion regime for both p- and n-type Ge are observed. The kinks reduce with increasing measurement frequency implying that there exist some "slow" surface states near the conduction band (E_C) for the p-Ge case and the valence band (E_V) for n-Ge. Beyond that, these surface states could also help to explain the high gate leakage current in inversion for p-type Ge (substrate injection), giving the unusually symmetric leakage behavior for opposite gate polarities [inset in Fig. 1(a)] as compared with the other samples shown later. However, the inversion leakage current for n-Ge is supplied through gate injection, where the surface states near the dielectric-substrate interface do not have significant contribution.

For n-Ge samples that were treated with DI water in order to remove the native oxide, the resultant C_g-V_g characteristic

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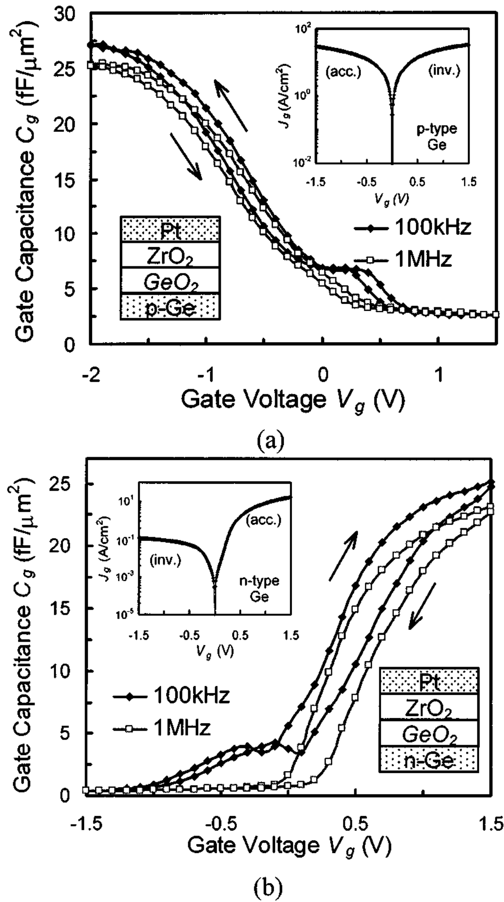

Fig. 1. Measured high-frequency C_g–V_g characteristics of the capacitor stacks with zirconium oxide on native oxide (Sample #1a and #1b). Insets show the corresponding J_g–V_g curve.

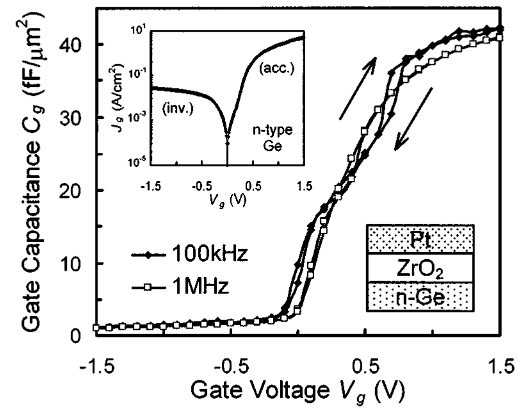

Fig. 2. Measured high-frequency C_g-V_g characteristics of the capacitor with zirconium oxide formed on DI water treated n-type Ge surface (Sample #2). The inset graph shows the measured J_g-V_g.

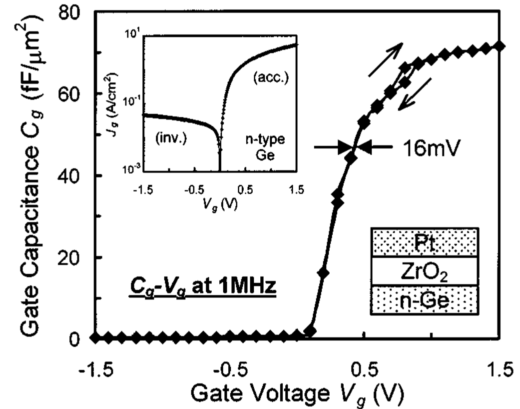

Fig. 3. Hysteresis estimation from bidirectional C_g–V_g measurement at 1 MHz on Sample #3. The inset graph shows the measured J_g–V_g.

for Sample #2 (Fig. 2) exhibits a drastic reduction in hysteresis and an EOT of about 8 Å. The accumulation leakage current density measured is 2.3 A/cm^2 at 1 V gate bias. However, the threshold voltage varies from device to device indicating either a nonuniform removal of the native oxide in the DI water rinse or nonuniform zirconia growth. In addition, the kink observed near the n-type Ge accumulation supports the previous hypothesis about the existence of surface states near E_C for p-Ge. However, those seen previously near E_V for n-Ge are now absent.

As an alternative to DI water exposure, HF vapor was applied to strip the native oxide (Sample #3). C_g-V_g measurements were performed at various frequencies ranging from 100 kHz to 1 MHz and the accumulation and inversion capacitances display minimal frequency dispersion. From Fig. 3, the hysteresis estimated from the bidirectional C_g-V_g measurement at 1 MHz is 16 mV. The measured EOT is ~ 5 Å before any quantum mechanical correction, which suggests that the native oxide interlayer was completely removed since the κ value for very thin GeO_2 is $\sim$ 3.0–3.8 [7]. Nonetheless, for these ultrathin gate dielectrics, a precise EOT extraction is difficult due to the inherently high gate leakage. Some C–V modeling and QM corrections have been attempted but none of them seem to be appropiate for Ge substrate. An alternative measurement could be made on the physical thickness of the dielectric stack and estimate the EOT using the approximate κ values. From the

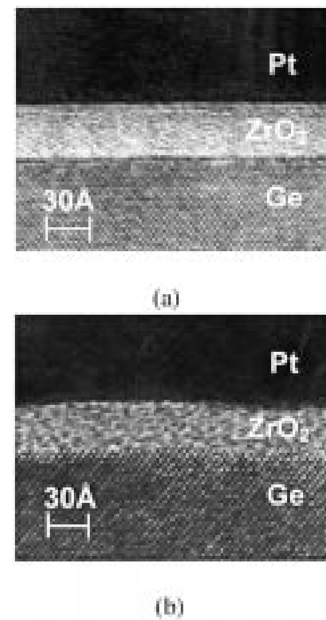

Fig. 4. High-resolution cross-sectional TEM image of (a) Sample #3 and (b) Sample #2.

cross-sectional high-resolution TEM (HRTEM) image shown in Fig. 4(a), the dielectric thickness is about 36 Å. Although

the HRTEM images in Fig. 4 are relatively insensitive to local composition variations, the uniform image contrast between the Ge substrate and Pt electrode suggests that the high-κ dielectric stack is free of any significant interfacial oxide layer between the high-κ film and Ge substrate. Compared with previous observations of well-defined polycrystallinity in zirconia on silicon dioxide [14], [15], the zirconia film grown directly on Ge has an amorphous or, at most, partially crystalline nature, which is currently under further investigation. Taking $\kappa \sim 25$ from the monoclinic phase of ZrO_2[16], the calculated EOT is 5.6 Å, consistent with our measured electrical results. At 1 V gate bias, a low leakage current density of 3.3 A/cm^2 is measured in accumulation.

The HRTEM image for Sample #2 is also shown in Fig. 4(b) for comparison. Even though the interface between the zirconia and the Ge substrate is relatively rougher than Sample #3, this dielectric stack appears to be interlayer-free as well. Together with the sub-nm EOTs and very low hysteresis C_g-V_g measured from both samples (#2 and #3), we could deduce that the absence of the GeO_2 interlayer improves the device performance substantially. The implication of the electrical data is that the best performance (in terms of EOT, interface states, and hysteresis) for high-κ on Ge can be obtained by simply eliminating the poor-quality and relatively unstable oxide interlayer and growing high-κ directly on Ge. Moreover, this oxide removal is readily achievable for high-κ on Ge.

Finally, device reliability and uniformity from Sample #3 have been evaluated. Upon constant-current stressing for 200 s with about 664 C/cm^2 of charge being injected from the substrate, only a small shift of 1.24 mV of flatband voltage is observed. Device-to-device variation across the die is almost negligible from electrical measurements and device yield is close to 100%.

IV. Conclusions

Excellent Ge MOS capacitors incorporating zirconia gate dielectric have been fabricated using a fairly low thermal budget process. Perhaps due to the relative thermodynamic instability of the inferior-quality native GeO_2, we have apparently avoided forming a low-κ interface layer in the high-κ gate stack. Around 5–8 Å EOT has thus been achieved with an extremely small C_g–V_g hysteresis, suggesting high-κ dielectrics for Ge MOS devices should be highly practical. This technology may allow fabrication of high performance MOSFETs needed in the sub-20 nm regime.

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