Atomic Layer Deposition of High-κ Dielectric for Germanium MOS Applications—Substrate Surface Preparation

Chi On Chui, *Student Member, IEEE*, Hyoungsub Kim, Paul C. McIntyre, and Krishna C. Saraswat, *Fellow, IEEE*

***Abstract*—In this letter, we present the use of atomic layer deposition (ALD) for high-κ gate dielectric formation in Ge MOS devices. Different Ge surface cleaning methods prior to high-κ ALD have been evaluated together with the effects on inserting a Ge oxynitride (GeO_xN_y) interlayer between the high-κ layer and the Ge substrate. By incorporating a thin GeO_xN_y interlayer, we have demonstrated excellent MOS capacitors with very small capacitance–voltage hysteresis and low gate leakage. Physical characterization has also been done to further investigate the quality of the oxynitride interlayer.**

***Index Terms*—Germanium, hafnium oxide, high-permittivity dielectric, MOS devices, surface cleaning, surface passivation.**

I. Introduction

THE SATURATION of Si MOSFET drain current $I_{\rm DS}$ upon dimension shrinkage may limit the prospect of future scaling. The lower effective mass and lower valley degeneracy of Ge [1] could alleviate the problem by providing a higher source injection velocity $v_{\rm inj}$ [2], which translates into higher drive current and smaller gate delay

$$I_{\rm DS} = W \times Q_{\rm inv} \times v_{\rm inj} \tag{1}$$

$$\frac{C_{\rm LOAD} V_{\rm DD}}{I_{\rm DS}} = \frac{L_{\rm gate} \times V_{\rm DD}}{(V_{\rm DD} - V_T) \times v_{\rm inj}} \tag{2}$$

where W is the channel width, $Q_{\rm inv}$ is the inversion charge, $C_{\rm LOAD}$ is the load capacitance, $V_{\rm DD}$ is the supply voltage, $L_{\rm gate}$ is the gate length, and V_T is the threshold voltage.

Nonetheless, the poor quality Ge native dielectrics for gate insulator and field isolation have been one of the classic problems that obstruct very large-scale integration (VLSI) CMOS device realization in Ge. In order to obtain a more stable native passivation layer either thermal or plasma anodic nitridation was applied to form Ge oxynitrides (GeO_xN_y) [3], [4], which were however not very scalable. Instead the use of high-κ dielectric directly [5], [6] or high-κ on oxynitride [7] on Ge has shown some promise. Among high-κ deposition techniques, ALD is particularly attractive in terms of precise thickness control and near-prefect conformality for ultrathin high-κ formation. Nonetheless, the uneven nucleation of ALD high-κ on nonhydroxylated surface (e.g., HF-last Si) could give poor electrical properties [8]. In this letter, we have investigated from a MOS capacitor perspective the effects of ALD high-κ deposition on both nonhydroxylated and hydroxylated Ge surfaces. Ge surface hydroxylation has been carried out using oxynitridation.

Manuscript received January 30, 2004. This work was supported in part by the Defense Advanced Research Projects Agency, in part by the Materials Structures and Devices Focus Center, in part by an Intel Foundation Ph.D. Fellowship, a Mayfield Stanford Graduate Fellowship, and an IBM Faculty Award. The review of this letter was arranged by B. Yu.

C. O. Chui and K. C. Saraswat are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: chion@stanford.edu).

H. Kim and P. C. McIntyre are with the Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305 USA.

Digital Object Identifier 10.1109/LED.2004.827285

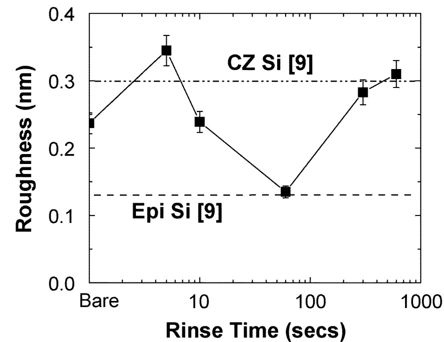

Fig. 1. Ge surface rms roughness as a function of DI water rinse time. The rms values from both epitaxial and Czochralski Si wafers were also included.

II. Experiments

Prior to the high-κ dielectric stack formation, two different Ge surface cleaning techniques were studied. The first method was deionized water rinsing (DIW) [5] to dissolve the soluble native oxide that was examined to be the dominant species on as-received Ge wafers by X-ray photoemission spectroscopy (XPS). To optimize the dwell time in DIW for minimum resultant surface roughness, atomic force microscopy (AFM) was used to track the root-mean-square (rms) values (Fig. 1). The initial peak in roughness (0–60 s) was due to partial and then complete removal of the soluble native oxide. Inferred from experience with Si [9]–[11], the dissociative adsorption of H_2O at room temperature on the Ge surface is believed to preferentially form a GeOH surface intermediate, which could lead to increased oxidation (and roughness) with increasing rinse time (>60 s). The second method was cyclic rinsing between 50:1 HF solution and DI water (CHF), originally developed by Deegan *et al.* [12] for effective surface oxide removal.

MOS capacitors were fabricated on (100) oriented Ge n-type and p-type substrates, with a net background doping concentration of $\sim 7 \times 10^{15}$ cm^{-3} and $\sim 3 \times 10^{17}$ cm^{-3}, respectively. In addition to the aforementioned cleaning, two types

0741-3106/04$20.00 © 2004 IEEE

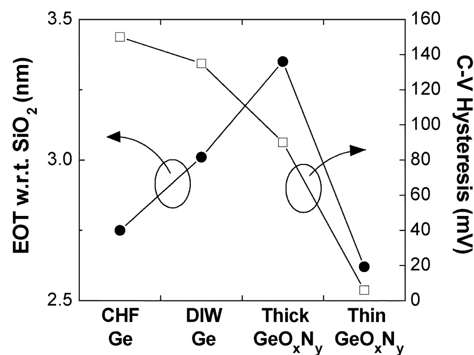

Fig. 2. Equivalent SiO_2 thickness (EOT) and hysteresis from bidirectional *C–V* sweep extracted (after series resistance correction [13] with 100- and 800-kHz data) from Pt gate Ge MOS capacitors with various surface preparations prior to high-κ dielectric deposition.

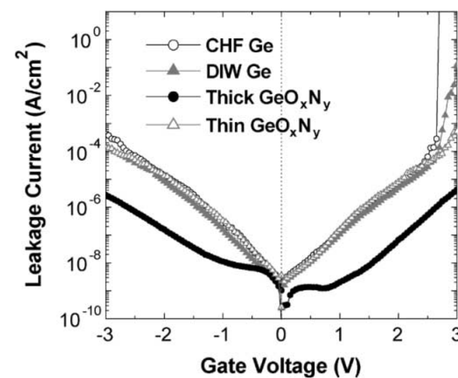

Fig. 3. Gate leakage current density as a function of voltage bias measured from Pt gate Ge MOS capacitors with different surface treatments prior to high-κ dielectric deposition. Data were taken from p-type Ge substrate.

of hydroxylated Ge oxynitride interlayer were investigated before the ALD high-κ deposition. The first oxynitride interlayer (thick GeO_xN_y) was formed by conventional furnace oxidation of CHF Ge at 500 °C for 2 min followed by rapid thermal nitridation (RTN) at 600 °C with 1-min soak time in NH_3 ambient. The second oxynitride interlayer (thin GeO_xN_y) was prepared by RTN of CHF Ge at 600 °C with 1 min soak time also in NH_3. The high-κ material, hafnium oxide (HfO_2) in this experiment, was deposited in a cold-wall high vacuum-base pressure ALD system at 300 °C, using alternating surface-saturating reactions of hafnium tetrachloride and H_2O precursors [6]. Various sizes of Pt gate electrode were formed by the room temperature e-beam evaporation through a shadow mask, and subsequently, Al was deposited on the wafer backside to reduce the sample contact (and series) resistance.

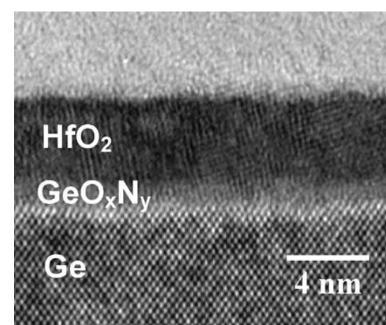

Fig. 4. High-resolution cross-sectional transmission electron microscopy (HR-XTEM) image of the optimum ALD HfO_2 on thin Ge oxynitride (GeO_xN_y) gate dielectric stack above the Ge substrate. The HfO_2 and GeO_xN_y thicknesses of this sample are about 45 and 11 Å, respectively.

III. Characterization and Discussion of Results

Multifrequency capacitance–voltage (*C–V*) characteristics were measured on the capacitors referred to as CHF Ge, DIW Ge, thick GeO_xN_y, and thin GeO_xN_y. Since the HfO_2 films on different samples were identically deposited at the same time with the same number of ALD cycles, the variation in deposition conditions should be minimized. Highlighted in Fig. 2 are the extracted capacitance-based accumulation equivalent SiO_2 thickness (EOT) and the corresponding *C–V* hysteresis estimated from bi-directional voltage sweep beginning at inversion. Among the four samples shown, the inclusion of a thicker Ge oxynitride interlayer intuitively produces a higher EOT value than a thinner one. For those without an interlayer, the CHF Ge offers a lower EOT compared to DIW Ge, indirectly suggesting that the combination of HF and DI water cleaning is more effective to remove Ge surface oxide than DI water alone. On the other hand, the *C–V* hysteresis obtained from different starting surface represents another scenario. The incorporation of an oxynitride interlayer delivers a reduction in the amount of charge trapping, and thus, hysteresis, versus ALD directly onto treated Ge substrates (CHF Ge and DIW Ge). The improvement may be attributed to the ease of uniform ALD on hydroxylated surfaces like SiO_2 or oxynitride passivation rather than on atomically clean Ge allowing locally epitaxial growth having a different microstructure [6].

Illustrated in Fig. 3 are the gate leakage current densities measured as a function of voltage bias. Under either gate or substrate injection, the gate leakages for all the samples were similarly low. The sample with a thick Ge oxynitride interlayer gave the lowest leakage which is expected because of its larger EOT. Compared to SiO_2 on Si in the same EOT range [14], the leakage current obtained from the high-κ Ge MOS capacitors demonstrated about 10^3 to 10^5 times reduction. Combining both the accumulation EOT, *C–V* hysteresis, and gate leakage data, we found that the optimum Ge MOS gate dielectric stack, for the processing methods investigated in this work, was composed of ALD HfO_2 on a thin GeO_xN_y interlayer exhibiting 26.2 Å of EOT, 6 mV of hysteresis, and 3.29×10^{-7} A/cm^2 of gate leakage at -1 V in accumulation. The high-resolution cross-sectional transmission electron microscopy (HR-XTEM) image of such a dielectric stack indicated the GeO_xN_y interlayer thickness was about 11 Å (Fig. 4). From XPS, the optimum GeO_xN_y layer was shown to contain about 22.5% of nitrogen.

Finally, the whole experiment was repeated on both p- and n-type Ge substrates to verify the reproducibility. Excellent *C–V* characteristics were obtained using the ALD HfO_2 and thin GeO_xN_y interlayer dielectric stack (Fig. 5). The difference in the extracted EOTs could not be attributed fundamentally to the opposite substrate types, but was instead due to variation in processes such as oxynitridation and ALD on different starting surfaces. In addition, minimum frequency dispersion was ob-

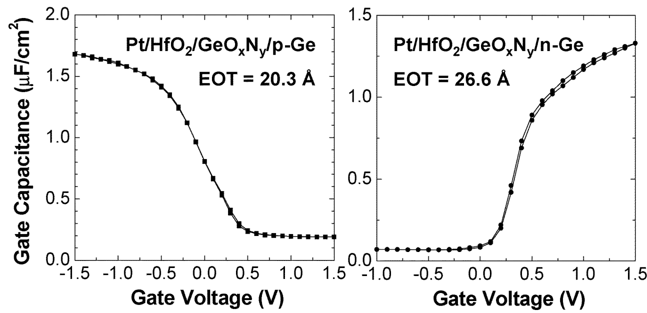

Fig. 5. Bidirectional gate *C–V* characteristics measured (at 800 kHz) from Pt gate MOS capacitors with HfO_2 on GeO_xN_y dielectric on both p- and n-type Ge substrates. Certain amount of interface states are still observable for p-Ge capacitors.

served in accumulation but the inversion capacitance (on n-type Ge only) increased slightly with decreasing measurement frequency that indicated the presence of some carrier generations near the surface.

IV. Conclusion

In conclusion, we have analyzed the effects of different Ge surface cleaning and the insertion of an oxynitride interlayer in Ge MOS capacitors with ALD high-κ dielectric. Very small *C–V* hysteresis and low gate leakage could be achieved. In order to offer a submicrometer EOT using this technology, the scaling of the thin hydroxylated GeO_xN_y interlayer has to be carefully studied.

Acknowledgment

The authors would thank Prof. B. B. Triplett for insightful discussions.

References

[1] S.-I. Takagi, "Re-examination of subband structure engineering in ultra-short channel MOSFETs under ballistic carrier transport," in *VLSI Symp. Tech. Dig.*, 2003, pp. 115–116.

[2] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, pp. 361–363, July 1997.

[3] O. J. Gregory, E. E. Crisman, L. Pruitt, D. J. Hymes, and J. J. Rosenberg, "Electrical characterization of some native insulators on germanium," in *Proc. Mater. Res. Soc. Symp.*, vol. 76, 1987, pp. 307–311.

[4] Z. Sun and C. Liu, "Plasma anodic oxidation and nitridation of Ge(111) surface," *Semicond. Sci. Technol.*, vol. 8, pp. 1779–1782, 1993.

[5] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS capacitors incorporating ultrathin high-k gate dielectric," *IEEE Electron Device Lett.*, vol. 23, pp. 473–475, Aug. 2002.

[6] H. Kim, C. O. Chui, K. C. Saraswat, and P. C. McIntyre, "Local epitaxial growth of ZrO_2 on Ge (100) substrates by atomic layer epitaxy," *Appl. Phys. Lett.*, vol. 83, pp. 2647–2649, 2003.

[7] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO_2 gate dielectrics and TaN gate electrode," in *VLSI Symp. Tech. Dig.*, 2003, pp. 121–122.

[8] M. Copel, M. Gribelyuk, and E. Gusev, "Structure and stability of ultra-thin zirconium oxide layers on Si(001)," *Appl. Phys. Lett.*, vol. 76, pp. 436–438, 2000.

[9] B. B. Triplett, "The limitation of extrinsic defect density on thin gate oxide scaling in VLSI devices," in *Silicon Symposium VII, Electrochemical Society*, 1994.

[10] S. Rajagopalan, U. Mitra, S. Pan, K. Gupta, C. M. Lin, G. Sery, S. Mittal, K. Hasserjian, W. J. Lo, and G. Neubauer, "Reaction of DI water and silicon and its effect on gate oxide integrity," in *Proc. IEEE IRPS* , 1993, pp. 28–31.

[11] A. T. S. Wee, C. H. A. Huan, P. S. P. Thong, and K. L. Tan, "A comparative study of the initial oxygen and water reactions on germanium and silicon using SIMS," *Corros. Eng.*, vol. 36, pp. 9–22, 1994.

[12] T. Deegan and G. Hughes, "An X-ray photoelectron spectroscopy study of the HF etching of native oxides on Ge (111) and Ge (100) surfaces," *Appl. Surf. Sci.*, vol. 123–124, pp. 66–70, 1998.

[13] K. J. Yang and C. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Trans. Electron Devices*, vol. 46, pp. 1500–1501, Oct. 1999.

[14] S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Lett.*, vol. 18, pp. 209–211, Apr. 1997.