

# A Sub-400°C Germanium MOSFET Technology with High- $\kappa$ Dielectric and Metal Gate

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## Abstract

A novel low thermal budget ( $\leq 400^\circ\text{C}$ ) germanium MOS process with high- $\kappa$  gate dielectric and metal gate electrode has been demonstrated. For the first time, self-aligned surface-channel Ge  $p$ -MOSFETs with  $\text{ZrO}_2$  gate dielectric having equivalent oxide thickness (EOT) of 6-10 Å and platinum gate electrode are demonstrated with twice the low-field hole mobility of Si MOSFETs.

## Introduction

A fundamental scaling limit, the maximum saturated drain current ( $I_{Dsat}$ ), for Si MOSFETs is set by the thermal injection of carriers from the source into the channel [1]. This can be overcome by incorporating a more efficient carrier injecting material like Ge, which has a higher low-field carrier mobility [2] and smaller mobility bandgap for supply voltage ( $V_{DD}$ ) scaling. In addition, the smaller optical bandgap for Ge [3] broadens the absorption wavelength spectrum allowing opto-electronic integration to enhance CMOS functionality. Unlike Si, however, the lack of a stable native oxide hinders the passivation of Ge surfaces. Recently we demonstrated MOS capacitors on Ge with  $\text{ZrO}_2$  gate dielectric [4]. In this work we present for the first time Ge MOSFETs with  $\text{ZrO}_2$  gate dielectric and platinum gate electrode. Integration of Ge with high- $\kappa$  dielectric and metal gate promises higher  $I_{on}$ , higher  $C_{gate}$  (Fig. 1), and no carrier depletion commonly encountered in poly-Si gates. As an initial attempt,  $p$ -MOSFETs were built, as they usually limit the speed of a CMOS circuit. Owing to low-temperature dopant activation in Ge [5] and the room temperature  $\text{ZrO}_2$  growth process [6], the peak temperature in the entire fabrication process was  $400^\circ\text{C}$ , significantly less than that required for Si devices.

## Device Design and Process Development

### A. Device Design

To simplify the process for demonstration purposes, self-isolated ring transistor structures (Fig. 2) were employed. Device operation is the same as a conventional rectangular MOSFET; however, the definition of the channel width is not straightforward. By applying the Square-Law Theory on a long-channel ring MOSFET (Fig. 3), the effective channel width,  $W_{eff}$ , could be extracted. Devices with drawn gate length ( $L_{drawn}$ ) of 2-200  $\mu\text{m}$  were designed.

### B. Process Development

Two key steps in developing the process were gate stack and source/drain junction formation.

The idea of passivating the Ge surface with high- $\kappa$  dielectric was first investigated through extensive experiments using MOS capacitor test structures. Different high- $\kappa$  materials, deposition techniques, and Ge surface cleaning strategies were attempted; electrical and physical characterizations were done by C-V measurements and transmission electron microscopy (TEM), respectively, on MOS capacitor structures. One gate dielectric candidate was formed (Fig. 4) by UHV sputtering of  $\sim 20$ -30 Å Zr films on the Ge surface followed by *in-situ* UV ozone oxidation at room temperature [6]. Pt gate electrode was formed by the liftoff process. The Ge/ $\text{ZrO}_2$  interface (Fig. 5) formed by UV-ozone processing [4, 6] was found to produce excellent C-V characteristics (Fig. 6). However, gate leakage prevents a precise extraction of the interface state density and EOT from the raw C-V data. Alternately, a combination of the electrical characteristics and the physical dielectric thickness was used for EOT extraction. EOT was estimated to be in the range of 6-10 Å [4] without any quantum mechanical correction.

To study  $p$ -type dopant implantation and activation in Ge,  $\text{BF}_2^+$  at 35 keV energy and  $4 \times 10^{15} \text{ cm}^{-2}$  dose was implanted in a lightly Sb-doped ( $\sim 10^{16} \text{ cm}^{-3}$ ) Ge substrate which was capped with LPCVD  $\text{SiO}_2$  deposited at  $300^\circ\text{C}$ . Activation anneals were then performed at various temperatures in  $\text{N}_2$  ambient. Hall measurements showed a huge reduction in sheet resistance and increase in activated dopant on raising the anneal temperature from  $325^\circ\text{C}$  to  $400^\circ\text{C}$  (Fig. 7). Annealing at higher temperatures does not show significant change, consistent with the results of Gusev *et al.* [5]. Fig. 8 shows the activated B profile measured by a spreading resistance probe.

### Transistor Fabrication

The sub- $400^\circ\text{C}$  Ge transistor process flow is summarized in Fig. 9. The starting substrates were (100) oriented,  $n$ -type ( $\sim 10^{16} \text{ cm}^{-3}$ ) Ge wafers. Either DI water rinse or HF vapor etch was used in an attempt to remove native oxides, followed by  $\sim 35$ -50 Å  $\text{ZrO}_2$  deposition. No threshold adjustment implant was used. After Pt gate electrode formation the self-aligned source/drain  $\text{BF}_2^+$  implant was done. Dopant activation was performed at  $400^\circ\text{C}$  in  $\text{N}_2$  for 30 mins. Source/drain contact holes etching of  $\text{ZrO}_2$  and contact metallization were

combined into a single lithography step.  $ZrO_2$  was first etched in chlorine plasma. Keeping the same photoresist masking, a Ti/Al metal stack was e-beam evaporated followed by the liftoff process. Finally, the samples were subjected to forming gas anneal at 300°C for 30 mins. Fig. 10 shows the HR-TEM taken from a fully processed Ge MOSFET. No degradation of the gate stack can be seen.

### Results and Discussion

Ge  $p$ -MOSFETs with  $L_{drawn}$  from 2-200  $\mu\text{m}$  were all working. The measured 2  $\mu\text{m}$  gate length transistor output characteristics are illustrated in Fig. 11. The device exhibited reasonable turn-on behavior and a relatively high on current of  $\sim 100 \mu\text{A}/\mu\text{m}$  at 1 V gate overdrive and 2 V drain voltage. On reducing the gate overdrive close to zero, the transistor characteristics started to be influenced by the gate leakage. At zero gate overdrive, the drain current and gate leakage were of the same order of magnitude due the relatively large gate electrode area for the *ultrathin* high- $\kappa$  gate dielectric and the un-optimized threshold voltage ( $V_t$ ). A much better turn-off would be expected for a properly scaled device, i.e. a thicker gate dielectric in a long channel length device or a sub-micron channel length device with the correct  $V_t$ .

The effective carrier mobility was extracted [7] by measuring the gate oxide capacitance in inversion ( $C_{ox}$ ), and  $I_D$  in the linear region, as shown in Fig. 12. Usually, the mobility data extracted should not depend strongly on the transistor channel length. However, the  $C_{ox}$  obtained was less reliable for very long channel length,  $L_{drawn} = 100 \mu\text{m}$ , devices (with large gate electrode) due to the relatively larger frequency dispersion, and for very short channel length,  $L_{drawn} = 2 \mu\text{m}$ , devices because of the inevitably large fraction of fringing capacitance measured together in this simple and un-optimized device structure (Fig. 2). The 25  $\mu\text{m}$  Ge MOSFET was therefore chosen to be studied for mobility with the C-V characteristics shown in Fig. 13. The inversion capacitance was much less influenced by the gate leakage and was considered reliable for mobility calculations.

To further minimize errors introduced by the gate leakage to the pure source-to-drain channel current ( $I_{DS}$ ) measurements for accurate mobility extraction, the transistors were operated at gate and drain biases where the gate leakage is negligibly small ( $< 1\%$ ) compared to either  $I_D$  or  $I_S$ , while ensuring linear regime device operation. Effective mobility as a function of effective E-field is extracted from the 25  $\mu\text{m}$  gate length and 35 Å  $ZrO_2$  film MOSFETs is shown in Fig. 14. For comparison data for a conventional Si  $p$ -MOSFET is also shown. At low effective E-field, the Ge transistors with high- $\kappa$   $ZrO_2$  dielectric demonstrated roughly 2-fold enhancement of the effective hole mobility compared to the universal mobility model for Si MOSFETs with  $SiO_2$  [8]; the peak effective mobility was 313  $\text{cm}^2/\text{V}\cdot\text{s}$ . Taking into account the inherent mobility degradation with the *ultrathin* gate dielectric in place, the above mobility values show the promise of employing surface Ge channel devices. With proper optimization of the

device structure and the fabrication process it should be possible to obtain even higher values of the mobility and lower leakage. Possible sources of reduction in the measured current, which is reflected in the extracted mobility, include the current crowding effect at the drain for this ring MOSFET structure and the large series resistance at the source/drain contacts (Fig. 2). In addition, the Ge surface damage caused by the Zr sputtering during high- $\kappa$  formation [6] would enhance carrier scattering and hence lower the mobility.

It should be noted that, in this short-flow process, no other optimization such as LDD implant, spacer formation etc. was employed, as our goal was to demonstrate the feasibility of Ge MOSFETs with *ultrathin* high- $\kappa$  gate dielectric and metal gate electrode.

### Conclusions

Ge PMOSFETs with *ultrathin* high- $\kappa$  dielectric and metal gate have been fabricated using a low thermal budget process (400°C), demonstrating a low-field mobility twice that of Si MOSFETs. With more development, this novel technology should allow the fabrication of high performance deep sub-micron Ge MOSFETs.

### Acknowledgements

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$$I_{channel} \propto \text{charge} \times \text{source injection velocity}$$

$$\propto (\text{gate oxide cap} \times \text{gate overdrive}) \times v_{inj}$$

$$\propto C_{ox} (V_{GS} - V_T) \times E_{source} \times \mu_{inj}$$

- High-κ Gate Dielectrics
- Metal Gate Electrode

- Materials with Higher Low-Field Mobility e.g. Ge

Figure 1. Material requirements for enhancing transistor performance.

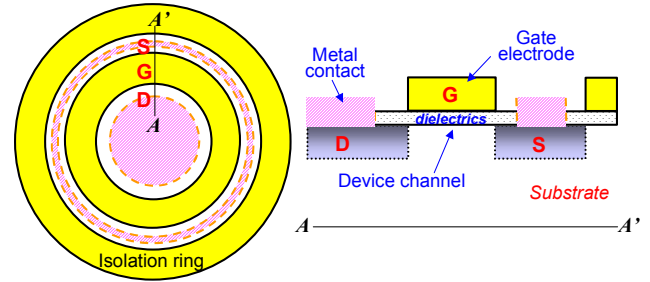
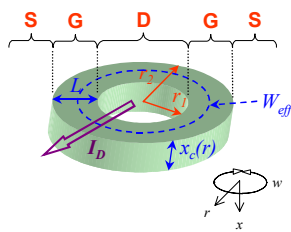


Figure 2. The top-view of the ring MOSFET structure (left) and the cross-sectional view of AA' (right). Self-isolation is achieved by tying the source ring potential to ground. Additional isolation could be obtained by using the isolation ring for some device operations.

The conduction volume in a long-channel ring MOSFET (linear region):



From the Square-Law Theory (integrate the radial carrier flux):

$$J_N \equiv J_{Nr} \equiv q\mu_n n E_r = -q\mu_n n \frac{d\phi}{dr}$$

$$I_D = -\iint J_{Nr} dx dw = -(2\pi r) \bar{\mu}_n Q_N \frac{d\phi}{dr}$$

$$I_D = -\left[ \frac{\bar{\mu}_n C_{ox}}{2\pi \ln\left(\frac{r_2}{r_1}\right)} \right] \left[ (V_G - V_T) V_D - \frac{V_D^2}{2} \right]$$

$$\Rightarrow W_{eff} = \frac{2\pi L}{\ln(r_2/r_1)} = \frac{2\pi(r_2 - r_1)}{\ln(r_2/r_1)}$$

Figure 3. Effective channel width extraction by applying the conventional Square-Law Theory on a long-channel device.

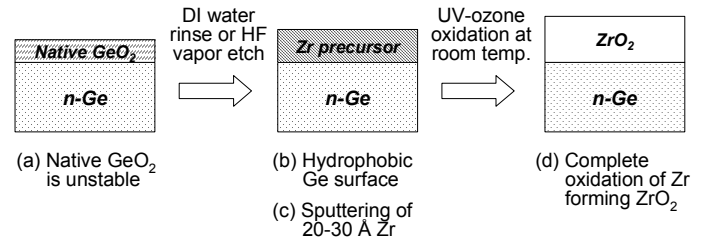


Figure 4. Illustration of the room temperature ZrO<sub>2</sub> deposition by the UV-assisted ozone oxidation of sputtered Zr precursor films [4].

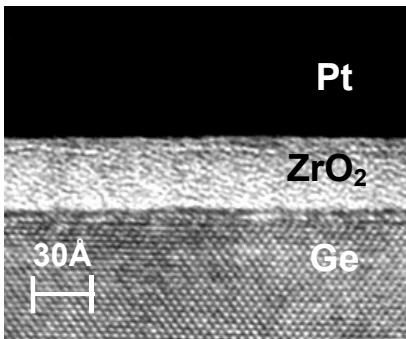


Figure 5. High-resolution transmission electron microscope (HR-TEM) image of the Pt/ZrO<sub>2</sub>/Ge capacitor stack [4].

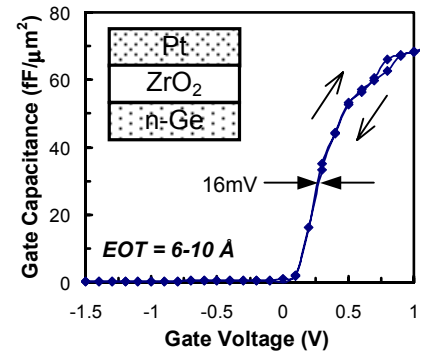


Figure 6. Bi-directional C-V measurement at 400 kHz for hysteresis estimation [4].

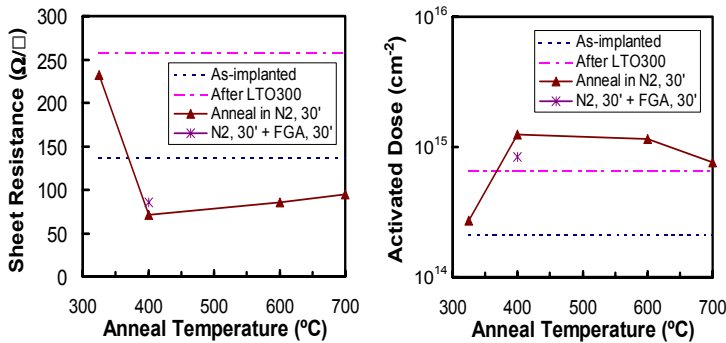


Figure 7. Hall measurement results show the reduction in sheet resistance ( $R_{sheet}$ ) and the increase in activated dose saturate at around 400°C. The initial  $R_{sheet}$  increase, after LTO deposition, from the as-implanted case was probably caused by the dopant out-diffusion at 300°C before activation.

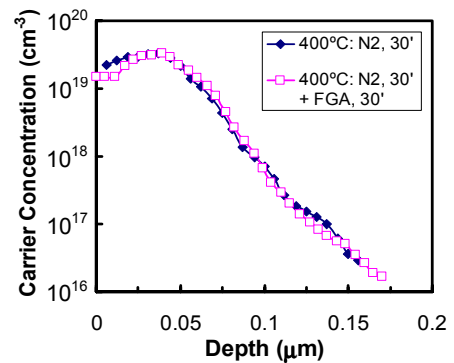


Figure 8. Spreading Resistance Probe (SRP) data measured from the surface of the samples. No appreciable diffusion observed after an additional FGA on an anneal-activated (N<sub>2</sub> at 400°C) sample.

- 1) 4", (100),  $\sim 10^{16} \text{ cm}^{-3}$  Sb-doped Ge wafers
- 2) DI water rinse or HF vapor etch
- 3)  $\sim 35\text{-}50 \text{ \AA}$   $\text{ZrO}_2$  deposition at room temperature
- 4) Lithography for metal gate liftoff
- 5)  $\sim 500 \text{ \AA}$  Pt e-beam evaporation
- 6) Pt liftoff
- 7) Self-aligned S/D implant ( $\text{BF}_2^+$ , 35 keV,  $4 \times 10^{15} \text{ cm}^{-2}$ )
- 8) Dopant activation in  $\text{N}_2$  at  $400^\circ\text{C}$  for 30 mins
- 9) Lithography for contact hole ( $\text{ZrO}_2$ ) etch and contact metallization by liftoff
- 10)  $\text{ZrO}_2$  etch in chlorine plasma
- 11)  $\sim 750 \text{ \AA}$  Ti/ $\sim 1000 \text{ \AA}$  Al e-beam evaporation
- 12) Ti-Al metal stack liftoff
- 13) FGA at  $300^\circ\text{C}$  for 30 mins

Figure 9. Synopsis of the sub- $400^\circ\text{C}$  Ge transistor process flow.

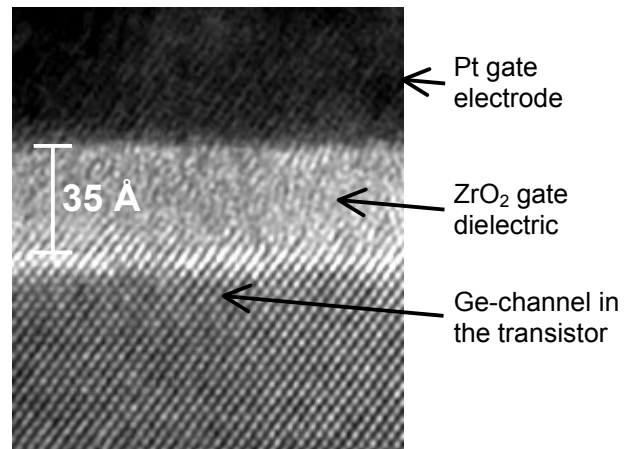


Figure 10. HR-TEM image taken from a fully processed Ge transistor.

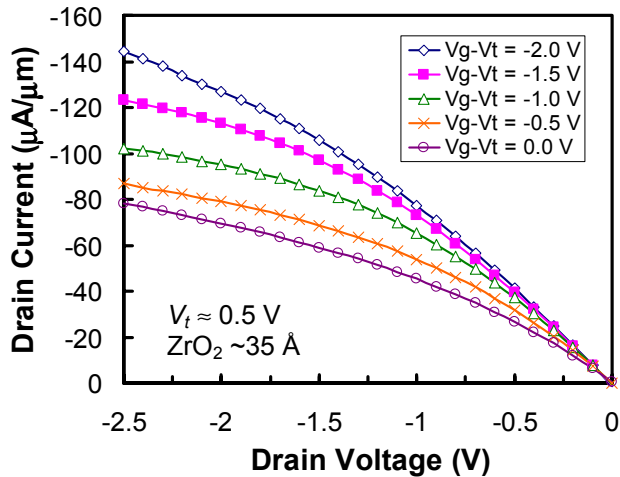


Figure 11. Output characteristics of a  $2 \mu\text{m}$  gate length Ge transistor. ( $W_{\text{eff}} = 320.4 \mu\text{m}$ ). The device is not turning off well due to gate leakage and the un-optimized  $V_t$ .

Linear regime drain current:

$$I_D = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} (V_{\text{GS}} - V_T) V_{\text{DS}}$$

$$\Rightarrow \mu_{\text{eff}} = \frac{I_D}{(W/L) C_{\text{ox}} (V_{\text{GS}} - V_T) V_{\text{DS}}}$$

$$E_{\text{eff}} = \frac{Q_{\text{dep}} + \eta Q_{\text{inv}}}{\epsilon_s} = \frac{E_{\text{ox}} \epsilon_{\text{ox}} - (1-\eta) Q_{\text{inv}}}{\epsilon_s}$$

For  $V_{\text{GS}} \gg V_{\text{DS}}$ :

$$Q_{\text{inv}} \approx C_{\text{ox}} (V_{\text{GS}} - V_T) \ \& \ E_{\text{ox}} \approx V_{\text{GS}} / t_{\text{ox}}$$

$$\Rightarrow E_{\text{eff}} \approx \frac{C_{\text{ox}} [V_{\text{GS}} / \epsilon_0 - (1-\eta)(V_{\text{GS}} - V_T)]}{\epsilon_s}$$

$Q_{\text{dep}}$  : Bulk depletion charge

$Q_{\text{inv}}$  : Inversion layer charge

$\eta$  : Fitting parameter  
1/2 for electrons & 1/3 for holes

Figure 12. Effective channel mobility extraction from the linear regime transistor current [7].

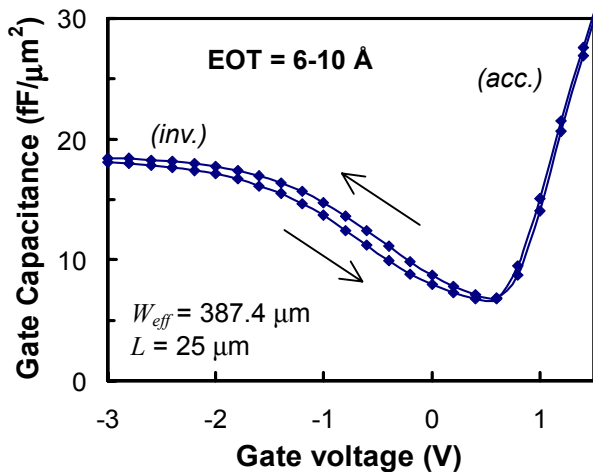


Figure 13. C-V measurement (400 kHz) collected from a  $25 \mu\text{m}$  Ge transistor. Due to the high gate leakage in accumulation [4], the MOSFET C-V does not saturate, but the inversion C-V does.

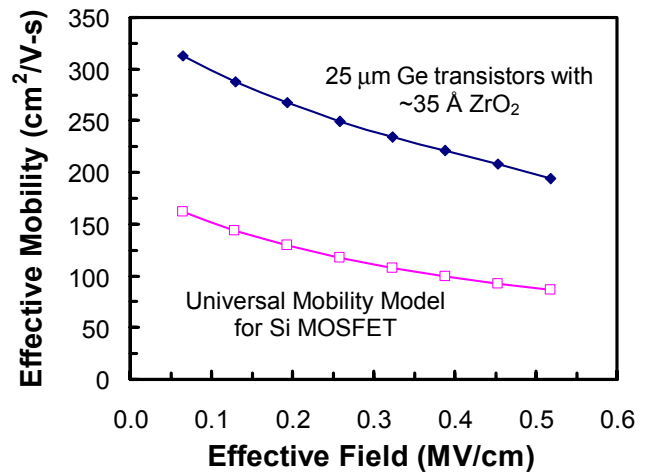


Figure 14. Effective mobility vs. effective E-field for the  $25 \mu\text{m}$  Ge transistors with  $\sim 35 \text{ \AA}$   $\text{ZrO}_2$  and the universal mobility model for Si MOSFET [8].