A Novel Self-aligned Gate-last MOSFET Process Comparing High-κ Candidates

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The high-κ dielectrics ZrO_2 and HfO_2 have been researched in the last 15 years to replace SiO_2 to suppress leakage upon scaling [1]. However, no systematic physical and electrical comparison of the behavior of these two metal oxide dielectrics has been reported. In this work we compare these two dielectrics deposited in the same chamber with the same technique using a newly developed self-aligned gate-last MOSFET process, that is much less-involved than processes like replacement or damascene gate [2].

The high-κ materials were formed by atomic layer deposition (ALD) at 300°C [3]. The κ-values of 29 (for ZrO_2) and 17 (for HfO_2) were extracted by measuring the EOT from a series of MOSCAPs with different physical thickness (Fig. 1). When the gate leakage densities are plotted against EOT (Fig. 2), ZrO_2 displays a lower leakage than HfO_2 at the same EOT, consistent with its higher κ-value. As-deposited ZrO_2 was polycrystalline in the tetragonal phase while HfO_2 was amorphous (no long-range order); both films had excellent surface roughness.

The novel self-aligned gate-last process is summarized in Fig. 3. Since only *n*-MOSFETs were fabricated to verify the process, *p*-Si substrates (5×10^{16} cm^{-3}) were used. After standard field isolation and active area opening, 8 wt% phospho-silicate glass (PSG) was then deposited followed by LPCVD SiO_2 (LTO) capping (Fig. 3(a)). The source/drain regions were defined by etching the LTO/PSG above the channel position (Fig. 3(b)). To prevent auto-doping from the PSG sidewall, a chemical SiO_2 was formed on the channel surface prior to source/drain formation by solid source diffusion (SSD) using rapid thermal anneal (RTA). Resulting junction depth profiles are shown in Fig. 4. Numerous SSD tests were launched to optimize both peak concentration and junction depth (Fig. 5). RTA at 1100°C for 10 secs from 8 wt% PSG was chosen. 15 Å of SiO_2 was then grown on the channel surface followed by ALD of about 35~45 Å of ZrO_2 or HfO_2 (Fig. 3(c)). Pt gate electrodes overlapping the source/drain were formed by photoresist liftoff followed by LTO back-end isolation, contact hole etching, and metallization using 1% Si-doped Al (Fig. 3(d)). All the samples were subjected to forming gas anneal at 400°C for 45 min. SiO_2 of about the same EOT as high-κ using Al gate electrode was included as a control. This simple implantation-less process consists of only 5-lithography levels.

Transfer characteristics of both an Al gate SiO_2 control device and Pt gate ZrO_2 and HfO_2 *n*-MOSFETs of the same size are exhibited in Fig. 6. The EOTs extracted from these devices are 21.9 Å, 20.6 Å, and 23.3 Å respectively. For similar EOT, the SiO_2 device off-current was mainly gate leakage while that for ZrO_2 and HfO_2 was source/drain leakage, for these bulk devices without intentional short-channel effect (SCE) suppression. Since the amount of transistor drive current is the ultimate concern from a circuit perspective, MOSFET output characteristics of these three dielectrics should be compared (Fig. 7). With the same amount of gate (standby) leakage estimated from the corresponding EOTs (from Fig. 2), both ZrO_2 and HfO_2 devices delivered about the same amount of drive current (Fig.7), even though the mobility estimated from ZrO_2 and HfO_2 devices were about 59% and 72% respectively compared to the SiO_2 control device. To conclude, these results suggested that using either ZrO_2 or HfO_2 would provide similar on-to-off current ratio at a given device size.

[1] Wilk *et al*., *J. Appl. Phys.*, vol. 89, p. 5243, 2001. [2] Tavel *et al*., *IEDM Tech. Dig*., p. 429, 2002.
[3] Kim *et al., Appl. Phys. Lett*., vol. 82, p. 106, 2003. [4] Timp *et al*., *IEDM Tech. Dig*., p. 615, 1998.

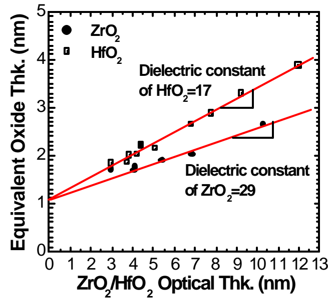

Figure 1. EOT vs. physical thickness of ZrO_2 and HfO_2. Pt gate MOSCAPs were used for extraction.

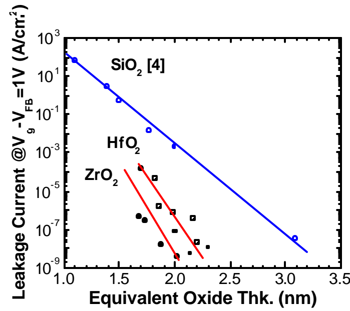

Figure 2. MOSCAP gate leakage density vs. EOT for ZrO_2, HfO_2, and thin SiO_2 [4].

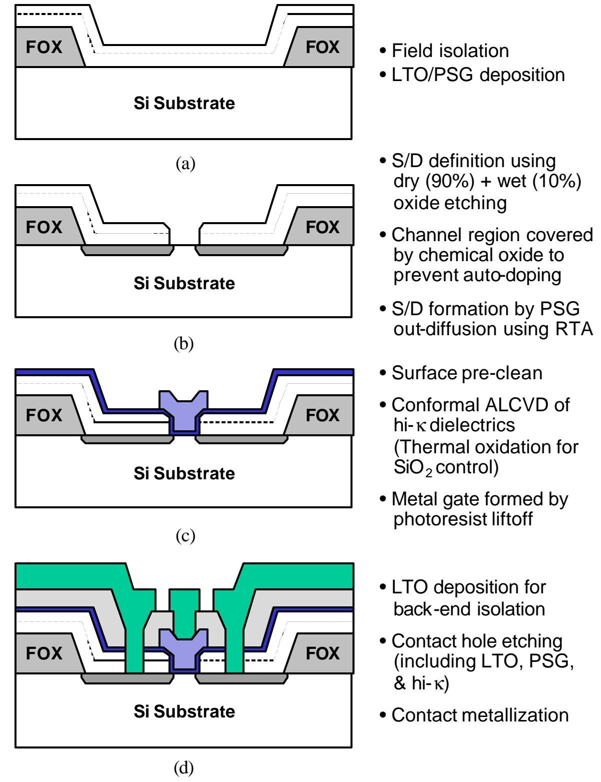

Figure 3. The novel self-aligned gate-last MOSFET process flow.

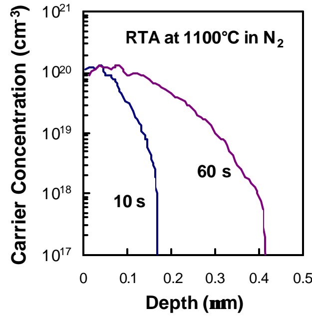

Figure 4. Spreading Resistance Probe (SRP) profiles of phosphorus SSD from 8 wt% PSG driven by RTA.

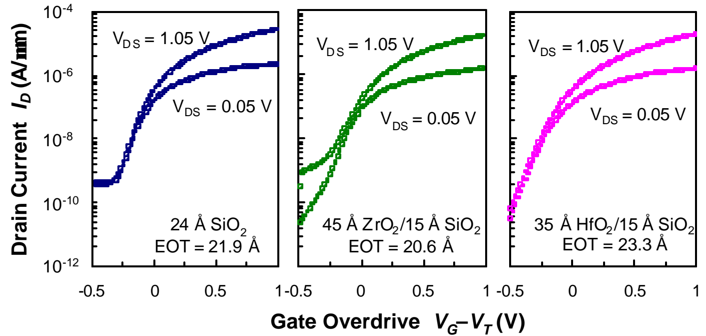

Figure 6. Drain current vs. gate overdrive for three dielectrics. Data were measured from Pt gate n-MOSFETs with W/L = 100/1.5 µm/µm.

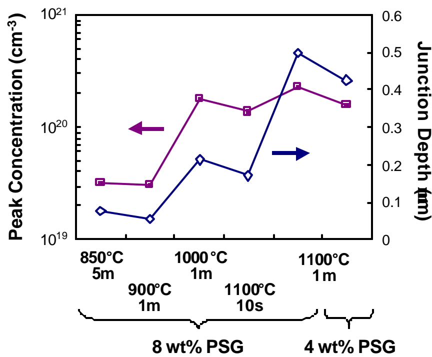

Figure 5. Peak electrical active concentrations and junction depths obtained by SSD from 8 wt% PSG under different anneal budgets.

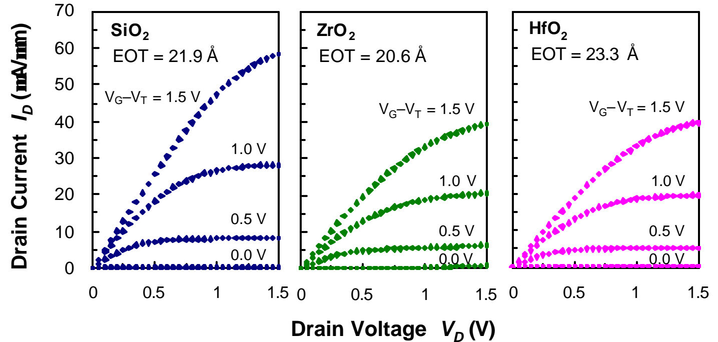

Figure 7. Drain current vs. drain voltage for three dielectrics. Data were measured from Pt gate n-MOSFETs with W/L = 100/1.5 µm/µm.