

the benefit of the high-k material, but at the same time seems to have a positive effect on the mobility. In addition, we have observed, for example by TEM, that interactions occur between the HfO₂ and the polySi gate electrode at the top interface. Furthermore, we have determined, based on a thickness series, the k-value for HfO₂ deposited at various temperatures and found that the k-value of the HfO₂ depends upon the gate electrode deposited on top (polySi or TiN). We propose a hypothesis to explain this dependency and discuss the impact on EOT scalability. Finally, we demonstrate that also the thermal stability of the gate stack forms a potential problem for scaling EOT values.

4:00 PM D2.8

SCALING LIMITS OF ATOMIC LAYER DEPOSITED HfO₂ GATE DIELECTRICS. M.L. Green and G.D. Wilk, Agere Systems, Berkeley Heights, NJ; M.-Y. Ho, National University of Singapore, SINGAPORE; B. Busch, Micron, Boise, ID; T. Sorsch, Lucent Technologies, Murray Hill, NJ.

The international semiconductor roadmap calls for gate dielectrics with equivalent oxide thickness (EOT) < 1.0 nm by about 2007. Therefore, it is important to understand to what extent one of the most promising high-k candidate materials, HfO₂, can be scaled. In this capacitor study, the parameters studied were HfO₂ layer thickness (3 - 6 nm), type of underlayer (SiO₂, Si-O-N or Si-O-H (chemical oxide)), and post-deposition anneal (PDA) temperature (600 - 1000°C), time (spike anneal - 600 seconds), and ambient (N₂, O₂ or NO). Chemical oxide underlayers were favored in this study, as they gave rise to the smoothest, most two-dimensional films. Using them leads to the thinnest "sealed" (i.e., pinhole-free) films. These results were compared to HfO₂ growth on thermal oxide or oxynitride underlayers. Electrical measurements reported in this study are EOT, leakage current and ΔV_{fb} . Regardless of the PDA ambient, high temperature anneals (>700°C) are required to lower ΔV_{fb} , as is some interfacial regrowth. For 3 nm HfO₂ layers, the thinnest practical from a growth and gate current leakage standpoint, even if the PDA resulted in no regrowth at the interface, the minimum achievable EOT would be about 1.2 nm. Therefore, to achieve sub-nanometer EOT gates with HfO₂, the intentionally grown underlayers should be eliminated. Schemes for accomplishing this, while achieving satisfactory growth morphology, will be discussed. The alternative is to identify suitable high-k films with dielectric constants greater than that of HfO₂ (18-20).

4:15 PM D2.9

ENHANCEMENT OF THE THERMAL STABILITY OF HF-SILICATES WITH NITROGEN INCORPORATION AND ITS INFLUENCE ON THE ELECTRICAL PROPERTIES.

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Hf-silicate is one of the prospective materials for the first high-k gate dielectrics applied to real LSIs due to its modest dielectric constant and relatively good interface properties with silicon substrate. However, the major drawback of this material has been its poor thermal stability. Experiments with Hf-silicate, sputter-deposited on Si substrate have clearly revealed that the phase separation from the uniform silicate structure to HfO₂ and the remaining matrix during high-temperature annealing, which is required in the conventional CMOS process, resulted in the reduction of the average dielectric constant of the film. It could lead to significant degradation in the speed of CMOS circuits. To enhance the thermal stability, nitrogen was incorporated in Hf-silicate by adding N₂ in the ambient of the sputtering system. The result indicated that the nitrogen as well as hafnium in the material could increase the dielectric constant of the material. Moreover, nitrogen can retain its high dielectric constant by suppressing the phase separation phenomenon. Poly-Si/Hf-silicate/p-Si capacitors with the same physical dielectric thickness revealed that the equivalent oxide thickness decreased as the nitrogen concentration increased, while the reduction in leakage current relative to that of SiO₂ remained almost the same. The dependence of other electrical parameters such as fixed charge and charge trapping on the nitrogen concentration will be also discussed at the presentation.

4:30 PM D2.10

PHYSICAL-CHEMICAL EVOLUTION OF HF-ALUMINATES UPON THERMAL TREATMENTS. Barbara Crivelli, Mauro Alessandri, Stefano Alberici, Daniela Brazzelli, Alice Camille Elbaz, Gabriella Ghidini, Giuseppe Pavia, STMicroelectronics, Agrate Brianza, ITALY; Jan Willem Maes, ASMI, Leuven, BELGIUM; Giampiero Ottaviani, University of Modena, Department of Physics and Unitai INFN, Modena, ITALY; Claudia Wiemer, Laboratorio MDM-INFN, Agrate Brianza, ITALY.

The continuous scaling down of transistor and memory devices toward 65 nm technology node demands for the replacing of ultra thin SiO₂ based dielectrics with high-k materials. In this study, the investigation of physical-chemical stability of Al₂O₃-HfO₂ alloys upon prolonged post-deposition annealings (PDA) is presented. Two different Hf-aluminates were analyzed, containing 35% and 75% Al₂O₃ mol% respectively. Amorphous films were deposited on RCA treated p-type silicon by ALCVDTM. Post-deposition annealings were carried out in O₂ or N₂ atmosphere, at 850°C and 900°C for 30 minutes. Interfacial layer (IL) increase after PDA was detected on all the samples. No impact of annealing temperature was observed on Al-rich alloy, while sensible effect was noticed on Hf-rich material. N₂ and O₂ annealings resulted in limited IL differences, suggesting that these films were not completely permeable to oxygen diffusion. XRD and planar TEM-ESI analysis evidenced first phase separation and then, in the case of Hf-rich samples, crystallization phenomena occurring at HfO₂ cluster sites. Differently from HfO₂, this alloy crystallized mainly in tetragonal phase with some specific features depending on annealing ambient. Stack composition was characterized by means of TOF-SIMS, XRR, EELS, standard and microprobe XRF. Growth of interface layer was justified by limited oxygen incorporation from external ambient. Silicon diffusion from the substrate into high-k material and aluminium/hafnium redistribution were observed and associated to annealing temperature. Finally, Hf-aluminates were electrically characterized by means of C-V and I-V measurements on basic capacitors. Variations in material electrical properties were found consistent with change in physical-chemical film structure. Overall, Hf-aluminates were found to remain amorphous during high temperature prolonged treatments up to 900°C for 75% and 850°C for 35% alloys respectively. Oxygen, silicon and metals inter-diffusion was observed at these conditions, but with no relevant physical differences and lower impact on electrical properties compared to Al₂O₃ and HfO₂.

4:45 PM D2.11

ATOMIC LAYER DEPOSITION OF ZrO₂ ON Si AND Ge SUBSTRATE. Hyoungsub Kim, Paul C. McIntyre, Stanford Univ., Dept of Materials Science & Engineering, Stanford, CA; Chi-On Chui, Krishna Saraswat, Stanford Univ., Dept of Electrical Engineering, Stanford, CA.

As the continued scaling of Si CMOS devices approaches its fundamental limits, alternative semiconductor materials, such as Ge, with high intrinsic carrier mobility are increasingly promising for use in the channel region of field effect transistors. However, in the case of a Ge substrate, the lack of a sufficiently stable native oxide (GeO_x) can hinder the formation of a good quality gate dielectric. Recently, deposited high-k dielectric materials prepared on Si by methods such as ALD (Atomic Layer Deposition) have demonstrated excellent film quality and dielectric characteristics. In this presentation, we compare the microstructural and electrical properties of ZrO₂ films grown by the ALD technique on Si and Ge substrates with different surface cleaning/passivation methods. A cold wall ALD system with ZrCl₄/H₂O precursors was used and the deposition was carried out at 300°C. ZrO₂ microstructures on different substrates were investigated using HR-TEM imaging and electron diffraction. Several compositional analyses were performed using AR-XPS and the electrical properties such as C-V and I-V characteristics were compared using Pt gate capacitor structures fabricated through a shadow mask process. High-k dielectric deposition by ALD often occurs readily on hydroxylated surfaces such as chemical SiO₂ or a hydroxylated oxynitride passivation. Deposition processes for gate dielectric preparation on Si surfaces usually result in the unavoidable and uncontrolled formation of a thin interfacial oxide layer if the Si is not already passivated by such a layer prior to deposition. However, in contrast to results on Si substrates, ALD deposition of ZrO₂ film on a Ge (100) substrate showed locally epitaxial growth without a distinct interfacial layer unlike ZrO₂ on SiO₂/Si. Due to the large lattice mismatch (~10%) between ZrO₂ and Ge, a significant areal density of interfacial dislocations was observed. The effects of interface traps, possibly the result of these interfacial dislocations, on the CV hysteresis and frequency dispersion will be presented.

SESSION D3: POSTER SESSION
ADVANCED GATE STACK MATERIALS
Chairs: Hiroshi Kitajima and Robert J.P. Lander
Tuesday Evening, April 22, 2003
8:00 PM
Salon 1-7 (Marriott)

D3.1

A NEW PARAMETER OF PREDICATING GM FOR ULTRA THIN NITRIDED GATE OXIDE. Mitsuaki Hori^a, Naoyoshi Tamura^a, Masataka Kase^a, Hiroko Sakuma^b, Hiroyuki Ohata^b, Mayumi Shigeno^b, Yuuzi Kataoka^b, ^aFujitsu, ^bFujitsu Lab., Tokyo, JAPAN.