

(C-V) measurements on as deposited W/HfO₂ films result in a CET $\sim 15.5 \text{ \AA}$, low C-V hysteresis, and low leakage ($6 \times 10^{-4} \text{ A/cm}^2$). However, high frequency CVs clearly show the presence of a high density of interface states. Post metal anneals are required to eliminate these interface states and result in an increase of the CET. Structural analysis of the as deposited gate stack by high resolution transmission electron microscopy (HRTEM) shows a well defined W/HfO₂ interface in contrast to as deposited Al/HfO₂ interfaces which clearly show a reacted layer and also a higher CET for the same thickness of stack. Upon post metal annealing, HRTEM images of W/HfO₂ indicate a thickening of the interfacial layer between the HfO₂ and Si, corroborating the increase in CET. Annealed W/HfO₂ films have a CET $\sim 16.5 \text{ \AA}$, low C-V hysteresis $< 15 \text{ mV}$, leakage 5 orders of magnitude better than an equivalent SiO₂ film and minimum flatband shift (extracted workfunction of W $\sim 4.7 \text{ eV}$) indicating little fixed charge in the gate stack. In addition, charge trapping has been monitored in these films as a function of different rapid thermal anneals.

D3.13

YTTRIUM STABILIZED HfO₂ EPITAXIAL THIN FILMS - A NEW APPROACH FOR HIGH-k GATE DIELECTRIC. P.F. Lee, J.Y. Dai, H.L.W. Chan and C.L. Choy, Department of Applied Physics, Hong Kong Polytechnic University, Hung Hom, Kowloon, Hong Kong, CHINA.

HfO₂ is an attractive candidate for high-k gate dielectric due to its thermodynamic stability on Si under high temperature annealing. Epitaxial growth of HfO₂ thin films on Si is of significant fundamental and technological interest, even though the amorphous structure has been commonly accepted as the approach to select high-k gate dielectric candidates. We report successful epitaxial growth of yttrium stabilized HfO₂ thin films on p-type (100) Si substrates by pulsed laser deposition at relatively lower substrate temperature of 550°C. Transmission electron microscopy observation illustrated a fixed orientation relationship between the epitaxial films and Si substrates, i.e. (100)Si||[100]HfO₂ and [001]Si//[001]HfO₂. However, the rough film/Si interface suggests that interdiffusion and interfacial reaction at the interface may happen. High-resolution deep profile X-ray photoelectron spectroscopy analysis (XPS) revealed Hf silicate formation at the interface area. Very next to Si surface, XPS spectra also show the presence of Hf-Si bonding. Capacitance-voltage measurement revealed that an equivalent SiO₂ thickness of about 10Å has been achieved by a 40Å-thick epitaxial yttrium stabilized HfO₂ film with a leakage current density of $1 \times 10^{-2} \text{ A/cm}^2$ at 1 V gate bias voltage. The growth mechanism of the yttrium stabilized HfO₂ thin films on Si has been studied and it was found that substrate temperature is a critical parameter for the epitaxy of yttrium stabilized HfO₂ films. Substrate temperature higher than 600°C causes SiO₂ formation on Si surface before film deposition and therefore prevents the intended epitaxial growth. On the other hand, the films grown at substrate temperature lower than 450°C also resulted in polycrystalline structure even the interface is free from SiO₂ layer. This can be interpreted by relatively lower kinetic energy of Hf and O atoms arrived at the Si surface at lower substrate temperature leading to island growth of the films.

D3.14

MICROSTRUCTURAL EVOLUTION OF ZrO₂/HfO₂ NANO-LAMINATE GATE STACKS GROWN BY ATOMIC LAYER DEPOSITION. Hyongsu Kim, Man-Ho Cho^a, Paul C. McIntyre, Stanford Univ., Dept of Materials Science & Engineering, Stanford, CA; Krishna Saraswat, Stanford Univ., Dept of Electrical Engineering, Stanford, CA; ^acurrently at Korea Research Institute of Standards and Science, Daejeon, KOREA.

Among many possible high-k dielectric candidates for the future sub-nanometer MOSFET devices, ZrO₂ and HfO₂ are attractive because of their relatively high dielectric constant and large bandgap. Although ZrO₂ and HfO₂ have similar electrical properties, including their dielectric constants, ZrO₂ is typically deposited as a polycrystalline (tetragonal) phase and HfO₂ as amorphous, especially using low thermal budget processes such as atomic layer deposition (ALD). In this presentation, microstructural evolution and electrical properties of nanolaminate structures composed of alternating ZrO₂ and HfO₂ layers will be investigated. In order to obtain extremely precise thickness and interface control without breaking vacuum, ALD was used because excellent film quality can be achieved owing to its surface adsorption-controlled deposition mechanism. A cold wall ALD system with ZrCl₄/H₂O and HfCl₄/H₂O precursors for ZrO₂ and HfO₂, respectively, were used and the deposition was carried out at 300°C on a p-type Si substrate having $\sim 15 \text{ \AA}$ chemical or thermally grown SiO₂ surface passivation. Alloy and nanolaminate structures having different layer sequences with different numbers of layers were grown and their film microstructures were investigated using HR-TEM imaging and electron diffraction. Nanolaminate structures composed of ZrO₂ layers larger than a characteristic thickness had a

polycrystalline structure with both tetragonal and monoclinic phases, and their surface roughness and final film grain size strongly depended on the identity of the initial layer deposited. Electrical properties such as C-V and I-V characteristics were evaluated using Pt gate capacitors fabricated through a shadow mask process.

D3.15

COMPARISON OF UV-OZONE PROCESSED HfO₂ AND ZrO₂ HIGH-κ GATE DIELECTRICS. David Chi, Shriram Ramanathan, and Paul C. McIntyre, Department of Materials Science and Engineering, Stanford University, Stanford, CA.

Oxidation of thin metal films in the presence of ultraviolet light has been shown to produce high quality metal oxide gate dielectric layers. The oxides of hafnium and zirconium are both considered potential high-κ replacements for SiO₂ in future MOS devices. Growth kinetics for these two metal oxides under UV-ozone conditions is compared using imaging (HRTEM) and ion scattering (NRA) techniques. The primary advantage of nuclear reaction analysis (NRA) is its high sensitivity to oxygen. Accurate measurements of oxygen areal density were used to calculate effective metal oxide thicknesses. Results from NRA were corroborated using HRTEM. Our results show that the UV-ozone process can be used to fabricate gate oxides of the thickness required for the gate dielectric application. Electrical measurements (CV, IV) on MOSCAP structures demonstrate the promise of UV-ozone grown HfO₂ and ZrO₂ as gate dielectrics on Si substrates passivated by an ultrathin SiO₂ layer. Capacitance-derived EOT values of 1.5-2.0 nm (without quantum mechanical corrections) were obtained for starting metal precursor thicknesses of 2.0 nm, corresponding to 2.5-3.5 nm final metal oxide layer thickness. Leakage current densities were on the order 10^{-4} A/cm^2 at 1 V bias. Electrical results obtained were highly dependent upon the surface passivation of the silicon substrate. Several passivation methods will be discussed. The procedure yielding the optimum electrical results entailed an HF strip followed by a low P_{O2} UV-ozone re-oxidation of the Si surface.

D3.16

EFFECTS OF Ge ON THE ELECTRICAL PROPERTIES OF MOS CAPACITOR WITH POLY Si/HfO₂ AND POLY Si_{0.4}Ge_{0.6}/HfO₂ GATES STACK AFTER VARIOUS ANNEALING VARIOUS ANNEALING CONDITION. B.G. Min, S.K. Kang, S. Nam, S.W. Nam, D.-H. Ko, Department of Ceramic Engineering, Yonsei University, Seoul, KOREA; H.B. Kang, C.W. Yang, School of Metallurgy and Material Engineering, Sung Kyun, Kwan University, Suwon, Kyounggi-do, KOREA; K.Y. Lim, Memory Research and Development Division, Hynix Semiconductor Inc, Ichon, Kyounggi-do, KOREA.

Recently, high K dielectric films have been suggested as alternatives to the currently employed SiO₂ gate dielectric for CMOS-FET technology since high k dielectric films reduce the leakage current and improve the reliability without decreasing oxide capacitance. Among the suggested materials, HfO₂ films have received attention due to the high k value, wide band gap, and low heat of formation. In addition, HfO₂ films are compatible with conventional CMOS processes including a poly silicon gate electrode without any barrier layer. In spite of previous studies, long time and high temperature annealing is expected to bring about the silicidation in the poly Si/ HfO₂ system, as like poly Si/ZrO₂ system, due to the similar chemical properties. Furthermore, as the gate depletion effect and boron penetration becomes more prominent for the sub-10Å oxide regime, it is importantly considered that other gate material, such as a metal gate and poly Si_{1-x}Ge_x films, have to replace poly Si. In our experiments, poly Si_{0.4}Ge_{0.6} films were deposited on HfO₂ films as a gate electrode to compare with the electrical results of the poly Si/ HfO₂ gates stack after annealing. It is well known that the Ge in the epi Si_{1-x}Ge_x films retarded the silicidation in the Ti, Co, Zr/ Si_{1-x}Ge_x system as compared to the Co, Ti, Zr/Si system. From these previous results, compared with poly Si/ HfO₂ system, the silicidation will be retarded in poly Si_{1-x}Ge_x/ HfO₂ system after annealing and then, the retardation of silicidation is expected to bring about other reaction, silicate formation, in poly Si_{1-x}Ge_x/ HfO₂. HfO₂ films and poly Si_{1-x}Ge_x (x=0, 0.6) films were deposited by using a DC magnetron sputtering and a low pressure chemical vapor deposition (LPCVD) system. After the formation of the MOS structure, the specimens were annealed from 700°C to 900°C in N₂ ambient for 5min and the electrical properties were measured by using C-V and I-V measured.

D3.17

HIGH-κ METAL OXIDES DIELECTRICS ON Ge (100) SUBSTRATES. David Chi, Baylor B. Triplett, and Paul C. McIntyre, Department of Materials Science and Engineering, Stanford University, Stanford, CA; Chi On Chiu and Krishna C. Saraswat, Department of Electrical Engineering, Stanford University, Stanford, CA; Eric Garfunkel and Torgny Gustafsson, Departments of Chemistry and Physics, Rutgers University, Piscataway, NJ.

As a semiconductor channel material for use in future scaled MOS transistors, Ge has the advantage of enhanced low-field mobility compared to Si. However, a primary drawback that has limited use of Ge surface channel devices is the absence of a stable Ge oxide that can serve as a dielectric and a surface passivation. With the expected introduction of deposited high- κ dielectrics in MOS technology, the poor quality and stability of GeO₂ may no longer be a significant obstacle to development of Ge-channel field effect transistors. Growth of ZrO₂-based gate dielectrics on Ge (100) substrates is reported in this presentation. UV-ozone oxidation is used to fabricate ultrathin metal oxide dielectrics. ARXPS, MEIS, and HRTEM have been used to characterize the gate stack structure with atomic resolution. A comparison of the gate stack structure of ZrO₂/Si and ZrO₂/Ge will be presented. Promising electrical results obtained from MOSCAP and MOSFET structures will also be presented, demonstrating important functional characteristics of high- κ /Ge gate stacks.

D3.18

Abstract Withdrawn.

D3.19

Abstract Withdrawn.

D3.20

HfO₂, Al₂O₃ AND HfAlO_x HIGH- κ DIELECTRICS CHARACTERIZED BY VUV SPECTROSCOPIC ELLIPSOMETRY. Pierre Boher and Christophe Defranoux, SOPRA, Bois-Colombes, FRANCE; Hugo Bender, IMEC, Leuven, BELGIUM.

New high κ dielectric materials are intensively investigated to replace the silicon dioxide as gate dielectric in the next generations of electronic devices. Several candidate materials and deposition processes are currently under investigation but the technological problem is difficult due to the specifications of these new materials not only in terms of electrical properties but also for the compatibility with the fabrication process of the devices. In any case, the layer thickness which will be used in the future devices is of the order of some nanometers and a precise control of this critical stage of the process will be mandatory. In this respect, spectroscopic ellipsometry has long been recognized as a powerful technique for thin film characterization and is now used routinely to control thin films and multilayers at different stages of the device fabrication process. For very thin layers like high κ dielectrics, the situation is complicated by the fact that the interface properties play a key role in the device. A precise physical model is then needed to extract accurate information from ellipsometry. In addition, since these layers are completely transparent in the visible and UV range, the correlation between thickness and refractive index is very high and so, structural and thickness information cannot be extracted independently. In this paper, we use vacuum UV (VUV) spectroscopic ellipsometry to characterize such layers. Indeed, all the candidates for high κ dielectrics become absorbent when the wavelength is reduced down to 190nm. So, the correlation between thickness and refractive index is reduced in the VUV range and more precise structural information can be deduced. HfO₂, Al₂O₃ and mixed HfAlO_x layers have been deposited by Atomic Layer Deposition (ALD) on a 1 nm oxide grown in-situ by rapid thermal oxidation (RTO) on 200 mm (100) silicon wafers. The thickness and the composition of the layers has been changed and some wafers have been annealed in a nitrogen ambient at 700°C after the deposition. X-ray reflectometry (XRR) has been used to measure precisely the layer thickness and transmission electron microscopy (TEM) was used to get information on the crystallinity and on the interface properties. In particular, it will be shown that VUV spectroscopic ellipsometry can detect the crystalline character of the HfO₂ layers thanks to the absorption peaks detected in the VUV range. The composition of HfAlO_x layers can also be deduced in addition to the layer thickness from the optical absorption in the same wavelength range.

D3.21

FLAT-BAND VOLTAGE STUDY OF ATOMIC-LAYER-DEPOSITED ALUMINUM-OXIDE SUBJECTED TO SPIKE THERMAL ANNEALING. A.T. Fiory, V.R. Mehta, and N.M. Ravindra, New Jersey Institute of Technology, Newark, NJ; Mun Yee Ho and G.D. Wilk, Agere Systems, Berkeley Heights, NJ; T.W. Sorsch, Bell Laboratories, Lucent Technologies, Murray Hill, NJ.

High-K dielectrics based the oxide of Al were prepared by atomic layer deposition (ALD) on 200-mm diameter Si wafers in an ASM Pulsar ALCVD system. Films were deposited directly on clean Si or on ~0.5-nm underlayers of chemical oxide, rapid thermal oxide, and rapid thermal oxynitrides grown in NO and a mixture of O₂ and NO. The purpose of the underlayer films is to provide a barrier for atomic diffusion from the crystalline Si to the high-K dielectric film. Deposited Al-oxide films varied in thickness from 2 to 6 nm. Post deposition anneals were used to stabilize the ALD oxides. Equivalent oxide thickness varied from 1.5 to 3.5 nm. In situ P-doped 160-nm

amorphous-Si films were deposited over the oxides to prepare heavily-doped gate electrodes in the MOS structures. Samples were rapid thermal annealed in N₂ ambient at 800°C for 30 s, or spike annealed at 950, 1000, and 1050°C (nominally zero time at peak temperature). Heating and cooling rates are approximately 50°C /s. Flat band voltages (V_{FB}) were determined from C-V measurements on dot patterns. The 800°C anneals were used as a baseline, at which the poly-Si electrodes are crystallized and acquire electrical activation while subjecting the high-K dielectrics to a low thermal budget. Positive shifts in V_{FB} were observed, relative to a pure SiO₂ control, ranging from 0.2 to 0.8V. Spike annealing changes V_{FB} towards that for SiO₂ for ALD films deposited over underlayer films. The V_{FB} shift and the changes with annealing temperature show systematic dependence on the nitridation of the underlayer.

D3.22

LS-MOCVD OF BARIUM STRONTIUM TITANATE THIN FILMS USING NOVEL PRECURSORS. Hyun Goo Kwon, Young Woo Oh, Jung Woo Park, Young Kuk Lee, Chang Gyun Kim, Yunsoo Kim, Thin Film Materials Laboratory, Advanced Materials Division, Korea Research Institute of Chemical Technology, Daejeon, KOREA; Do Jin Kim, Department of Materials Engineering, Chungnam National University, Daejeon, KOREA.

BST have attracted much attention in memory devices due to their high dielectric constants. However, low volatility of the Ba or Sr precursors with only thd ligands has limitations in obtaining high quality thin films by liquid source metal organic chemical vapor deposition (LS-MOCVD) processes. To improve the volatility of these precursors, many attempts have been made such as adding polyether ligands to satisfy the coordinative saturation. We report the synthesis of new precursors Ba(thd)₂(tmeea) and Sr(thd)₂(tmeea), where tmeea = tris[2-(2-methoxyethoxy)ethyl]amine, and LS-MOCVD of barium strontium titanate (BSTO) thin films using these precursors. Due to increased basicity of amines compared with ethers, it is expected that the nitrogen-donor ligand will make a strong bond to a metal than an analogous oxygen-donor ligand, consequently improving the volatility and thermal behavior of these precursors. Thin films of BSTO were grown by LS-MOCVD using a cocktail source consisting of the conventional Ti precursor Ti(thd)₂(OiPr)₂ and these new Ba and Sr precursors. As-grown films were characterized by XPS, SEM, XRD, XRF, and C-V and I-V measurements. BSTO films grown at 420°C were stoichiometric BST with very smooth surface morphology and their dielectric constants were found to be as large as 450. Dependence of the composition and the electrical properties of the BSTO films on the growth temperature, working pressure, and the composition of the cocktail source will be discussed.

D3.23

METAL-ORGANIC CHEMICAL VAPOR DEPOSITION OF Pr₂O₃ FILMS ON SILICON SUBSTRATES. Raffaella Lo Nigro and Vito Raineri, Consiglio Nazionale delle Ricerche, IMM-sezione di Catania; Roberta Toro, Graziella Malandrino, Ignazio Fragala, Univ of Catania, Dept. of Chemistry, Catania, ITALY.

In recent years, Pr₂O₃ has received much attention because of the possible use as alternative gate dielectrics in CMOS devices. Physical vapor deposition methods have been successfully used to grow Pr₂O₃ films on silicon substrates, while, to date, there are no studies on chemical vapor deposition methods. We report on the results of a recent study on the deposition of praseodymium oxides thin films on silicon substrates by metal-organic chemical vapor deposition (MOCVD). Suited Pr(III) b-(diketonate) precursor has been used as the metal source and the deposition conditions have been carefully selected because of a large variety of possible PrO_{2-x} (x= 0-0.5) phases. Pr₂O₃ films have been obtained in a non oxidizing ambient in an hot-wall MOCVD reactor, using 750°C deposition temperature, while Pr₆O₁₁ films were formed using 50-100 sccm oxygen flow as reaction gas. The structural and morphological characteristics of Pr₂O₃ films were carried out by X-ray diffraction (XRD), high resolution transmission electron microscopy (TEM) and atomic force microscopy (AFM). Chemical compositional studies have been performed by energy filtered transmission electron microscopy (EFTEM) analysis and a fully understanding of the MOCVD process has been achieved. Preliminary electrical measurements point to MOCVD as a reliable growth technique to obtain good quality Pr₂O₃ films.

D3.24

INTERFACE CHARACTERIZATION OF THE HIGH- κ GATE DIELECTRIC Pr₂O₃. Hans-Joachim Müssig and Jarek Dąbrowski, IHP, Frankfurt (Oder), GERMANY; Dieter Schmeisser, Angewandte Physik-Sensorik, BTU Cottbus, Cottbus, GERMANY.

Pr₂O₃ is currently under consideration as a potential alternative gate dielectric candidate for sub-0.1 μ m Complementary Metal Oxide Semiconductor (CMOS) technology [1-3]. For all thin gate dielectrics,