potential, germanium wafers need to be available, and this at the same size and standard obtained for silicon wafers. Providing germanium wafers on silicon carriers, i.e. germanium-on-insulator (GeOI), gives the product some additional advantages. Germanium does not have the same strength as silicon wafers, leading to potential breakage issues in wafer fabs. GeOI allows to strengthen the wafer up to the carrier material strength (i.c. silicon). It also allows the robotic equipment to be solely in contact with silicon, partially avoiding contamination issues with germanium. Moreover integration of germanium and silicon allows for combined material electronics such as optical germanium receivers on silicon substrates. Finally, the limited availability of bulk germanium, which could otherwise hamper its use in large volume semiconductor industry, is hereby solved by limiting the germanium consumption to the top μm's of the wafer. Recent developments in crystal growth and substrate production have led to the manufacturing of 200mm germanium substrates. Here GeOI wafers with diameters of 100mm and 200mm are reported using back−grind technology. By choosing box layer deposition techniques and effective chemical, mechanical and megasonic cleaning of the wafers to be bonded, nearly void-free wafers can be produced as demonstrated by acoustic imaging. Bond strengths sufficient to withstand grinding and polishing operations without delamination were obtained by applying plasma activation under atmospheric conditions previous to bonding (Süss MicroTec patent pending). This allowed a relaxation on the thermal annealing of the bonded pairs, which is important as germanium and silicon have a large difference in thermal expansion. By optimising the bulk germanium wafer grinding and polishing process to GeOI wafers, device layer thicknesses down to 5μm were realised with TTV less than 2μm. Despite the thermal expansion differences between device and carrier materials, bow and warp figures were kept within normal Si wafer specifications. Although development of GeOI wafers must be further improved and is still on-going at Umicore Electro-Optic Materials, we believe that the development of GeOI wafers up to 200mm diameter will facilitate the integration of germanium in the silicon environment, allowing the research community to demonstrate its potential use for high-performance micro−electronics, MEMS and MOEMS.

SESSION B5/D5: Joint Session: High-k and High Mobility Substrates
Chair: Tsutomu Tezuka
Wednesday Morning, April 14, 2004
Room 2004 (Moscone West)

10:15 AM *B5.1/D5.1

Novel Deposition Processes for High-k/Ge Devices: Interface Engineering. Paul McIntyre[1], Hyoungsub Kim[1], David Chi[1], Chi On Chui[2], Baylor Triplett[1], Ali Javey[3], Hongjie Dai[3] and Krishna Saraswat[2]; [1]Materials Science and Engineering, Stanford University, Stanford, California; [2]Electrical Engineering, Stanford University, Stanford, California; [3]Chemistry, Stanford University, Stanford, California.

High permittivity dielectric materials and metal gate electrodes are currently being investigated by many research groups world-wide in an effort to continue the aggressive dimensional scaling of metal oxide semiconductor devices. The development of relatively high-quality deposited gate dielectrics to replace SiO2-based dielectrics for silicon field effect transistors presents an opportunity to consider alternative materials for the semiconductor channel in such devices. There are many fundamental advantages to using Ge in the channel in place of Si. The relative instability of GeO2 with respect to most high-k metal oxides under oxidizing conditions may avoid growth of an undesirable low-k interface layer under the deposition conditions used to form the high-k gate dielectric, in contrast to the typical situation for high-k deposition on Si. Furthermore, use of Ge may result in lower temperatures for dopant activation compared to Si. The larger (and better-matched) low-field carrier mobilities in Ge relative to Si result in devices that operate beyond the universal mobility model for Si MOSFETs. In this presentation, results obtained from atomic layer deposition- and UV-ozone oxidation-synthesized metal oxide dielectric layers on Ge (100) substrates will be compared. Physical characterization of HfO2 and ZrO2 gate dielectric layers and their interfaces with different Ge surface passivations will be emphasized. Recently published electrical data obtained from MOSCAP structures and high-k Ge MOSFETs will also be reviewed. The presence and effects of interface states on electrical behavior will be discussed, including comparison with results obtained from high-k/SiO2/Si and high-k/carbon nanotube devices.

10:45 AM B5.2/D5.2

Synchrotron Radiation Photoemission Spectroscopy of High-k Gate Stack in High-performance Ge MOS Devices.
Chi On Chui[1], Dong-Ick Lee[2], Andy A. Singh[2], David Chi[3], Paul C. McIntyre[3], Piero A. Pianetta[2] and Krishna C. Saraswat[1]; [1]Electrical Engineering, Stanford University, Stanford, California; [2]Stanford Synchrotron Radiation Laboratory, Menlo Park, California; [3]Materials Science and Engineering, Stanford University, Stanford, California.

The saturation of Si MOSFET drain current upon dimension shrinkage may limit the prospect of future scaling. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Nonetheless, unlike Si, the poor quality Ge native dielectrics for gate insulator and field isolation have hindered the realization of Ge MOS devices in the last four decades. Inspired by the recent successes of the high-k dielectric deposition technique on Si and the thermodynamically unstable nature of the common germanium native oxides, we have investigated the possibility of applying high-k dielectrics to Ge without a native oxide interlayer. We have fabricated MOS capacitors on Ge with zirconia gate dielectric using ultraviolet-assisted ozone (UVO) oxidation of thin Zr metal at room temperature on Ge surface with various treatments. In addition, this novel dielectric technology has led to the demonstration of high-performance Ge MOSFETs with enhanced carrier mobility. To study the scalability of the gate stack and inspect the existence of an interfacial layer, high-resolution cross-sectional transmission electron microscopy (HR-XTEM) was used to examine the ZrO2-Ge interface microstructure; though the poor phase contrast between ZrO2 and GeOx (if any) mandates a better physical characterization. In this presentation, we analyze the elemental composition variation across the dielectric layer by applying synchrotron radiation photoemission spectroscopy (SR-PES) to ZrO2 on Ge samples wet etched in an atomic layer scale. Core-level spectra for Ge have been taken at specific kinetic energies to minimize the Zr subshell photoemission cross-section and thus avoiding interference. These spectra were then peak-fitted and modeled to map out the elemental depth profile. Lastly, their impact on future Ge MOSFET scaling will be addressed.

11:00 AM B5.3/D5.3

integration of high-K dielectrics and metal gate electrodes with strained silicon channels. Yanxia Lin, Veena Misra and Mehmet C. Ozturk; Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina.

Strained Si devices can provide significant mobility enhancements for both electrons and holes and is being aggressively studied by many research groups. The incorporation of high-K dielectrics on strained silicon provides the additional benefit of low gate leakage current. In addition, to eliminate gate depletion problems and Fermi level pinning associated with polysilicon electrodes, metal gates are also necessary. This warrants the investigation of high-K gate dielectrics and metal gate electrodes with strained Si devices. Issues that need to be understood include the i) interfacial layer formation of strained Si/high-K dielectrics, ii) effects of metal gate electrodes on high-K dielectrics, and iii) corresponding effects on the channel strain. In this paper, strained Si films were deposited on <100> relaxed SiGe virtual substrate by rapid thermal chemical vapor deposition (RTCVD). Different Ge compositions in the SiGe substrate and different strained Si thickness were formed to introduce varying strain levels which were confirmed by Raman spectroscopy. HfO2, one of the most promising high-K gate dielectrics, was deposited by physical vapor deposition (PVD) of thin Hf layers followed by oxidation at 600 C in N2 for 30seconds. Different metal gate electrodes, both element metal and binary metal alloys, were deposited by PVD and MOS capacitors were fabricated. The paper will discuss the electrical characteristics of metal-gate high-K dielectrics and present a comparison of EOT, flatband voltage, interface traps, leakage current and work function between strained Si samples and bulk Si controls. Also the interfacial layer formation of strained Si/high-K system will be investigated and compared with bulk Si/high-K. Finally, thermal stability of EOT, flatband voltage will also be presented.

11:15 AM B5.4/D5.4

Physical characterization of HfO2 deposited on Ge substrates by MOCVD. Sven Van Elshocht, Bert Brijs, Matty Caymax, Thierry Conard, Stefan De Gendt, Stefan Kubicek, Marc Meuris, Bart Onsia, Olivier Richard, Ivo Teerlinck, Jan Van Steenbergen, Chao Zhao and Marc Heyns; IMEC, Heverlee, Belgium.
Germanium is currently under consideration as a way to improve transistor performance because of its, compared to Si, intrinsically higher mobility. Germanium oxide, however, is inherently thermodynamically unstable, preventing formation of the gate dielectric by simple oxidation. A solution might be a high-k dielectric as much progress has been made depositing thin high-quality layers. Also from a high-k point of view germanium might prove to be beneficial: the instability of germanium oxide could limit the formation of an interfacial layer allowing more aggressive scaling; and the higher mobility might (partly) compensate for the mobility degradation seen for high-k dielectrics on Si. We studied the growth properties of HfO2 deposited on Ge by MOCVD, using TDEAH and