

O₂ as precursors, and compare the results to similar layers deposited on silicon substrates. Analysis techniques include Ellipsometry, Rutherford Backscattering Spectroscopy (RBS), Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD), and Time of Flight Secondary Ion Mass Spectroscopy (TOF-SIMS). Our results show that the physical properties of MOCVD-deposited HfO₂ layers on Ge are very similar to what we have observed in the past for Si. Some of the negative aspects observed for Si, such as diffusion of substrate material in the high-k layer, a low density for thin layers, or a rough top surface, are comparable or more pronounced for the case of Ge. However, a careful surface pretreatment such as NH₃ annealing the Ge substrate prior to deposition greatly improves the physical characteristics. Most important observation is a very thin interfacial layer as predicted, offering more aggressive scaling possibilities for Ge. In conclusion, based on physical characterization, the deposition of HfO₂ on Ge by MOCVD results in layers of comparable quality compared to Si with as major difference a much thinner interfacial layer. Similar as for Si, surface pretreatments are shown to be very important.

11:30 AM B5.5/D5.5

Retarded Growth of Sputtered HfO₂ Films on Germanium. Koji Kita, Masashi Sasagawa, Masahiro Toyama, Kentaro Kyuno and Akira Toriumi; Dept. of Materials Science, The Univ. of Tokyo, Tokyo, Japan.

Ge CMOS has recently attracted much attention, because of the trend of using deposited high-k films than thermally grown SiO₂ for further scaling of CMOS devices, and of the intrinsically higher carrier mobility of Ge than that of Si. In this paper, we report a new advantage of high-k/Ge systems over high-k/Si, that both the interface layer and the HfO₂ film on Ge are thinner than those on Si despite of simultaneous fabrication processes. HfO₂ films were deposited simultaneously on Ge (100) and Si (100) wafers, after removing the native oxides. In order to restrict the interface layer growth, an ultra-thin Hf metal layer was deposited, followed by the HfO₂ film deposition by a reactive sputtering of Hf in O₂/Ar. By using TEM and a combination of the glazing incidence x-ray reflectivity (GIXR) with the spectroscopic ellipsometry measurements, the interface layer thickness was accurately determined to be 0.5 nm on Ge and 1.1 nm on Si, for the samples annealed at 500°C in O₂ (0.1%) + N₂ ambient. This result shows that the interface layer thickness on Ge is only a half of that on Si even though the films on both substrates were processed simultaneously. The ultra-thin Hf metal layer has an important role for thinner interface layer formation on Ge, since no difference of interface layer thickness was observed when HfO₂ films were deposited directly on both substrates without Hf metal layers. This phenomenon can be explained if it is assumed that Ge oxides may form a Hf-Ge-O ternary volatile compound with Hf metal. If this is the case, the total HfO₂ film thickness (without the interface layer) on Ge must be thinner than that on Si. The fact is that the HfO₂ film on Ge was 0.6 nm thinner than that on Si with TEM and GIXR measurements. Furthermore, the film thickness difference ($\Delta T_{HfO_2} = T_{HfO_2(ONSi)} - T_{HfO_2(ONGe)}$) was detected even without annealing, and then it can be assumed Hf-Ge-O volatilization would occur during the film deposition process. It is worthy of particular attention that ΔT_{HfO_2} was seen as a retardation of the film growth on Ge in the very early stage of the growth. Thus it is inferred that the Hf-Ge-O volatilization would occur with the assistance of oxygen plasma until the ultra-thin Hf metal is fully oxidized, and that it is the key mechanism for forming a thinner interface layer and a thinner HfO₂ film on Ge than those on Si. Finally, C-V characteristics of Au/HfO₂/Ge and Au/HfO₂/Si MOS capacitors were characterized. As was expected from the thickness difference of both interface layer and HfO₂ film discussed above, HfO₂/Ge MOS capacitor showed a larger accumulation capacitance than HfO₂/Si, even though they were fabricated simultaneously by the same process. These results show a new advantage of high-k/Ge over high-k/Si system from the viewpoint of fabricating a CMOS with ultra-thin high-k gate dielectric.

11:45 AM B5.6/D5.6

Metal Oxide/Semiconductor Interfaces in UV-Ozone Oxidized High- κ Dielectric Stacks on Si and Ge (001) Substrates. David Chi¹, Chi On Chui³, Shriram Ramanathan², Baylor Triplett¹, Krishna C. Saraswat³ and Paul C. McIntyre¹; ¹Department of Materials Science & Engineering, Stanford University, Stanford, California; ²Components Research, Intel, Hillsboro, Oregon; ³Department of Electrical Engineering, Stanford University, Stanford, California.

UV-ozone oxidation of hafnium and zirconium metal films to form HfO₂ and ZrO₂ gate dielectrics has been demonstrated to yield MOS gate stacks with low leakage current densities and very high capacitance densities. In this technique, metal precursor films are deposited directly on to the substrate and are subsequently transformed to metal oxides by exposure to oxygen in the presence of UV light. Because both Hf and Zr are highly reactive metals,

interaction with the substrate after deposition but before oxidation is likely. In this presentation we describe characterization of the interface between UV-ozone oxidized dielectrics and Si and Ge substrates. We demonstrate reduction of the native oxide above Si and Ge as a result of Hf or Zr deposition. However, during UVO processing, oxidation of the substrate is observed. This byproduct silicon oxide exhibits different properties than the native oxide of Si. X-ray photoelectron spectroscopy indicates a sub-oxide or silicate/germanate at the high-k/substrate interface. Results from electrical testing of MOS-capacitors with a range of oxide thicknesses will also be presented.

SESSION B6: Strained Si and SiGe Devices I

Chair: Junichi Murota

Wednesday Afternoon, April 14, 2004

Room 2004 (Moscone West)

1:30 PM *B6.1

SiGe HBT/BiCMOS Technologies and Their Applications to Communication ICs/LSIs. Katsuyoshi Washio¹, Katsuya Oda¹ and Takashi Hashimoto²; ¹Central Reserach Lab., Hitachi, Ltd., Tokyo, Japan; ²Device Development Center, Hitachi, Ltd., Tokyo, Japan.

To meet the growing demand for multi-gigabit data communication systems and wide-bandwidth radio communication systems, both high-speed digital operation with sophisticated functions and high-frequency analog operation should be implemented. High-speed monolithic integrated circuits (ICs) and large-scale ICs (LSIs) are the key components for such systems. From this point of view, the high-speed SiGe heterojunction bipolar transistor (HBT) and SiGe HBT with CMOS (BiCMOS) technologies are the most promising candidates to meet these requirements. In this paper, technologies for a self-aligned SiGe HBT and BiCMOS developed for use in optical transmission and wireless communication systems are described. A Si-cap/SiGe-base multilayer fabricated by selective-epitaxial-growth (SEG) was used to obtain both high-speed and low-power performance for the SiGe HBTs. The process except the SEG is almost completely compatible with well-established Si bipolar-CMOS technology, and the SiGe HBT and BiCMOS were fabricated on a 200-mm wafer line. High-quality passive elements, i.e., high-precision poly-Si resistors, a high-Q varactor, an MIM capacitor, and high-Q spiral inductors have also been developed to meet the demand for integration of the sophisticated functions. Both cutoff frequency and a maximum oscillation frequency of 200 GHz, and an ECL gate-delay time of 4.9 ps have been demonstrated for the SiGe HBTs. An IC chipset for 40-Gb/s optical-fiber-links, a single-chip 10-Gb/s transceiver LSI, a 5.8-GHz electronic toll collection transceiver IC, and other ICs that are applicable to optical transmission and microwave/millimeter-wave wireless communication systems have been implemented by applying the SiGe HBT or BiCMOS technique.

2:00 PM B6.2

Optimizing SiGe HBTs technology using small signal and high frequency noise device's modeling. Jean-Guy Tartarin¹,

Gilles Cibiel¹, Augustin Monroy², Vincent LeGoascoz² and Jacques Graffeuil¹; ¹CISHT, LAAS-CNRS, Toulouse, France; ²ST microelectronics, Crolles, France.

Well known properties of BiCMOS technology over RF dedicated technologies in terms of integration (RF circuits on the same chip than base band modules) get advantage from the introduction of SiGe in the HBT's base layer to improve the device operating frequencies : these technologies suit very well with applications such as voltage control oscillators (VCO) and low noise amplifiers (LNA), thanks to their good behavior in terms of low frequency as well as high frequency noise performances respectively. We have investigated the influence of technological parameters such as doping profile, doping level and thickness of the base layer (4 different wafers) on the dynamic and high frequency noise performances to converge towards the optimum technological process (now available with the BiCMOS6G process provided by ST microelectronics). We made use of S-parameters measurements on the devices to extract the electrical parameters of our small signal model (according to an original technique already published by the author). The high frequency noise parameters based on the electrical model (with noise sources added to the base-emitter junction, resistances, ...) are simulated and compared with the measured noise parameters of the devices. The four noise parameters (Fmin, Rn, and complex Γ_{opt}) measurements have been performed from 1 GHz to 12 GHz, and the dynamic S parameters measurements ranged from 40 MHz to 40 GHz. Good agreement has been found on both electrical small signal and noise model and the measurements. Thus, these models have been developed for several bias conditions : this study enabled the localization of potential technological defeats (etching, junction location, ...) and the identification of the limiting parameters on the transition frequency Ft and on the maximum oscillation frequency Fmax. The study on