section a silicon nitride layer was deposited using LPCVD over a pre-deposited low temperature oxide (LTO) layer. The second section had only the nitride layer while the third section was left uncoated. We expect inert, vacancy and interstitial injection conditions to exist in the first, second and third sections, respectively during annealing in an oxygen ambient. These samples were rapid thermal annealed (RTA) at a number of temperature/time combinations between 940-1050 degrees Celsius in oxygen. Diffusion coefficients were extracted by computer simulation, using SIMS profiles obtained from samples before and after the RTA treatment. For samples annealed at 1050 degrees Celsius for 15s, the diffusivity extracted is compatible with values published by Fair for inert diffusion, suggesting the MBE material was of fairly high quality with a low density of grown-in defects. Diffusion of B is highest in pure Si, reduced by the incorporation of 11% Ge, reduced further in Si with 0.1% C, and the lowest value in SiGe:C. In Si, Si:C and SiGe containing samples which experienced interstitial injection during annealing, a marked increase in B diffusion was observed, compared to the inert case. In samples which experienced vacancy injection, B diffusion was suppressed for the Si, Si:C and SiGe containing samples. The increase in diffusivity for the carbon-containing samples under interstitial injection annealing conditions suggests the undersaturation of interstitials by C is probably not infinite, as the injected flux of interstitials seems to overwhelm the suppression effect by C.

B8.7

Ge MOS Dielectric Stack with ALD High-k Metal Oxide and Oxynitride Interlayer. Chi On Chui[1], Hyoungsub Kim[2], Paul C. McIntyre[2] and Krishna C. Saraswat[1]; [1]Electrical Engineering, Stanford University, Stanford, California; [2]Materials Science and Engineering, Stanford University, Stanford, California.

Future scaling of Si MOSFET devices may be limited by drain current saturation. It has been proposed that the higher intrinsic carrier mobility of Ge could alleviate the limit by providing a higher source injection velocity, which results in higher drive current and smaller gate delay. To circumvent the long-lasting problem of poor Ge native surface passivation, high-k metal oxides have been introduced as the gate dielectric materials for Ge MOS applications. Among other deposition techniques, atomic layer deposition (ALD) is particularly attractive in terms of precise thickness control and near-perfect conformality for ultrathin high-k formation. On Ge surfaces after HF vapor exposure, we have demonstrated previously locally epitaxial growth of ZrO2 on Ge without a distinct interfacial layer. Due to the large lattice mismatch between ZrO2 and Ge, the electrical characteristics of these MOS capacitors were not satisfactory. By incorporating a Ge oxynitride interlayer before the ALD of high-k on Ge, excellent MOS capacitors could be obtained with very low leakage. In this presentation, we compare the high-k/Ge interface microstructure with various surface treatments including Ge oxynitride formation. The oxynitride interlayer was formed using rapid thermal nitridation (RTN) in NH3 ambient. High-resolution transmission electron microscopy (HR-XTEM) has been used for cross-sectional imaging. To confirm the nitrogen incorporation on Ge surface while optimizing the RTN condition for the best electrical results, extensive x-ray photoemission spectra (XPS) have been taken and the nitrogen percentage has been extracted as a function of temperature. On the optimum Ge oxynitride film, wet chemical processing stability have been investigated and the film has shown to be have minimum solubility in DI water, but soluble in HF. Lastly, both the C-V and I-V characteristics of these MOS capacitors will be presented and the impact of the interlayer on the future Ge MOS device scaling will be discussed.

B8.8

Growth of High-Performance SiGe MODFET Layer Structures. Jack O. Chu, Steven J. Koester, Qiqing C. Ouyang, John A Ott, Leathen Shi and Katherine L Saenger; IBM TJ Watson Research Center, Yorktown Heights, New York.

SiGe modulation-doped field effect transistors (MODFETs) are an interesting emerging technology option for high-performance communications applications, due to their potential for higher speed and lower noise operation than Si MOSFETs [1-2]. However control of short-channel effects in sub-100nm gate-length MODFETs is difficult due to the large gate-to-channel distance[3] and because counter-doping in the channel can lead to mobility degradation. In this paper we describe the regrowth of vertically-scaled Si/SiGe n-MODFET layer structures on buried p-type layers and thin SiGe-On-Insulator(SGOI) substrates, and also show that these innovations should enable the realization of MODFETs with f_{max} well over 200 GHz. The layer structures were grown by UHV-CVD on 8” Si(100) wafers and consisted of a $Si_{0.7}Ge_{0.3}$ bottom barrier layer, a strained Si quantum well, a top undoped $Si_{0.7}Ge_{0.3}$ spacer layer, a n-$Si_{0.7}Ge_{0.3}$ phosphorous doped supply layer and a Si cap layer. The spacer and supply layers were appropriately reduced or scaled for improved performance by leveraging reduced growth rate effects for P in order to improve the steady-state incorporation of phosphorous[4]. In this way, layer structures with ”thinner” n+SiGe supply layers of <10nm were grown with carrier densities of $2x10^{12}cm^{-2}$ and no mobility degradation was observed when compared to thicker samples. We have also demonstrated for the first time the growth of similar scaled layer structures on p-well implanted SiGe buffer layers. However, it was found that reduced temperature conditions were needed for the initial regrown layers to prevent 3D growth. Using lower temperature conditions Si quantum wells as close as 20nm to the regrowth interface were grown without mobility degradation compared to control samples, though some carrier depletion was observed. Finally, we have demonstrated the regrowth of high performance MODFET layer structures on thin SGOI substrates. The SGOI substrates were fabricated by wafer bonding, and consisted of a relaxed $Si_{0.7}Ge_{0.3}$ layer with thickness of 50nm. The regrown MODFET layer structures on SGOI substrates have shown high room-temperature mobility of >1700 cm^2/Vs, a value comparable to bulk controls. The total SGOI thickness after regrowth was about 100nm, which is considerably thinner than in previous work[5]. The current SGOI layer structures are planned to be used for fabricating 50nm gate-length MODFETs, which according to numerical simulations should produce f_{max} values over 200 GHz, while still maintaining acceptable voltage gain and good turn off characteristics. [1] S.J. Koester et al, Spring MRS (2004). [2] M. Enciso-Aguilar et al., Electron. Lett. 39, 149 (2003). [3] C. Ouyang et al., SISPAD (2002). [4] J.O. Chu et al, Spring MRS (1996). [5] J.O. Chu et al, Spring MRS (2001).

B8.9

Heteroepitaxial growth and characterization of Ge and SiXGe1-X films on patterned silicon structures*.
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Epitaxial growth has often been a key component in the development of new materials. Recently, there has been a great interest in strained Si-based heterostructures to achieve high mobility optoelectronic materials.In order to produce relaxed Si1-xGex on a Si substrate, conventional practice has been to grow a uniform, graded, or stepped, Si1-xGex layer beyond the metastable critical thickness. The aim of the various buffer structures is to reduce the threading dislocation density in the epilayer. This work is based on novel 2-D structures on the silicon surface that facilitate strain relief and allow us to obtain epilayers that are free of defects. Conventional lithography techniques have been combined with reactive ion and wet-chemical etching to fabricate a 2-D patterns of silicon mesas. The pitch of the pattern was kept constant while the width of the posts was varied. Heteroepitaxial growth of Ge/SixGe1-x layers on these micrometer-scale structures was investigated. These types of structures can potentially absorb thermal expansion and lattice expansion mismatch as well as enable liftoff of heteroepitaxial layers for subsequent wafer reuse. While, keeping the growth parameters constant, the geometry of the structures was varied to determine the optimum configuration for the highest quality heteroepitaxial growth. In this work, the quality of the Si1-xGex buffer system was investigated using high-resolution x-ray reciprocal space mapping by triple-axis x-ray diffractometry. We have used transmission electron microscopy (TEM) to analyze the epilayer cross-sections. Surface morphology was analyzed using scanning electron microscopy (SEM), atomic force microscopy (AFM) and optical microscope. Our results show that the quality of the heteroepitaxial layers improves as the width of the posts in the 2-D pattern was decreased. *This research was performed using the facilities at the Center for High Technology Materials at UNM.

B8.10

Diffusion of Boron and Silicon in Germanium. Suresh Uppal[1], Arthur F. W. Willoughby[1], Janet M. Bonar[2], Nick E. B. Cowern[3], Tim J. Grasby[4], Mark G. Dowsett[4] and Richard J. H. Morris[4]; [1]Materials Research Group, University of Southampton, Southampton, Hampshire, United Kingdom; [2]Department of Electronics and Computer Science, University of Southampton, Southampton, Hampshire, United Kingdom; [3]School of Electronics, Computing and Mathematics, University of Surrey, Guildford, United Kingdom; [4]Physics Department, University of Warwick, Coventry, United Kingdom.

Channel engineering in combination with ultra shallow junctions using ion implantation has shown potential for improvement in performance of existing MOSFET devices. On material front, strained Si, $Si_{1-y}Ge_y$, and Ge layers grown on $Si_{1-x}Ge_x$ (y>x) virtual substrates are prospective candidates especially for p-type MOSFET. In the present work, the diffusion of boron and silicon in germanium is studied using implantation doping. Concentration profiles after furnace annealing in the temperature range 675-900°C were obtained using high resolution secondary ion mass spectroscopy (SIMS). Diffusion coefficients are calculated by fitting the annealed profiles