Kaneko, Soichi Yamazaki, Kazuhiro Eguchi and Yoshitaka Tsunashima; Toshiba Corporation, Semiconductor Company, Yokohama, Japan.

Metal gate electrode without gate depletion and B penetration is required to realize high performance CMOSFETs for hp 45nm generation and beyond. Fully silicide gate processing is attractive technology for realizing metal gate transistors, since it is compatible with conventional Si processing. However, it is reported that work function of fully silicide gate electrode on high-k dielectric differs from that of fully silicide gate electrode on SiO2. Therefore, in order to clarify the root causes of this phenomenon, we studied the workfunction of various kinds of fully silicide gates on HfSiON gate insulator. In this report, we discuss about a thermal stability of fully silicide gate and a controllable range of workfunction on both SiO2 and HfSiON gate insulator. In this study, we formed MOS capacitors to measure workfunctions of various fully silicide gates. At first, a SiO2 gate insulator is thermally grown on Si substrates. Oxide thickness is varied from 5nm to 10nm. A HfSiON film with thickness of 4.5nm is deposited on the SiO2. A 100nm thick Poly-Si film is deposited on the HfSiON/SiO2 stacked gate insulator. Poly-Si gate is formed by dry etching. On the Poly-Si gate, various metal films, such as Ni, Co, Pt, and Er, are deposited. Silicide formation is carried out by annealing at the range of temperature from 250°C to 450°C for 1hours in a N2 ambient. After the silicide formation, unreacted metal is removed. Finally, forming gas annealing is carried out at 450°C for 1hour. We obtained work functions of metal silicide gates from flat band voltage as a function of dielectric film thickness by C-V We examined thermal stability of fully silicide gate on both SiO2 and HfSiON gate insulator. In Ni2Si gate, a fully silicide is completely formed at 350°C. At annealing temperature of silicide formation above 400°C, leakage current of MOS capacitor with HfSiON gate insulator degraded. On the other hand, no degradation is observed on MOS capacitor with SiO2 gate insulator at annealing temperature of 450C. The degradation of electrical property is due to diffusion of Ni atoms into the HfSiON gate insulator. Work function of Ni2Si gate electrode on SiO2 and on HfSiON gate insulator are 4.66eV and 4.73eV, In PtSi gate, no degradation is observed on MOS capacitor with HfSiON gate insulator at annealing temperature of 450°C. In order to examine the interface between PtSi and gate insulator, we observed the cross section by TEM. No apparent interaction of PtSi/HfSiON is observed. However, work function of PtSi gate electrode on HfSiON The work function of metal silicide on the SiO2 was successfully controlled from 3.9eV to 4.8eV by using ErSi1.7 and PtSi gate electrode. The controllable range of workfunction of these fully silicide gate is 0.9eV. On the other hand, the controllable range of work function was found to be so narrow as 0.34eV on the HfSiON gate insulator, even though rare earth metal silicide and noble metal silicide are used.

2:30 PM G13.4
Intermixing in NiSi/HfO2/SiOx/Si Gate Stacks.
Michael Gribelyuk[3,1], Cyril Cabral[2,1], Nestor Bojarczuk[2,1], Supratik Guha[2,1], Evgeni Gusev[2,1] and Vijay Narayanan[2,1]; [1]Semiconductor Research and Development Center, IBM, Hopewell Junction, New York; [2]Research Division, T. J. Watson Research Center, IBM, Yorktwon, New York; [3]Systems and Technology Group, IBM, Hopewell Junction, New York.

Implementation of fully silicided metal gates (FUSI) together with high-k gate dielectrics provides a promising path toward further scaling of semiconductor CMOS devices. A combination of High resolution TEM (HRTEM) and a 0.5nm small probe electron energy loss spectroscopy (EELS) has been applied to study interfacial reactions between metal gate, NiSi, and high-k gate dielectric, HfO2. NiSi was found to be polycrystalline with the grain size varying from 5nm to 10nm. Some 2nm large Si regions were found between the NiSi grains. On the other hand, some NiSix grains at NiSi/MOCVD HfO2 interface were matched by lattice images to a Ni-rich m-Ni3Si phase, thus confirming a non-uniform distribution of Ni both in bulk and at the interface and incomplete silicidation. EELS analysis has shown presence of Ni in HfO2 gate dielectric (but not in underlying Si oxide film!). The same conclusion was drawn from analysis of lattice spacings of some crystalline grains of Hf oxide in HRTEM images: they could not be matched to any of reported Hf oxide phases whereby the best match was found for the Ni21Hf8 alloy. A monolayer of Si3N4 grown by MBE between Hf oxide and NiSi to prevent intermixing was found ineffective: HRTEM and EELS data showed similar results as in the stack without Si nitride.

2:45 PM G13.5
Combinatorial Study of Metal Gate Compatibility on HfO_2.
Martin L. Green[1], Kao-Shuo Chang[2], Toyohiro Chikyow[4], Ahmed Parhat[4], John Suehle[1], Eric Vogel[1], Prashant Majhi[3] and Ichiro Takeuchi[2]; [1]NIST, Gaithersburg, Maryland; [2]University of Maryland, College Park, Maryland; [3]Sematech, Austin, Texas; [4]NIMS, Tsukuba, Japan.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The SiO_2/polycrystalline Si gate stack that has served the industry for 35 years must now be entirely replaced with one having a higher capacitance and lower power dissipation. At a minimum, the interfaces of the HfO_2/metal gate electrode advanced gate stack must be thermally stable with respect to interfacial reactions, and the changes in electrical properties that would ensue. In this talk, we will describe research aimed at understanding the thermal as well as electrical stability of metal gate electrode layers on HfO2, a likely high-k gate dielectric. Combinatorial methodologies, ideally suited for this problem since a wide variety of metal electrode layers will be examined, will be utilized to determine the ideal composition and structure of the metal gate electrode. An ideal metal gate stack is one in which the work function is properly matched to HfO_2, and the interface between the HfO_2 and the electrode is stable under typical processing conditions. We will determine the band structure at the HfO_2/metal gate electrode interface through the extraction of appropriate parameters from I-V and C-V capacitor measurements, and internal photoemission and Kelvin probe measurements. Typical of the metal gate alloy systems that will be investigated are binary and ternary combinatorial "libraries" containing Ru, Ta, W, Pt, Al, and Si. We will also present data for polycrystalline Si gates on HfO_2, for comparison.

SESSION G14: Transistor Processing and Characterization-II
Chairs: M. Heyns and M. Meuris
Thursday Afternoon, March 31, 2005
Room 2007 (Moscone West)

3:30 PM *G14.1
Ge Based High Performance Nanoscale MOSFETs.
Krishna C. Saraswat[1], Chi On Chui[1], Tejas Krishnamohan[1], Ammar Nayfeh[1] and Paul McIntyre[2]; [1]Department of Electrical Engineering, Stanford University, Stanford, California; [2]Department of Materials Science and Engineering, Stanford University, Stanford, California.

It is believed that the difficulty in scaling the conventional Si MOSFET makes it prudent to search for alternative device structures, new material and fabrication technology solutions that are generally compatible with current and forecasted installed Si manufacturing. The saturation of Si MOSFET drain current upon dimension shrinkage limits the prospect of future scaling. It has been recently pointed out that a fundamental scaling limit for MOSFETs is the source injection velocity into the channel limiting the drain current. The lower effective mass (and lower valley degeneracy) of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Heteroepitaxial growth of Ge on Si, surface passivation for gate dielectric and field isolation and n-type dopant incorporation are classic problems that obstruct CMOS device realization in Ge. In this paper we present a review of the recent activity in this area. Using a novel multi-step growth and hydrogen anneal process we have grown heteroepitaxial-germanium layers directly on silicon, with defects confined near the Si/Ge interface, thus not threading to the surface as expected in this 4.2% lattice mismatched system. The results achieved are defect-free fully-relaxed smooth single crystal Ge layers on Si without any graded buffer SiGe layer. High mobility MOSFETs have been demonstrated in bulk Ge and in nanowires with high-k gate dielectrics and metal gates. In order to enhance performance and continue scaling MOSFETs to the sub-20nm regime, novel, high-mobility materials like strained-Si and Ge (or Si_xGe_{1-x}) are actively being researched for incorporation into the channel. We demonstrate novel heterostructures with high mobility center channel, double gate N and PFETs that incorporate novel transport principles, which fully exploit the advantage of high mobility.

4:00 PM G14.2
MOSFET with La_2HfO_7 and HfO_2 High-k Dielectrics Integrated in a Conventional Flow. Luigi Pantisano[1], Thierry Conard[1], Martine Claes[1], M. Demand[1], Wim Deweerd[1], Stefan Degendt[1], Marc Heyns[1], Michel Houssa[1], Marc Aoulaiche[1], Guilherme Lujan[1], Lara-Ake. Ragnarsson[1], Erika Rohr[1], Tom Schram[1], J. C. Hooker[2], Z. M. Rittersma[2], Jean Fompereyne[3], Jean Pierre Locquet[3] and A. Dimoulas[4]; [1]SPDT / Hirel, IMEC, Leuven, Belgium; [2]Philips Research Leuven, Leuven, Belgium; [3]IBM Research, Ruschlikon, Switzerland; [4]NCSR "Demokritos", Athens, Greece.

N-channel MOSFET were fabricated in a conventional etched gate flow using either 15A SiON or bare silicon (HF-last) as starting surface. LaHfO or HfO2 were deposited in an 8in Riber MBE tool. LaHfO or HfO2 were considered with a physical thickness in the 3-6nm range. TaN was used as gate material. Since LaHfO was found to be hydrophilic and soluble in acid solutions, no polymer removal step was done after gate etching. The gate was spacer-encapsulated