

structures exhibit good thermal stability in regards to workfunction on both SiO₂ and high-k dielectrics. The compositional analysis indicates some diffusion occurs during annealing, but we have not to date observed any evidence of pile-up of the top metal at the interface of the lower metal/gate dielectric. We investigated several possible mechanisms for the gradual workfunction transition behavior, including carrier redistribution, non-uniform thin film deposition, metal/metal reaction, and metal diffusion. While direct evidence of a diffusion mechanism for this behavior is not clearly seen in our initial compositional analyses, the electrical behavior before and after anneal points to a diffusion/reaction mechanism that saturates after the initial anneal, rather than to a carrier redistribution mechanism. We will report on all these results involving tunable workfunction bilayer metal gates on SiO₂ and high-k dielectrics.

9:30 AM G6.4

Work Function Controllability of Al-Ni Alloy Metal Gates Evaluated by Scanning Maxwell-Stress Microscopy.

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Work function (ϕ_m) control of metal gates is essential to obtain optimum threshold voltage (V_{th}) especially in FD-SOI or double-gate MOSFETs [1]. One possible candidate for a gate metal enabling work function adjustment is a binary alloy composed of metals with different work functions [2,3]. In this study, we investigated the applicability of the alloys combining Al, with low ϕ_m (4.28 eV), and Ni, with high ϕ_m (5.15 eV). Two different processes, interdiffusion of Ni/Al stack and direct sputtering of Al-Ni alloy target, were used to form Al-Ni alloy films. The CV curves of Al-Ni alloy MOS capacitors fabricated by both the processes exhibited work functions approximately between those of Al and Ni. The CV curve for the interdiffusion process, however, exhibited a significant decrease in CV slope in comparison with those of Al and Ni. In addition to the conventional CV measurement, we microscopically characterized the work function uniformity through scanning Maxwell-stress microscopy (SMM), which is capable of measuring the contact potential distribution between a sample and a probe [4]. The SMM image for the Al-Ni alloy formed by direct sputtering exhibited a uniform work function distribution, in a manner comparable to that for pure Ni film. On the other hand, the SMM image for the interdiffused Al-Ni alloy exhibited a remarkably non-uniform distribution of the work function. The non-uniform work function correlated with the degradation of CV characteristics for the interdiffused Al-Ni alloy. Thus, we conclude that direct sputtering is preferable for the Al-Ni alloy formation to suppress work function non-uniformity. The composition of the direct-sputtered Al-Ni alloy films was varied by using three different targets: Al₇₅Ni₂₅, Al₅₀Ni₅₀ and Al₂₅Ni₇₅. The CV and SMM measurements revealed that the work functions of the alloys were successfully controlled by the alloy composition. Except for the Al-rich alloy made from the Al₇₅Ni₂₅ target, the Al-Ni alloys exhibited sufficient thermal stability against annealing up to 700°C in terms of gate leak currents of the MOS capacitors. This work was partially supported by the Industrial Technology Research Grant Program (2002) of NEDO, Japan. [1] L. Chang *et al.*, IEDM (2000) 719. [2] H. Zhong *et al.*, IEDM (2001) 467. [3] I. Polishchuk *et al.*, IEEE EDL 23 (2002) 200. [4] T. Matsukawa *et al.*, J. Vac. Sci. Technol., B19 (2001) 1911

9:45 AM G6.5

Fabrication and Electrical Characteristics of HfN_x Metal Gate Electrode by MOCVD. **Wen Wu Wang**¹, Toshihide Nabatame² and Yukihiko Shimogaki¹; ¹Dept. of Materials Engineering, The Univ. of Tokyo, Tokyo, Japan; ²MIRAI-ASET, Tsukuba, Japan.

Continued scaling down of CMOS devices now requires metal gate electrode. HfN may be one of the most suitable candidates as gate electrode because of various advantages, such as work function of 4.65eV for midgap electrode material and simple device integration of HfN/HfO₂/Si MOS gate stack by single CVD/ALD apparatus just changing reactants. In this work, hafnium nitride HfN_x was prepared by MOCVD using Hf[N(C₂H₅)₂]₄ (TDEAHf) precursor and its work function was evaluated from HfN_x/SiO₂/Si stack. The film composition and electrical properties were evaluated by XPS, I-V and C-V measurements. It was found that HfN_x films with low levels of C (<0.1 at.%) and O impurities (<2 at.%) were formed by employing TDEAHf precursor and NH₃ reaction gas, however the film resistivity was very high about 4.8×10¹⁰ μΩ-cm. This was due to the formation of N-rich Hf₃N₄ phase with high resistivity. Therefore, in order to decrease the sheet resistance of HfN_x films, NH₃-free thermal growth was employed. As a result, metallic HfN_x films were synthesized. The composition and electrical properties of HfN_x films were strongly dependent on the deposition temperature, especially beyond 500°C, the resistivity was decreased to the level of 1×10⁴ μΩ-cm. For I-V and C-V measurement, in order to achieve much low total sheet resistance

for the final metal gate, Au(100nm)/Ti(50nm) layers were deposited sequentially on the HfN_x/SiO₂/Si stack by electron assisted vacuum evaporation technique. After gate patterning using Cl₂-based dry etching, the work function of HfN_x in Au/Ti/HfN_x/SiO₂/Si MOS stack was extracted from the C-V measurements of the MOS stack with different SiO₂ thickness ranging from 4nm to 10nm. The work function of MOCVD-HfN_x was estimated to be about 4.74eV. In addition, C-V characteristics revealed that the EOT values of HfN_x/SiO₂/Si MOS stack decreased for the final gate stack, e.g., Au/Ti/SiO₂/Si stack showed EOT of 11nm, the EOT value became 9.7nm. By means of XPS depth profile and composition analysis, this was confirmed to be due to the formation of Hf silicate interlayer during film deposition. The thickness of interlayer was estimated to be 3nm assuming the dielectric constant of interlayer to be 16. I-V characteristics indicate that the leakage current density was almost the same with Au/Ti/SiO₂/Si stack sample. One point should be noteworthy that a relative large slope value was extracted from the plot of flatband voltage (V_{fb}) versus equivalent oxide thickness (EOT) for the as-deposited samples. This suggests the existence of charge trapping, which may be mainly from the integration process of gate stack, especially the Cl₂-based dry etching process. The effect of post RTA treatment on reducing charge trapping will be discussed in detail. In addition, the growth sequence and RTA dependences of metal work function, EOT and leakage current are also studied.

SESSION G7: Transistor Processing and Characterization-I

Chairs: R. Chau and E. Gusev
Wednesday Morning, March 30, 2005
Room 2007 (Moscone West)

10:30 AM *G7.1

Integration of Advanced Gate Dielectrics on Germanium and Strained Germanium Channel MOSFETs. **Huiling Shang**¹,

Evgeni Gusev¹, Michael Gribelyuk², Paul Jamison², Jack Chu¹, John Ott¹, Kathryn Guarini¹ and Meikei Jeong¹; ¹IBM T.J. Watson Research Center, Yorktown Heights, New York; ²IBM MD division, Hopewell Junction, New York.

Pure Ge channel MOSFETs have been considered as one promising option for future high performance CMOS technology because of the high electron and hole mobilities in Ge. A compressively strained Ge (s-Ge) channel is expected to further enhance hole mobility due to the very small effective hole mass (0.1m₀). Indeed, dramatic hole mobility enhancement of 4-25X has been demonstrated in s-Ge MOSFETs – the highest mobility enhancement for hole carriers among all available options. However, achieving a high quality thin gate dielectric for Ge and s-Ge channel MOSFETs has proven to be challenging. We will show the effects of Ge surface preparation before the high-K film deposition and the gate electrode material on the final Ge/high-K MOS characteristics. On s-Ge channel MOSFETs, we demonstrated the thinnest ever SiO₂ (2.5nm) by low temperature remote plasma oxidation of the thin Si cap while maintaining the strain in the s-Ge layer. We have also demonstrated that combining a Ge channel with HfO₂/poly can achieve appropriate PFET V_{th}. Finally, we will describe two CMOS-compatible integration scheme for s-Ge channel PMOSFETs, including the conventional STI isolation and scaled thin gate dielectrics for high performance CMOS technology.

11:00 AM *G7.2

Germanium Deep-Submicron pFET and nFET Devices with Etched TaN Metal Gate and High-K Dielectric, Fabricated on Germanium-on-Insulator Substrates. **Marc A. Meuris**¹, Brice De Jaeger¹, Jan Van Steenberghe¹, Fabrice Letertre, Geofroy Raskin, Thierry Billon and Marc Heyns¹; ¹IMEC, Leuven, Belgium; ²Soitec, Bernin, France; ³Umicore, Olen, Belgium; ⁴LETI, Grenoble, France.

Since a few years, the interest of Ge FET devices has been increasing. The higher mobility of the germanium material could be one of the solutions for the problem of further CMOS scaling. In this paper, the results of pFET and nFET germanium devices with gate lengths down to 0.15 micron will be shown. The issues of the germanium will be discussed: the interface state passivation of the Ge/High-K interface, the diode leakage and the necessity of high quality germanium-on-insulator substrates.

11:30 AM G7.3

A Reason for Poor Ge n-MOSFET Performance: Source/Drain Junction Dose-Dependent Activation.

Chi On Chui^{1,2}, Leonard Kulig¹, Jean Moran¹, Wilman Tsai¹ and Krishna C. Saraswat²; ¹Intel Corporation, Santa Clara, California; ²Electrical Engineering, Stanford University, Stanford, California.

Ge-channel has previously been suggested to supplement Si in decanano-scale MOSFET owing to its higher complementary carrier

mobilities. This inspiration has been technologically enabled by passivating the unstable Ge surface with high-k dielectrics, which also concurrently guarantees the gate stack scalability by employing metal gate electrodes. Nonetheless, the limited thermal stability of these advanced gate stacks imposes additional complexity in optimizing the source and drain junction formation process. Since p-dopants in Ge could be activated below 400 degree Celsius with minimum redistribution, mobility enhanced Ge p-MOSFET demonstrations with metal gate and high-k dielectric have not been an issue. On the contrary, the relatively higher thermal budget required to n-dope Ge causes significant diffusion and challenges the gate stack integrity. Before a better Ge n-MOSFET performance could be discerned, an uncompromised source and drain junction formation process with minimized parasitic impedance should be established. In this work, the activation of common n-dopants in Ge and the associated dependencies are investigated. Phosphorus and arsenic were first ion-implanted into p-Ge at a range of dose, and these samples are subsequently annealed with a spectrum of thermal budgets. On these n-Ge junctions, secondary mass ion spectroscopy (SIMS) and spreading resistance probe (SRP) were employed to monitor the chemical and electrically active dopant concentration respectively. By cross-comparing these SIMS and SRP profiles, several dependencies on the activation anneal are observed. For instance, higher thermal budget anneals on a given implanted dose often lowers the maximum concentrations, which could be attributed to either an excessive diffusion or a solid-solubility limitation (SSL). In order to suppress both the first and second order diffusion effects, activations were analyzed at lower thermal budgets to map out their dose-dependency. Chemical profiles reveal an increase in maximum concentration with implanted dose, yet the accompanying electrical data indicate a rather constant active level. This resultant decrease in the fraction of activated dopant hints that any excess input dose beyond the point of SSL would not improve the junction sheet resistance, but simply worsen the crystal damage due to the surplus implants. Among others, this important finding may provide an explanation for many unsatisfactory Ge n-MOSFET experimentations, whose source and drain junctions were either over-dosed or under-activated.

11:45 AM G7.4
High-Mobility GaAs and GaN MOSFETs using Atomic Layer Deposition Al₂O₃ Gate Dielectrics. Glen Wilk¹ and Peide Ye²;
¹ASM America, Phoenix, Arizona; ²Purdue University, West Lafayette, Indiana.

Achieving excellent electrical properties of high-k films on GaAs or GaN substrates has been very difficult to realize, due to the nature GaAs interface, and the lack of a high-quality, stable native oxide. Previous attempts at depositing high-k oxides by CVD have led to high interface state density, large I-V hysteresis, and poor support of positive biases. MBE techniques have shown promising results for films such as Gd₂O₃, but this process requires ultrahigh vacuum, and extreme control of surface conditions, and therefore has several challenges for manufacturability. We have demonstrated excellent electrical properties on both GaAs and GaN MOSFETs using a robust, highly manufacturable Atomic Layer Deposition Al₂O₃ process for the gate dielectric. These MOSFET devices exhibit extremely low gate leakage currents on GaAs of ~1 pA/μm² over a 10 V gate bias range, which is many orders of magnitude lower than for MESFETs under similar bias. For these same GaAs devices, channel mobilities of ~550 cm²/Vs have been achieved at E_{eff} = 1E5 V/cm, with an f_T and f_{max} of 14 and 25 GHz, respectively, and negligible drain current drift and I-V hysteresis on these devices. GaN devices using ALD Al₂O₃ gate dielectrics have measured breakdown of ~145 V for a 2μm gate-drain spacing, with a drive current > 350 mA/mm for V_{GS} = +6V. Electron mobilities of ~1200 cm²/Vs at E_{eff} = 1E5 V/cm have been achieved on AlGaIn/GaN channels. A description of the mechanism by which this ALD Al₂O₃ process forms a high-quality interface on these channels will be given.

SESSION G8: Physical & Electrical Characterization-I
 Chairs: P. McIntyre and K. Saraswat
 Wednesday Afternoon, March 30, 2005
 Room 2007 (Moscone West)

1:30 PM *G8.1
Negative Bias Temperature Instabilities in High-k Based MOSFETs. Michel J. C. Houssa¹, Marc Aoulaiche¹, Stefan De Gendt¹, Guido Groeseneken¹, Marc Heyns¹ and Andre Stesmans²;
¹IMEC, Leuven, Belgium; ²Department of Physics, University of Leuven, Leuven, Belgium.

Negative bias temperature instabilities (NBTI) are considered as major reliability issues in metal-oxide-semiconductor field effect transistors (MOSFETs), affecting the threshold voltage, drive current and mobility of the devices. NBTI in HfO₂, HfON and HfSiON-based

MOSFETs are investigated, with an emphasis on the impact of Hf and N content on device degradation. It is shown that an optimal Hf content of about 50 at.% results in reduced NBTI, which is attributed to the competition between increasing density of defect precursors and slower diffusion of hydrogen species with increasing amount of Hf. On the other hand, increasing the concentration of nitrogen in the high-k stack results, like in SiON-based devices, in enhanced NBTI. The experimental results are modeled considering the generation of interface defects, within the reaction-dispersive proton transport model, as well as the creation of bulk traps in the high-k layer. The partial recovery of device degradation, when the electrical stress is interrupted or the gate voltage is switched, is next studied. The recovery implies both partial interface states annealing, possibly via atomic hydrogen or proton re-passivation, as well as bulk defect reduction, resulting from hole (thermally and field assisted) de-trapping in the high-k gate stack.

2:00 PM G8.2
Electron Spin Resonance Observation of Si/Dielectric Interface Traps in Fully Processed Metal Gate Hafnium Oxide Field Effect Transistors. Thomas G. Pribicko¹, Jason P. Campbell¹, Patrick M. Lenahan¹ and Wilman Tsai²; ¹Engineering Science, Pennsylvania State University, University Park, Pennsylvania; ²Intel Corporation, Santa Clara, California.

The alternative high-k gate dielectric, hafnium oxide, is arguably the leading candidate for SiO₂ replacement in future MOS transistors. Using a very sensitive electron spin resonance (ESR) technique, spin dependent recombination (SDR), we have investigated dominating (100) Si/HfO₂ interface defects on fully processed metal/gate transistors. Transistor SDR spectra display a g-value of 2.0051 +/- 0.0003 when the magnetic field is perpendicular to the (100) Si surface. Although sample rotation in the magnetic field alters the average g-value, we are as yet unable to clearly resolve the SDR pattern into the several anticipated lines. The observed defects appear to be similar to, but probably not identical to a P_{b0} center, an unpaired electron strongly localized on a single silicon atom back bonded to three other silicon atoms at the Si/SiO₂ interface. The observed spectra may be a superposition of P_{b1-} and P_{b0}-like centers. We find that the densities of these defects may be altered greatly by gate dielectric stressing. After in-situ gate voltage stressing at modest gate voltages, we observed that the SDR amplitude of the (100) Si/HfO₂ interface P_b-like defect increases with the application of an increasing gate voltage. A hysteretic behavior in the SDR response was observed when modest negative and positive voltages were applied to the gate. This hysteretic result suggests that the application of modest gate voltages changes the chemical/physical nature of the observed defect, but does not eliminate electronic activity or paramagnetism. Work at Penn State was supported by the Semiconductor Research Corporation through Intel Corporation Funding.

2:15 PM G8.3
Interface and Defect States at Ultrathin SiO₂-HfO₂-SiO₂-Si Junctions. Mykola Bataiev¹, Sergey P. Tumakha¹, Yuri M. Strzhemechny¹, Stephen H. Goss¹, Leonard J. Brillson¹, Chris L. Hinkle² and Gerry Lucovsky²; ¹Electrical & Computer Engineering, Physics, and Center for Materials Research, The Ohio State University, Columbus, Ohio; ²Physics, North Carolina State University, Raleigh, North Carolina.

We have used low energy electron-excited nanoscale luminescence spectroscopy (LEEN), a low energy form of cathodoluminescence spectroscopy, to probe the interface states at ultrathin layers of SiO₂ and HfO₂ deposited by a remote plasma process on remote plasma-processed Si-SiO₂ substrates. HfO₂ is a leading alternative dielectric material for reducing direct tunneling in metal oxide semiconductor (MOS) devices. This is due to its increased dielectric constant K compared to SiO₂ and a significant reduction in tunneling current with respect to SiO₂ with the same equivalent oxide thickness. Critical to use of such structures is the reduction of interface defect densities that could introduce fixed charge that degrades threshold voltages and reduces field effect control. Currently, the only measurements of such states involve indirect transport and capacitance methods and show interface state densities of 10¹² cm⁻², far from state-of-the-art. Here we provide direct measurements of optical transitions involving deep localized energy states inside these ultrathin dielectrics and at their internal interfaces. We employed incident electron beam energies of 0.5 - 3.5 keV to probe 5 nm SiO₂/15 nm HfO₂/5 nm SiO₂/Si dielectric stacks in ultrahigh vacuum (UHV) with corresponding probe depths ranging from the outer SiO₂ layer to the Si substrate. These results revealed the presence of defect luminescence bands at 2.75 eV and 1.90 eV within the SiO₂ and at their interfaces with HfO₂. LEEN spectra also exhibited two non-SiO₂-related spectral peaks at 3.5 eV and 4.2 eV associated with the HfO₂ thin film and its interfaces with SiO₂. These assignments are confirmed by measurements on thick HfO₂. For the as-grown