

Nanoscale Germanium MOS Dielectrics—Part I: Germanium Oxynitrides

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Abstract—In this paper, nanoscale germanium (Ge) oxynitride dielectrics are investigated for Ge MOS device applications. The synthesizing methodology and physical properties of these oxynitride films have been examined first. Basic electrical characteristics have been acquired on metal-gated MOS capacitors with Ge oxynitride dielectric on substrates with different dopant types and crystal orientations. Using an optimized oxidation and nitridation recipe, high-quality Ge MOS capacitors with a minimal frequency dispersion and capacitance–voltage hysteresis have been demonstrated. In addition, the Ge oxynitride dielectric–substrate interface has also been analyzed with the combined low-frequency–high-frequency capacitance method that revealed a substantial reduction of interface trap density after the forming gas anneal. An asymmetric interface trap density distribution within the Ge bandgap has been mapped out, which might explain the inferior n-channel Ge MOSFETs with oxynitride dielectric. An abnormality in the general gate leakage behavior has been observed and found to originate from a transient charge-trapping effect.

Index Terms—Germanium (Ge), grown dielectric, MOS devices, oxynitride, surface cleaning, surface passivation.

I. INTRODUCTION

SILICON (Si) has been the most important semiconductor material in the modern electronic industry since the 1960s primarily due to the very high quality of its native oxide for surface passivation. After over 40 years of miniaturization, the scaling of classical bulk Si MOSFETs is approaching many fundamental limits, which mandates the integration of novel materials and innovative device structures [1] to continue the historic progress in information technology.

Among the various high-mobility channel candidates, germanium (Ge) has recently been suggested [1]–[4] to alleviate the problem of MOSFET drain–current saturation by providing a higher source injection velocity [5]. Historically, Ge had been one of the most important semiconductors, and the instability of native Ge oxides (GeO_x) was one of the key enablers in the first (point-contact) transistor demonstration [6].

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Conversely, its inferior properties, especially when compared to silicon dioxide (SiO_2), make this dielectric unsuitable for Ge MOSFET gate insulation and integrated circuit (IC) field isolation and has therefore prevented very large scale integration (VLSI) of Ge devices in the past.

Over the last four decades, a variety of grown and deposited dielectric approaches have been suggested for Ge MOS applications. Gate-quality germanium dioxide (GeO_2) dielectrics have been grown by wet chemical oxidation [7], thermal oxidation [8], [9], electron cyclotron resonance plasma oxidation [9], vacuum ultraviolet-assisted oxidation [10], as well as remote plasma oxidation [11]. To improve their thermal and chemical stability, either thermal nitridation [12] or plasma anodic nitridation [13] was applied to transform the Ge oxides to Ge oxynitrides (GeO_xN_y). Alternatively, several different deposited dielectrics have been attempted including SiO_2 [14], SiO_2 on a thin Si cap [15], silicon nitride (Si_3N_4) [16], [17], GeO_2 [17], germanium nitride (Ge_3N_4) [17], [18], aluminum oxide (Al_2O_3) [19], and aluminum-phosphorus oxide (AlP_xO_y) [20]. Nevertheless, none of these approaches has been previously shown to hold promises as a dielectric for nanoscale Ge MOSFETs.

Before the interest in Ge as a channel material for deca-nanoscale MOSFETs could be facilitated, a stable as well as scalable gate dielectric technology has to be developed. In this paper (Part I), we have investigated the grown GeO_xN_y , and in a companion paper (Part II), the deposited high-permittivity metal oxides, as nanoscale Ge MOS dielectric candidates. In this paper, we first present the GeO_xN_y synthesis and their physical properties. Then, we report their basic electrical characteristics on the fabricated metal-gated MOS capacitors. Finally, the $\text{GeO}_x\text{N}_y/\text{Ge}$ interface properties and the general gate leakage behavior from these MOS capacitors are analyzed.

II. GERMANIUM OXYNITRIDE SYNTHESIS AND PROPERTIES

Among all the grown dielectric approaches listed in Section I, thermal nitridation of the intentionally grown Ge oxides is apparently the most promising and accessible technique. As the first step toward the GeO_xN_y synthesis, different methods for Ge surface oxidation including thermal oxidation, native oxidation, and chemical oxidation were studied as listed in Table I. Before either thermal or chemical oxidation, the surface native GeO_x was first removed by a diluted hydrofluoric acid (HF).

TABLE I
DIFFERENT GERMANIUM PREOXIDATION TREATMENTS
AND SURFACE OXIDATIONS

Sample number	(i)	(ii)	(iii)	(iv)
Pre-oxidation treatment				
Reagent	50:1 HF	-	50:1 HF	50:1 HF
Duration (s)	30	-	30	30
Surface oxidation				
Type	thermal	native	chemical	chemical
Reagent	dry O ₂	air	30% H ₂ O ₂	conc. HNO ₃
Temperature (°C)	500	20	20	20
Duration (min)	8	-	1	1

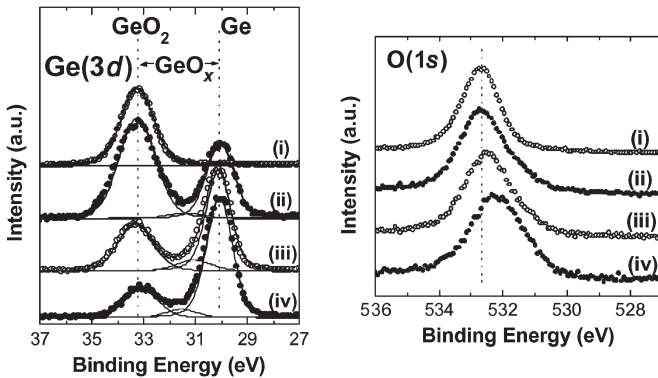


Fig. 1. Core-level Ge(3d) (left) and O(1s) (right) XPS on differently prepared Ge surface oxides: (i) thermal oxide, (ii) native oxide, (iii) H₂O₂ chemical oxide, and (iv) HNO₃ oxide. The Ge surfaces were HF cleaned prior to oxidation [except on sample (ii)].

Core-level Ge(3d) and O(1s) X-ray photoemission spectra (XPS) were taken on different Ge oxides as plotted in Fig. 1. To analyze the chemical bonding nature and stoichiometry of these oxides, Ge(3d) signals were further peak fitted assuming the existence of Ge, GeO_x, and/or GeO₂ configurations. Because the thermal oxide on sample (i) was relatively thick, the substrate elemental Ge peak (with binding energy ~ 30 eV) was absent given its small photoelectron escape depth. On the other hand, the elemental Ge peak was observed on samples (ii)–(iv) as these native and chemical oxidations are usually self-limiting. Due to the absence of the elemental peak (i.e., common reference) from the spectrum on sample (i), it should be primarily used for relative comparison with other spectra on oxide stoichiometry. Nonetheless, from both the Ge(3d) and O(1s) spectra, the bulk of the thermal oxide (i) was mainly composed of stoichiometric GeO₂, whereas the other samples consisted of a mixture of GeO₂ and GeO_x. Moreover, the relative intensity ratio of GeO₂ to GeO_x is lower for the chemical oxides prepared with either hydrogen peroxide (H₂O₂) (iii) or nitric acid (HNO₃) (iv), whose sub-stoichiometry may generate high density of trap states at the dielectric–substrate interface. These interface states could eventually induce charge trapping and detrapping (i.e., hysteretic current–voltage behavior) and MOSFET channel carrier scattering (i.e., mobility and drive current degradation). The thermal oxide was thereby chosen for subsequent nitridation to engineer the high-quality GeO_xN_y, with both processes carried out in a commercial rapid thermal processing (RTP) system.

The starting substrates used to synthesize GeO_xN_y were (100)-oriented n-type Ge wafers with a net background dop-

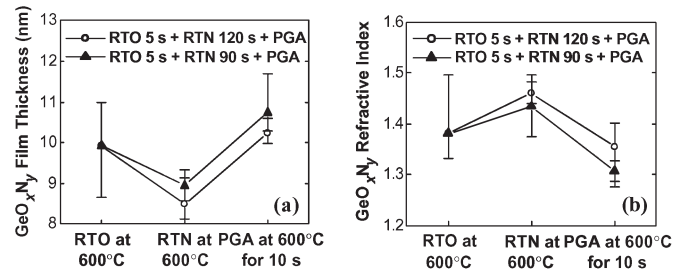


Fig. 2. (a) GeO_xN_y film thickness and (b) refractive index estimated using optical ellipsometry after various rapid thermal processes.

ing concentration of $\sim 7 \times 10^{15}$ cm⁻³. These substrates were first cleaned by a cyclic rinsing between deionized (DI) water and HF [21] to remove native GeO_x. The HF concentration employed was 50:1, and the rinse time was 15 s in each chemical for a total duration of 150 s. The cyclic HF (CHF) cleaning was finished with a 10 s DI water rinse for chemical safety reasons. The cleaned Ge substrates were then blown dry with nitrogen gas (N₂) and immediately loaded into the RTP system.

The GeO_xN_y formation experiments [22] consisted of an initial rapid thermal oxidation (RTO) at 500 °C–600 °C with a soak time of 5–120 s in dry oxygen (O₂) to form GeO₂ followed by an *in situ* rapid thermal nitridation (RTN) at 600 °C with a soak time of 1–5 min in ammonia (NH₃) ambient to convert the oxides into oxynitrides. NH₃ was chosen as the nitriding agent due to its ability to incorporate more nitrogen (N) into the oxynitride film over other species like nitrous oxide (N₂O) or nitric oxide (NO), as inferred from their behavior on Si oxides [23]. During oxynitridation, the rapid thermal ramp rates were set to 100 °C/s for both RTO and RTN, and the wafer temperature was brought down to room temperature prior to RTN. On selected samples, an *in situ* postgrowth anneal (PGA) at 600 °C for 10 s in dry O₂ was performed. The change in GeO_xN_y film thickness and refractive index during the entire process was monitored using optical ellipsometry. For example, as shown in Fig. 2, the GeO_xN_y film thickness decreased, whereas the refractive index increased after the RTN treatment following the initial 5 s RTO step. Both phenomena could be explained by the increased coordination between Ge and O atoms through N incorporation, with longer RTN soak time giving denser coordination that resembles the Si oxynitridation experience [24]. The optional PGA thickened the GeO_xN_y by additional surface Ge oxidation, diluted the N concentration within the GeO_xN_y film, and thereby reduced the Ge and O atom coordination. It is worth noting that because a uniform single-layer model was employed in the ellipsometry calculations, finite amount of errors would be expected [9]. In addition, our calculated refractive indexes were slightly lower than those reported on GeO₂ and GeO_xN_y films [7], [10], [12], [13] because the latter were grown using higher thermal budgets and/or with better N incorporation.

Finally, angle-resolved XPS (AR-XPS) was employed to qualitatively depth-profile the N content within the GeO_xN_y layer [22]. The XPS signals were first peak fitted around the N(1s) and O(1s) binding energies, and the extracted intensities

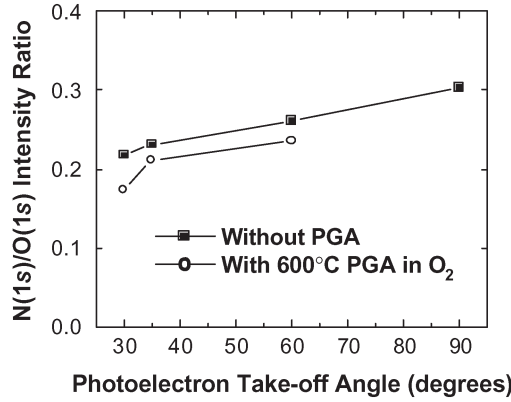


Fig. 3. XPS intensity ratios of N(1s) to O(1s) signals measured by AR-XPS on two typical GeO_xN_y films (grown by RTO at 600 °C for 5 s followed by RTN at 600 °C for 120 s) with and without PGA.

were normalized by their corresponding sensitivity factors. Fig. 3 illustrates the intensity ratio of N(1s) to O(1s) signals measured on two typical GeO_xN_y films (grown by RTO at 600 °C for 5 s followed by RTN at 600 °C for 120 s) with and without PGA. On both films, the N(1s)/O(1s) intensity ratio increases gradually with the increasing photoelectron takeoff angle measured from the surface; in other words, more N is piled up near the bottom $\text{GeO}_x\text{N}_y/\text{Ge}$ interface (rather than near the top surface) and raises the local dielectric permittivity (κ). In addition, the oxygen PGA at 600 °C lowered the N concentration and caused a slight change in the N depth profile within the GeO_xN_y film. In general, the scalability of GeO_xN_y can be improved by incorporating more N. One such strategy is to reduce the initial thermal oxide thickness so as to trim down the resultant lower- κ top surface portion of GeO_xN_y ; an alternative scheme could be enhancing the degree of nitridation (e.g., lengthening the RTN soak time and raising the NH_3 flow rate) and eliminating the optional oxygen PGA.

III. BASIC MOS ELECTRICAL CHARACTERIZATIONS

MOS capacitors were subsequently fabricated using these GeO_xN_y films to examine their dielectric bulk and $\text{GeO}_x\text{N}_y/\text{Ge}$ interface electrical qualities. Utilizing the same surface precleaning and oxynitridation recipe described in Section II, GeO_xN_y films were grown on both (100)- and (111)-oriented p- and n-type Ge substrates. No *in situ* oxygen PGA was performed to obtain a higher resultant dielectric permittivity. Next, gate electrodes of various sizes were formed by electron beam evaporation of approximately 70 nm of tungsten (W) through a shadow mask. Aluminum (Al) was then evaporated on the wafer backside to reduce the sample contact (and series) resistance. Finally, on the completed $\text{W}/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitor stacks, a forming gas (H_2/N_2) anneal was carried out at 300 °C for 30 min. This forming gas anneal treatment was selected to rectify the abnormal flat-band voltage (V_{FB}) shift originated from the radiation charging during W evaporation [22].

Capacitance–voltage (C – V) and conductance–voltage (G – V) characteristics were measured on these GeO_xN_y MOS capacitors using the HP4275A multifrequency inductance–

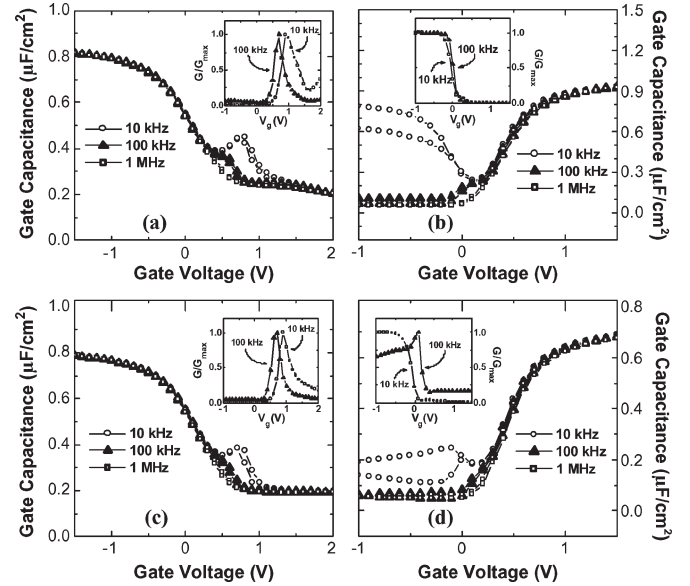


Fig. 4. Multifrequency bidirectional C – V characteristics measured from forming-gas-annealed $\text{W}/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors fabricated on Ge substrates with different doping types and orientations. The insets capture the corresponding G – V measurements. (a) p-Ge (111). (b) n-Ge (111). (c) p-Ge (100). (d) n-Ge (100).

TABLE II
ELECTRICAL PARAMETERS EXTRACTED FROM GERMANIUM OXYNITRIDE MOS CAPACITORS

Doping type & orientation	<i>p</i> -(111)	<i>p</i> -(100)	<i>n</i> -(111)	<i>n</i> -(100)
Doping concentration (cm^{-3})	5×10^{17}	3×10^{17}	1×10^{16}	1×10^{16}
CET from 100 kHz C – V (nm)	4.24	4.40	3.72	5.06
Flat-band voltage (V)	-0.05	0.01	0.27	0.32
C – V hysteresis (mV)	15	16	45	35
Interface trap level density ($\text{cm}^{-2}\text{eV}^{-1}$)	5×10^{12}	4×10^{12}	5×10^{12}	3×10^{12}

capacitance–resistance (LCR) meter. Because the amount of accumulation capacitance dispersion versus measurement frequency was negligible from most of the samples, we extracted the capacitance equivalent thickness (CET) from the 100-kHz C – V data. Fig. 4 shows the bidirectional C – V measurements on the $\text{W}/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors with the GeO_xN_y films grown by RTO at 600 °C for 15 s followed by RTN at 600 °C for 5 min. Although an identical surface cleaning and oxynitridation condition was exerted, the extracted electrical parameters from various substrates indicated some differences as well as similarities as summarized in Table II.

On one hand, the CET difference between the (111)- and (100)-oriented samples is very small for p-type substrates, but this mismatch becomes substantial on n-type substrates given their comparable doping levels. Moreover, the (111) samples deliver a lower CET value than the (100) samples even though the oxidation rate should be higher on the (111) surfaces [25]. Therefore, this counterintuitive observation should be accompanied with an enhanced nitridation of the (111) oxides, which may suggest either a better penetration of N atoms into the (111) oxides for oxygen replacement or a higher level of nitridation due to the larger number of available surface atoms than on the (100) surfaces. Furthermore, the slightly smaller V_{FB} observed on the (111) substrates for both doping types could be related to a lower amount of negative fixed charges within the dielectric.

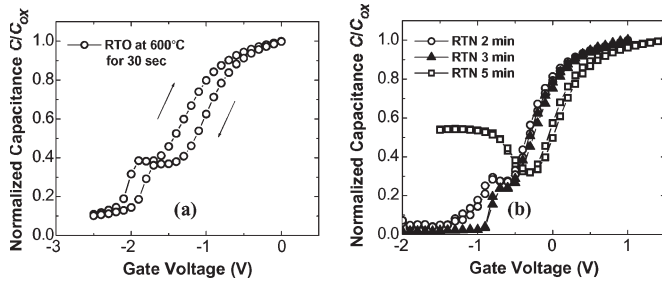


Fig. 5. Normalized bidirectional $C-V$ characteristics measured at 10 kHz from as-grown (a) $W/GeO_2/Ge$ and (b) $W/GeO_xN_y/Ge$ capacitors.

Besides, the n-type substrates tend to produce relatively more $C-V$ hysteresis than the p-type counterparts. As a result, any Ge p-channel MOSFETs with GeO_xN_y dielectric might be slightly more prone to channel carrier loss due to interface charge trapping. Additionally, the interface trap level densities (D_{it}) on the order of 3×10^{12} to $5 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ were preliminarily determined using the Terman method [26] from the 1-MHz curves showing a higher D_{it} value on the (111) surfaces than on the (100) surfaces. These GeO_xN_y/Ge interface trap level properties are further analyzed in the next section.

On the other hand, the major sources of ac small-signal energy loss (i.e., increase in equivalent conductance) in these GeO_xN_y MOS capacitors during the $C-V$ measurements can be identified from the corresponding $G-V$ measurements [27]. Usually, the shape of these $G-V$ curves could also be used to explain any deviations from the ideal $C-V$ behavior. As shown in the insets of Fig. 4, for instance, the equivalent parallel conductance captured on the p-type Ge substrates goes through a peak in weak inversion and drops to a low value in strong inversion. These conductance peaks are indicative of small-signal energy loss dominated by generation and recombination through interface trap levels, which coincide with the humps observed in the $C-V$ traces at the same applied gate voltage. On the n-type Ge substrates, however, the small-signal energy loss constitutes mainly of generation and recombination through bulk trap levels as the $G-V$ curves do not peak up as a function of gate bias in weak inversion. The variation of the measured conductance with gate bias is mainly due to the corresponding variation of capacitance [27]. This gate-bias-independent loss process also matches well with the characteristic “low-frequency” behavior observed in the high-frequency $C-V$ traces. Alternatively, the presence of a negative fixed charge within the GeO_xN_y dielectrics could deplete the n-type Ge surface (except underneath the capacitor electrode areas) and supply positive carriers for channel inversion [27]. This periphery effect, however, could be isolated from the former bulk trap argument by using grounded guard rings or standard field isolation, which will be the subject of the next experiment.

After the acquisition of the baseline electrical characteristics on the GeO_xN_y dielectrics, we have further examined the effects and degree of nitridation on their MOS capacitor behavior. Fig. 5 depicts the normalized bidirectional $C-V$ characteristics measured at 10 kHz from as-grown $W/GeO_2/Ge$ and $W/GeO_xN_y/Ge$ capacitors on (100)-oriented Ge substrates. The GeO_2 film was grown by RTO at 600°C for 30 s, and the GeO_xN_y layers were formed by RTO at 600°C for

5 s followed by RTN at 600°C for 2–5 min. The $C-V$ data were normalized with respect to their individual maximum accumulation capacitances to simplify the comparisons of the V_{FB} value and the bidirectional hysteresis. Only the 10-kHz data are displayed for easy exposure of any abnormal $C-V$ behavior.

After nitridation of the GeO_2 to form GeO_xN_y [Fig. 5(b)], a drastic reduction in the $C-V$ hysteresis is obtained, which proves its effectiveness in decreasing the amount of interface charge trapping over the inferior quality GeO_2 [Fig. 5(a)]. This conclusion is still valid even after normalizing these hysteresis amounts to their corresponding CET values. Indeed, the D_{it} values extracted from the 1-MHz $C-V$ curves (not shown) also decreased after nitridation. However, the degree of nitridation in GeO_xN_y should be well optimized before the real benefit can be discerned. For instance, Fig. 5(b) captures the $C-V$ characteristics of different GeO_xN_y with identical RTO conditions and varying RTN soak time, while keeping the same RTN temperature and NH_3 flow rate. When the RTN soak time was increased from 2 to 3 min, the kink existed near inversion shrank, and the V_{FB} shifted slightly toward the positive voltage direction. Once the soak time was further extended to 5 min, the inversion capacitance shot up to approximately half of the accumulation capacitance (C_{ox}), indicating an efficient carrier generation near the excessively nitrided GeO_xN_y/Ge interfaces. Although, the appearance of this “low-frequency” behavior is not unexpected from the Ge substrate, which has a high intrinsic carrier concentration and a short minority carrier response time [28], this overnitridation additionally led to an increased interface charge trapping and a negative fixed charge generation within the dielectric. These adverse effects may ultimately degrade the channel carrier mobility due to scattering.

IV. DIELECTRIC-SUBSTRATE INTERFACE ANALYSES

Of crucial importance to the MOS device performance, the GeO_xN_y/Ge interface trap level properties could be characterized by using a variety of techniques. The Terman method was previously employed to calculate D_{it} , which, however, necessitates a theoretical computation of the semiconductor surface capacitance and a measurement of the device doping profile. The second well-known technique is the conductance method in the depletion or weak inversion biasing [27] but requires a broader frequency range beyond our measurement system capability (i.e., 10 kHz–10 MHz). Among other classical techniques, the combined low-frequency–high-frequency capacitance method [29] is particularly simple and accurate for our GeO_xN_y/Ge interface analyses.

To illustrate the D_{it} extraction procedure, we synthesized $W/GeO_xN_y/Ge$ capacitors with the GeO_xN_y films grown by RTO at 600°C for 10 s followed by RTN at 600°C for 5 min and without PGA on (100)-oriented p- and n-type Ge substrates. On these capacitors, quasi-static $C-V$ measurements were carried out using the HP4140B pA meter/dc voltage source through the following relation:

$$C_{QS} = \frac{1}{\partial V / \partial t} \quad (1)$$

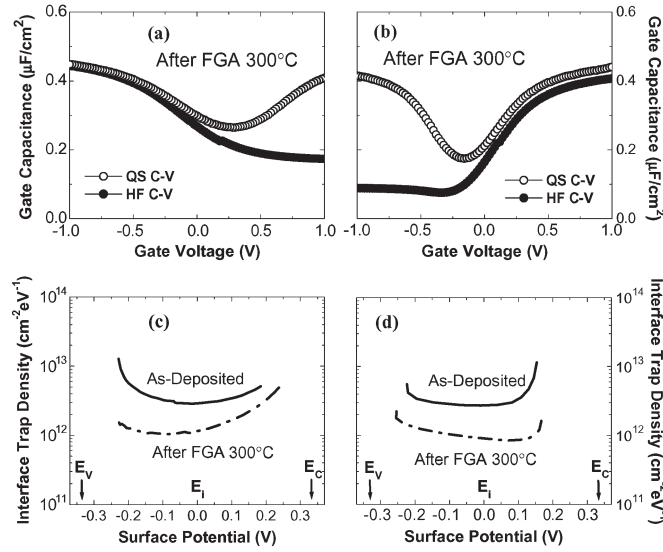


Fig. 6. Unidirectional quasi-static and high-frequency C - V characteristics measured from forming-gas-annealed $W/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors fabricated on (100)-oriented (a) p-type and (b) n-type Ge substrates. The corresponding interface trap level densities were extracted against the Ge surface potential on (c) p-type and (d) n-type Ge substrates before and after the forming gas anneal.

where C_{QS} is the quasi-static capacitance, I is the measured current value, and $\partial V/\partial t$ is the gate-biasing voltage ramp rate; a ramp rate of 0.1 V/s was employed. The unidirectional quasi-static and high-frequency (1 MHz) C - V characteristics are plotted together in Fig. 6(a) and (b) from both p- and n-type Ge substrates, and without loss of generality, only the postforming gas anneal data are shown. The C - V curves on the p-type Ge substrate appear to be more stretched out than the n-type counterparts primarily due to the higher p-type doping concentration (i.e., $3 \times 10^{17} \text{ cm}^{-3}$ for p-type and $2 \times 10^{16} \text{ cm}^{-3}$ for n-type) rather than an intrinsically higher D_{it} value. After combining both the quasi-static and high-frequency C - V measurements, D_{it} was computed with

$$D_{\text{it}} = \frac{C_{\text{ox}}}{q} \left(\frac{C_{\text{QS}}/C_{\text{ox}}}{1 - C_{\text{QS}}/C_{\text{ox}}} - \frac{C_{\text{HF}}/C_{\text{ox}}}{1 - C_{\text{HF}}/C_{\text{ox}}} \right) \quad (2)$$

where q is the electronic charge, and C_{HF} is the high-frequency capacitance. Equation (2) gives D_{it} over only a limited range of the bandgap, typically from the semiconductor flat-band condition to the onset of inversion ($2\psi_B$).

Fig. 6(c) and (d) shows the extracted D_{it} as a function of the Ge surface potential before and after a forming gas anneal at 300 °C for 30 min. The surface potential axes (i.e., x -axes) were labeled with the convention that 0.0 V represents the midgap position (E_i); a positive potential samples the upper half of the bandgap toward the conduction band edge (E_C), and a negative value explores the lower half of the bandgap toward the valence band edge (E_V). The plotted surface potential span was, in fact, less than the Ge bandgap as we were not mapping the D_{it} near either the E_C or the E_V edge. Because the surface potential calculations are usually subjected to errors such as doping and interface charge nonuniformities [27], the relative D_{it} distributions within the bandgap should be interpreted qualitatively.

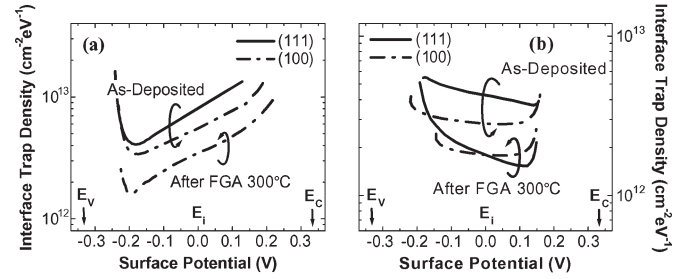


Fig. 7. Interface trap level densities extracted from $W/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors fabricated on (a) p-type and (b) n-type Ge substrates with different orientations before and after the forming gas anneal. The corresponding C - V and G - V characteristics are shown in Fig. 4.

The as-deposited D_{it} level was around $3 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ on both p- and n-type Ge substrates. After the forming gas anneal, the D_{it} level dropped by approximately a factor of 3 to roughly $1 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ on both substrates.

Because the low-frequency-high-frequency capacitance method is more accurate in sampling D_{it} from surface depletion to inversion but constitutes large errors between depletion and accumulation [27], the D_{it} distributions measured on p- and n-type substrates are not identical as similarly reported by others [30]. Therefore, a more representative D_{it} mapping within the bandgap should comprise the data on both substrates with the upper-half (lower-half) bandgap D_{it} taken from the p-type (n-type) sample. By comparing the upper-half D_{it} [Fig. 6(c)] to the lower-half D_{it} [Fig. 6(d)] after the forming gas anneal, one can perceive a relatively higher D_{it} level within the upper half of the bandgap, which has been similarly reported to be composed of acceptor-type states at the hafnia/Ge [30] and hafnia/nitrided Ge [31] interfaces. This important observation may help to explain the asymmetric electron and hole mobility degradation in Ge n- and p-channel enhancement-mode MOSFETs with GeO_xN_y gate dielectrics [4], [32]. In the enhancement-mode MOSFET ON-state, the surface inversion would govern the Fermi level to reside within the upper half of the bandgap in p-type Ge for the n-channel MOSFET (lower half of the bandgap in n-type Ge for the p-channel MOSFET) operation. Therefore, the n-channel carrier (i.e., electron) mobility would tend to be degraded more due to Coulomb scattering [32] with the filled acceptor states present at a higher D_{it} near the E_C edge (versus those states at a lower D_{it} near the E_V edge in n-Ge for hole scattering in the p-channel MOSFET).

Utilizing this combined low-frequency-high-frequency capacitance method, the $\text{GeO}_x\text{N}_y/\text{Ge}$ interface trap level properties were also investigated on the differently oriented substrates discussed in the last section. On the same set of samples whose C - V and G - V characteristics are shown in Fig. 4, the interface trap level densities were extracted before and after a forming gas anneal at 300 °C for 30 min as displayed in Fig. 7. As similarly observed in Fig. 6, the D_{it} levels decreased after the forming gas anneal on both Ge substrate types with either (100) or (111) orientation. The postanneal D_{it} curve from the (111)-oriented p-type Ge substrates could not be acquired because the associated dielectric leakage exceeded that required for a reliable quasi-static C - V measurement.

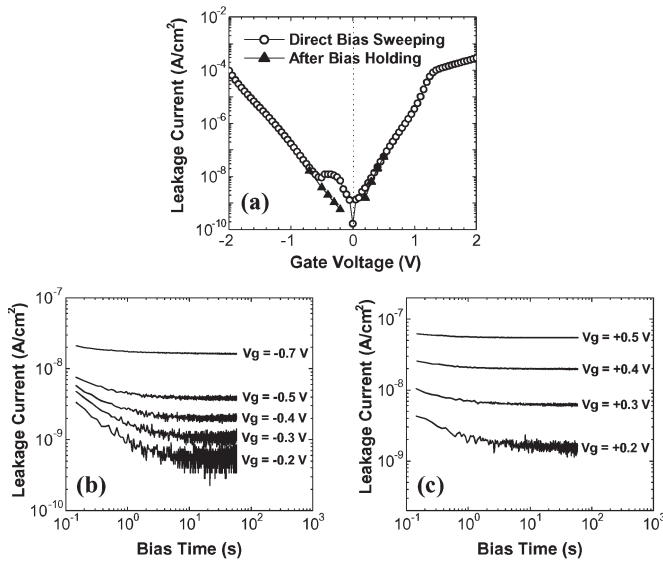


Fig. 8. (a) Gate leakage density as a function of voltage bias measured from typical $W/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors. (b) Corresponding transient leakage currents at negative biasing. (c) Corresponding transient leakage currents at positive biasing.

When the upper-half D_{it} curves from both the (100)- and (111)-oriented p-type Ge substrates [Fig. 7(a)] are compared with the lower-half D_{it} curves from the n-type counterparts [Fig. 7(b)], substantially higher D_{it} levels could be similarly obtained within the upper half of the bandgap that would interfere with the operation of the n-channel enhancement-mode MOSFET as previously explained. Moreover, the (111)-oriented substrates generally possessed a higher D_{it} level than the (100) samples possibly attributed to the larger number of available bonds per unit area on the Ge surface. Because the (111)-oriented Ge surface was theoretically shown, however, to carry higher ballistic current in the n-channel MOSFETs than the (100) surface [33], an interesting study should be highly warranted to contrast the real benefit of employing (111)-oriented Ge surface from both the D_{it} and ballisticity perspectives.

V. DIELECTRIC LEAKAGE BEHAVIOR

The general gate leakage behavior observed from the similar $W/\text{GeO}_x\text{N}_y/\text{Ge}$ capacitors was previously summarized in [22], and the typical gate leakage density as a function of voltage bias is shown in Fig. 8(a). These data were captured from a GeO_xN_y sample grown by RTO at 600 °C for 5 s followed by RTN at 600 °C for 3 min and without PGA on the (100)-oriented p-type Ge substrate. Both the gate and substrate injection leakage characteristics were measured using the HP4155A semiconductor parameter analyzer.

Through a direct gate voltage bias sweeping, the characteristic leakage density pattern [22] was observed with a symmetric leakage level at both positive and negative bias polarities [Fig. 8(a)]. However, there occasionally existed a leakage current hump around the gate voltage of -0.5 to 0 V, which could possibly arise from a transient charge-trapping effect. To verify this proposition, the transient leakage currents were monitored

at selected negative and positive voltage biases as illustrated in Fig. 8(b) and (c), respectively. After approximately 1 min of bias holding, the leakage currents appeared to stabilize at their respective gate voltages, which is an indication that the initially trapped charges are gradually relaxed to restore the normal leakage levels. When these “after bias holding” leakage levels were plotted against those through “direct bias sweeping” [Fig. 8(a)], a more reasonable leakage behavior can be comprehended with a monotonic increase in leakages with increasing bias amplitudes from 0 V. In the companion paper, the GeO_xN_y leakage levels are further benchmarked against those extracted from various high-permittivity metal oxide dielectric stacks on Ge.

VI. CONCLUSION

In this paper, we first discussed the synthesizing methodology of the GeO_xN_y by RTN of the intentionally grown Ge oxides. The resulting GeO_xN_y film thickness, reflective index, N content, and depth profile were examined by optical ellipsometry and X-ray photoemission spectroscopy.

Metal-gated GeO_xN_y MOS capacitors were subsequently fabricated to investigate their basic dielectric characteristics on Ge substrates with different dopant types and crystal orientations. Nitridation of Ge oxides was shown to be useful in lowering the amount of interface charge trapping; however, the degree of nitridation was needed to be well optimized to realize high-quality Ge MOS capacitors with minimal frequency dispersion and C - V hysteresis.

Dielectric-substrate interfaces were also analyzed using the combined low-frequency-high-frequency capacitance method, and the forming gas anneal was found to be effective in reducing the interface trap density. In addition, an asymmetry in the interface trap density distribution within the Ge bandgap was revealed, which helped to explain the inferior n-channel GeO_xN_y MOSFET performance over their p-channel counterparts. Finally, the general gate leakage behavior from these MOS capacitors was reported with an observed abnormality that could be attributed to a transient charge-trapping effect.

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