Nanoscale Germanium MOS Dielectrics—Part II: High-κ Gate Dielectrics

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***Abstract*—In this paper, atomic layer deposition (ALD) and ultraviolet ozone oxidation (UVO) of zirconium and hafnium oxides are investigated for high-κ dielectric preparation in Ge MOS devices from the perspectives of thermodynamic stability and electrical characteristics. Prior to performing these deposition processes, various Ge surface preparation schemes have been examined to investigate their effects on the resulting electrical performance of the Ge MOS capacitors. Interfacial layer-free ALD high-κ growth on Ge could be obtained; yet, insertion of a stable interfacial layer greatly enhanced the electrical characteristics but with a compromise for equivalent dielectric thickness scalability. On the other hand, interfacial layer-free UVO high-κ growth on Ge was demonstrated with minimal capacitance–voltage hysteresis and sub-1.0-nm capacitance equivalent thickness. Finally, the leakage conduction and scalability of these nanoscale Ge MOS dielectrics are discussed and are shown to outperform their Si counterparts.**

***Index Terms*—Germanium, hafnium oxide, high-permittivity dielectric, MOS devices, surface passivation, zirconium oxide.**

I. Introduction

EVEN though the grown germanium oxynitrides (GeO_xN_y) discussed in Part I of this paper could be scaled down to a capacitance equivalent thickness (CET) of 1.9 nm [1], a sub-1.0-nm CET solution is still mandated for Ge MOSFETs to advance beyond the 32-nm technology node [2]. Inspired by the research successes to scale down CET in silicon (Si) MOS devices with the use of high-permittivity (high-κ) metal oxides [3], we previously demonstrated the possibility of applying these high-κ materials onto Ge [4], [5]. Subsequently, variants of this "high-κ dielectric on Ge" concept have been independently realized [6]–[12].

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Usually, the common high-κ dielectric deposition onto Si either requires or produces a lower-κ Si suboxide (SiO_x) interfacial layer between the dielectric film and the substrate [3], which is currently a major bottleneck to scale the CET thinner than 1.3 nm. In comparison, the thermodynamic instability of Ge oxides (GeO_x) may permit a true high-κ gate stack on Ge without a performance-limiting lower-κ interfacial layer and thus overcome the CET scaling barrier.

In this paper, we first identify the high-κ dielectric candidates for Ge MOS device applications according to both the thermodynamic and electrical selection criteria. After which, we present two high-κ metal oxide deposition techniques, namely, 1) atomic layer deposition (ALD) and 2) ultraviolet ozone oxidation (UVO) of metals. Various Ge substrate surface preparations were attempted prior to high-κ dielectric deposition to examine the resultant effects on the fabricated metal-gated MOS capacitors. Finally, the leakage current densities measured from various nanoscale Ge MOS dielectrics are compared, and the scalability of various high-κ gate stacks on Ge is evaluated against their Si counterparts.

II. High-κ Dielectrics Selection Criteria

For a high-κ dielectric material to be chosen to integrate onto Ge for MOS device applications, both the thermodynamic and electrical criteria need to be met simultaneously. Various high-κ candidates including metal germanates (MGe_xO_y) and metal oxides (MO_x) have been considered from the perspective of their thermodynamic stability in contact with Ge, and several stable MGe_xO_y phases were initially identified from the binary phase diagrams of various metal oxide systems [13]. Owing to their complexity, however, we limited our study to the MO_x high-κ candidates for Si and investigated their application to Ge MOS devices. Based on the thermodynamic analysis using a pseudoternary phase diagram [14], the thermodynamic stability of zirconium oxide (ZrO_2) with respect to solid state reaction with Ge can be predicted as illustrated in Fig. 1. This thermodynamic calculation was performed at the nominal high-κ dielectric ALD temperature [15]. The existence of a tie line between ZrO_2 and Ge (Fig. 1), which indicates simultaneous stability of the two phases in contact with one another, results from the large standard Gibbs-free energy of formation ZrO_2 (-1135 kJ/mol) compared to that of GeO_2. Therefore, the solid state reaction between ZrO_2 and Ge should not occur spontaneously. An interfacial layer between the ZrO_2 dielectric and Ge substrate may be avoided under conditions in which the

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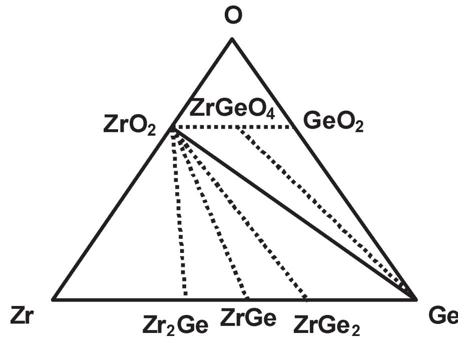

Fig. 1. Calculated Zr/Ge/O ternary phase diagram at 600 K.

deposition process does not produce significant Ge oxidation. Likewise, a similar thermal stability of hafnium oxide (HfO_2) on Ge was predicted for the Hf-Ge-O ternary system at the same ALD reaction temperature.

On the other hand, the electrical behavior of ZrO_2 and HfO_2 dielectrics on Ge is also of great importance. The κ values of these two gate dielectrics were extracted from Si MOS capacitors to be around 30 and 20 for ALD ZrO_2 and HfO_2, respectively [14], which should be effective in leakage suppression compared to grown GeO_xN_y at an equivalent CET. In addition, the conduction band offset (ΔE_C) at the MO_x/Ge interfaces can be computed [16] using the following expression:

$$\Delta E_C = \chi_{\mathrm{Ge}} - \chi_{\mathrm{MO}_x} + (S-1)(\Phi_{\mathrm{CNL,Ge}} - \Phi_{\mathrm{CNL,MO}_x}) \quad (1)$$

where χ_{Ge} and χ_{MO_x} are the electron affinities of Ge and MO_x, respectively, $\Phi_{\mathrm{CNL,Ge}}$ and $\Phi_{\mathrm{CNL,MO}_x}$ are the charge neutrality levels of Ge and MO_x, respectively, and S is an empirical parameter analogous to the Schottky barrier pinning factor in Bardeen's model of metal–semiconductor junctions. Employing the values reported in the literature [17]–[19], the theoretical values of ΔE_C are calculated to be 1.63 and 1.65 eV for ZrO_2 and HfO_2, respectively, which should be sufficiently large to provide an acceptable barrier for leakage conduction. Merging the thermodynamic and electrical qualifications together, both ZrO_2 and HfO_2 should be applicable for future Ge MOS device applications.

III. ALD of High-κ Dielectrics

ALD deposition of high-κ metal oxide dielectrics was carried out in a cold-wall high-vacuum-base-pressure system [14]. ALD is a particularly attractive method for preparing *ultrathin* MO_x layers with excellent electrical characteristics and near-perfect film conformality because of the layer-by-layer nature of the deposition kinetics. A typical ALD process for ZrO_2 or HfO_2 is performed at 300 °C using alternating surface-saturating reactions of water (H_2O) and metal tetrachloride (MCl_4). In our reactor, each precursor is pulsed for 2 s, and nitrogen (N) purging follows for 30 and 60 s after each H_2O and MCl_4 pulse, respectively. The base pressure of the system is $\sim 5 \times 10^{-8}$ Torr, and the process pressure is maintained at 0.5 Torr during ALD.

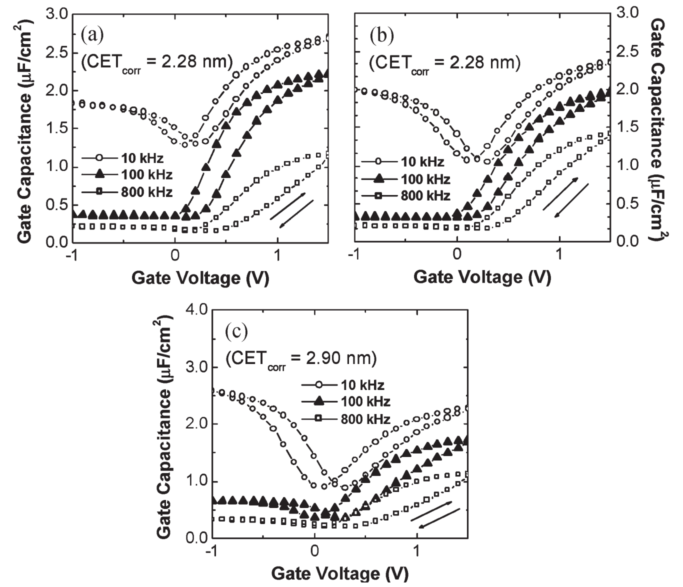

Fig. 2. Multifrequency bidirectional C–V characteristics measured from forming-gas-annealed $Pt/ZrO_2/Ge$ capacitors fabricated on (a) HF-vapor-etched, (b) DI-water-rinsed, and (c) native-oxide-capped Ge surfaces. The corrected CET values were computed from the 100- and 800-kHz traces.

A. ALD of ZrO_2

Because the ALD reaction on differently prepared substrate surfaces could yield high-κ films with various microstructures and electrical qualities, the ALD of ZrO_2 on Ge was investigated on three surfaces, namely:

1) etched for 1 min with hydrofluoric acid (HF) vapor evaporated from a concentrated (49%) aqueous solution;
2) rinsed for an optimized dwell time of 1 min [15] in deionized (DI) water to dissolve the soluble native oxide;
3) capped with a native oxide layer.

The first two preparations were intended to produce a non-hydroxylated Ge surface, and the last was designed to provide surface hydroxylation for the ALD reaction.

The starting substrate used for ALD of ZrO_2 was (100)-oriented n-type Ge wafers with a net background concentration of $\sim 7 \times 10^{15}$ cm^{-3}. The three different surface preparations were applied prior to the ALD of ~ 5.5 nm ZrO_2. Various sizes of 50-nm-thick platinum (Pt) gate electrodes were formed by electron beam evaporation through a shadow mask, and subsequently, aluminum (Al) was evaporated on the wafer backside to reduce the sample contact (and series) resistance. Finally, a forming gas anneal was carried out at 400 °C for 30 min on the completed $Pt/ZrO_2/Ge$ capacitors.

Capacitance–voltage (C–V) characteristics were measured on the MOS capacitors using the HP4284A precision inductance–capacitance–resistance (LCR) meter. On both of the non-hydroxylated [Fig. 2(a) and (b)] and hydroxylated [Fig. 2(c)] Ge surfaces, large bidirectional C–V hysteresis and abnormal inversion behavior could be similarly observed. The

large hysteresis is believed to stem from interfacial defects. For instance, an interfacial layer-free local epitaxial growth of ALD ZrO_2 on HF-vapor-etched Ge surface [20] possesses about 10% lattice mismatch between the tetragonal ZrO_2 and Ge. This results in a significant areal density of interfacial dislocations ($\sim 7 \times 10^{12}$ cm^{-2}) that may be responsible for the electron trapping ($\sim 3 \times 10^{12}$ cm^{-2} estimated from the hysteretic bidirectional C–V traces). Alternatively, the metal impurities diffused into the near-surface Ge substrate [21] would create bulk trap levels that allow efficient generation–recombination of minority carriers responsible for the abnormal inversion behavior. To minimize these problems, an interfacial passivation and diffusion barrier layer could be inserted as discussed in Section III-B.

After correcting for the substrate-resistivity-induced frequency dispersion [22] in the accumulation capacitance (using the 100- and 800-kHz C–V data), CET values of 2.28, 2.28, and 2.90 nm were computed for the HF-vapor-etched, DI-water-rinsed, and native-oxide-capped samples, respectively. Both of the non-hydroxylated surface passivation schemes result in a smaller CET because of their effectiveness at removing the native oxides prior to ALD. Gate leakage current densities were found to be remarkably low and are benchmarked with other dielectric stacks in Section V.

B. ALD of HfO_2

As a leading high-κ dielectric candidate for Si MOS devices, we have also studied the ALD HfO_2 on several Ge surfaces with and without intentional hydroxylation. The starting substrates were (100)-oriented p-type Ge wafers with a net background concentration of $\sim 3 \times 10^{17}$ cm^{-3}. From the ALD ZrO_2 on Ge results, we learned that the native-oxide-capped surface does not yield a good-quality dielectric, possibly due to its instability during the ALD reaction. Stimulated by the high-quality GeO_xN_y/Ge interface discussed in Part I of this paper, we also investigated the possibility of applying a GeO_xN_y interface layer prior to the ALD of HfO_2. Pt-gated HfO_2 capacitors were similarly fabricated as previously described on differently prepared Ge surfaces, namely:

1) cleaned by cyclic rinsing between 50:1 HF solution and DI water for 15 s in each solution for a total duration of 150 s (CHF) to remove both water-soluble and -insoluble native oxides [1], [15];
2) rinsed in DI water for 1 min;
3) capped with thick GeO_xN_y grown by furnace oxidation of CHF-cleaned Ge at 500 °C for 2 min followed by rapid thermal nitridation (RTN) at 600 °C for 1 min in ammonia (NH_3);
4) capped with thin GeO_xN_y grown by RTN at 600 °C for 1 min in NH_3 on CHF-cleaned Ge.

C–V characteristics were extracted from these ALD HfO_2 Ge MOS capacitors using the HP4284A precision LCR meter. After correcting for the substrate-resistivity-induced accumulation capacitance dispersion, the CET values and bidirectional hysteresis normalized to the corresponding CET were excerpted as shown in Fig. 3. As reported and discussed earlier [15],

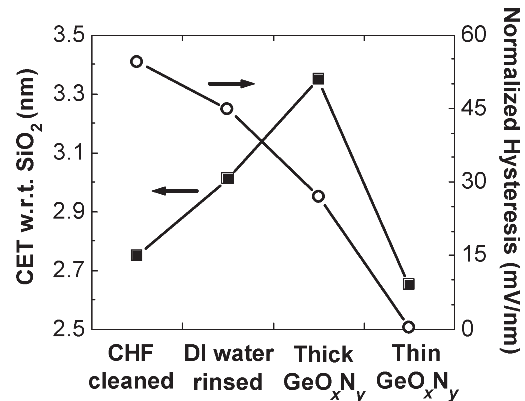

Fig. 3. CET values with respect to SiO_2 and normalized bidirectional C–V hystereses estimated $Pt/HfO_2/n-Ge$ with various surface preparations prior to ALD [15].

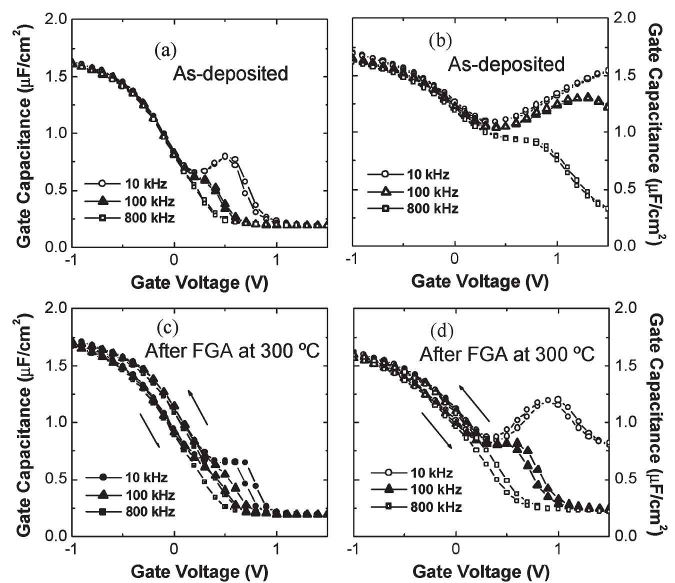

Fig. 4. Multifrequency bidirectional C–V characteristics measured from as-deposited and forming-gas-annealed $Pt/HfO_2/GeO_xN_y/Ge$ capacitors with the GeO_xN_y grown at 600 °C and 700 °C. (a) RTN at 600 °C. (b) RTN at 700 °C. (c) RTN at 600 °C. (d) RTN at 700 °C.

the thin-GeO_xN_y-capped sample yielded the best result (with minimal hysteresis and smallest CET).

To optimize the hydroxylation conditions for ALD of HfO_2 onto Ge, the $Pt/HfO_2/GeO_xN_y/Ge$ capacitor electrical characteristics with different GeO_xN_y RTN temperature were examined before and after a forming gas anneal. When the C–V curves for as-deposited films are compared [Fig. 4(a) and (b)], the 600 °C grown GeO_xN_y interfacial layer revealed minimal hysteresis and frequency dispersion compared to the 700 °C case. The higher RTN temperature degraded the interfacial quality and triggered an inversion capacitance increase (possibly due to generation and recombination through bulk trap levels), which are the characteristic phenomena of overnitridation as observed in Part I of this paper. It is worth noting that this behavior is not believed to result from metal impurity in-diffusion (Section III-A) as medium energy ion scattering (MEIS) data [21] suggest that the GeO_xN_y interfacial layer is

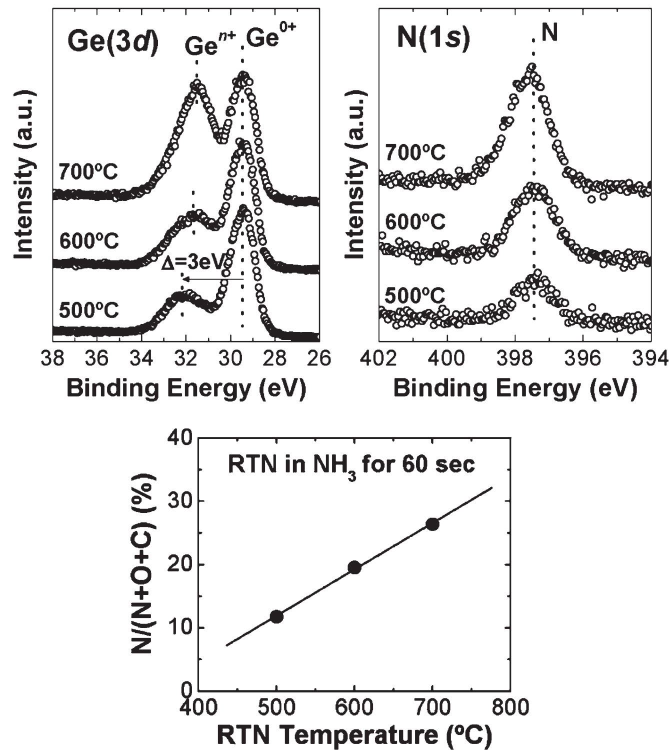

Fig. 5. (Top left) Core-level Ge(3d) XPS spectra, (top right) core-level N(1s) XPS spectra, and (bottom) relative N atomic concentration from the GeO_xN_y films as a function of RTN temperature.

effective in blocking Hf atoms from diffusing into Ge substrate at the process temperatures investigated.

After a forming gas anneal at 300 °C for 30 min, both the 600 °C and 700 °C GeO_xN_y capacitors showed increased bidirectional hysteresis due to hole trapping [Fig. 4(c) and (d)] because of a possible depassivation of the weak Ge–H bonds formed during NH_3 nitridation. Contrary to the typical case of forming gas passivating most of the SiO_2-Si interfacial dangling bonds, the efficacy of forming gas anneals for Ge MOS devices is not obvious. Low gate leakage current densities on these $HfO_2/GeO_xN_y/Ge$ capacitors were observed for both gate and substrate injection, which were relatively independent of the nitridation condition [15].

Finally, physical characterization of the GeO_xN_y interfacial layers was carried out to inspect their N content and chemical stability. X-ray photoemission spectroscopy (XPS) was employed to estimate the N atomic concentration in GeO_xN_y layers grown on CHF-cleaned Ge at various temperatures for 1 min (Fig. 5). Any surface hydrocarbon layer adsorbed during sample transfer in air was also included in the calculation. The relative ratio of N to the sum of N plus carbon (C) and oxygen (O) increases linearly with the RTN temperature from about 10% to 30%. In addition, the oxidized Ge(3d) peak (Ge^{n+}) shifted toward lower binding energy at higher RTN temperatures, which suggests a gradual modification of the Ge bonding configuration. The chemical stability of the GeO_xN_y layer grown at 600 °C was studied by dipping the sample in either a 20:1 HF solution for 1 min or a DI water for 2 min (Fig. 6). After the N incorporation into GeO_x, the

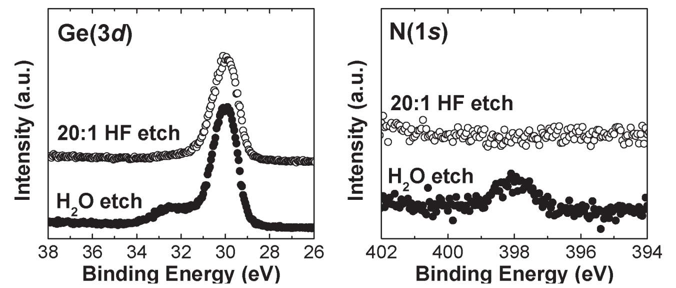

Fig. 6. (left) Core-level Ge(3d) and (right) N(1s) XPS spectra taken on the GeO_xN_y film grown at 600 °C after either a HF or DI water treatment.

resultant GeO_xN_y layer exhibited a drastic reduction in DI water solubility and an enhanced chemical stability, whereas this stabilized GeO_xN_y film can easily be etched away in HF solution—the standard SiO_2 etchant.

Combining both the electrical and physical characterization data, it can be concluded that the insertion of a GeO_xN_y interfacial layer is advantageous for producing high-quality ALD high-κ dielectric stacks on Ge for MOS applications, which is consistent with other reported high-κ deposition results on Ge [6], [8]–[11]. Nevertheless, the scaling of the thin GeO_xN_y interfacial layer has to be carefully studied to offer a sub-1.0-nm CET using either alternative formation techniques or other materials.

IV. UVO OF HIGH-κ DIELECTRICS

As an alternative high-κ dielectric deposition technique, the UVO process offers advantages including very low processing temperatures, low contamination levels, as well as an *in situ* gate electrode capping capability. In this technique, a thin metal (e.g., Zr or Hf) precursor film is first deposited by sputtering on the wafer surface in ultrahigh vacuum (UHV) followed by an *in situ* oxidation in atomic oxygen and ozone, which are co-generated by ultraviolet illumination on high-purity (99.999%) oxygen [23]. The typical UVO process proceeds at an oxygen partial pressure of 600 Torr and a low temperature ($\sim$ 50 °C) for 60 min. Due to the reactive nature of those metal precursors and instability of surface GeO_x, low-permittivity interfacial layer formation may possibly be avoided using this technique as well.

A. *UVO of ZrO_2*

To examine the UVO ZrO_2 quality on differently prepared substrate surfaces, MOS capacitors were fabricated on (100)-oriented n-type Ge wafers with a net background impurity concentration of $\sim 7 \times 10^{15}$ cm^{-3}. Three different surface preparations, as described in Section III-A, were applied prior to UHV sputtering of $\sim$ 2 nm Zr film and then followed by an *in situ* UVO at room temperature. About 50 nm of Pt was subsequently deposited by UHV sputtering as the gate electrode layer and circular capacitor structures were defined by optical lithography and argon (Ar) ion sputter etch. No wafer backside Al was applied to these $Pt/ZrO_2/Ge$ capacitors,

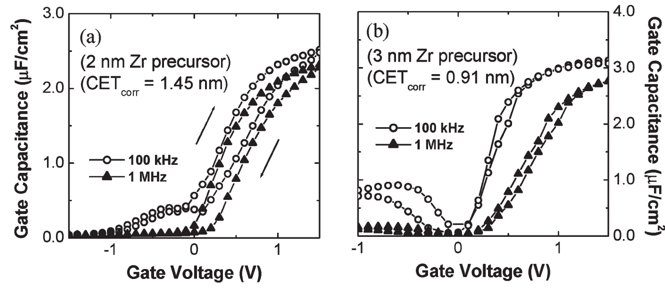

Fig. 7. Multifrequency bidirectional C–V characteristics measured from forming-gas-annealed $Pt/ZrO_2/Ge$ capacitors fabricated on (a) native-oxide-capped and (b) UV Ge-oxide-grown Ge surfaces. The corrected CET values were computed from the 100-kHz and 1-MHz traces.

which were finally subjected to a forming gas anneal at 410 °C for 30 min.

C–V characteristics were measured from these UVO ZrO_2 Ge MOS capacitors using the HP4275A multifrequency LCR meter as shown in Fig. 7. The corresponding CET values were computed after correcting for the substrate-resistivity-induced accumulation capacitance dispersion between the 100-kHz and 1-MHz traces. As reported and discussed earlier [4], very small hystereses, minimal frequency dispersions, as well as sub-1.0-nm CETs were achieved on the HF-vapor-etched and DI-water-rinsed samples whose surface GeO_x had been intentionally stripped.

On the native-oxide-capped sample [Fig. 7(a)], a large C–V hysteresis ($\sim$ 0.3 V), a substantial frequency dispersion, and a relatively large CET were obtained, which may stem from the inferior $ZrO_2/GeO_x/Ge$ interface quality. To further illustrate the importance of the Zr precursor thickness, an additional $Pt/ZrO_2/Ge$ sample was fabricated, whose Ge surface had been intentionally UV-oxidized followed by sputtering a thicker ($\sim$ 3 nm) Zr film and its UVO oxidation. Although the UVO-grown Ge oxides should be thicker than native GeO_x, the thicker Zr precursor produced a thinner CET value, which suggests that the reaction of the thick Zr precursor layer with the underlying oxide produces a substantially different high-κ film and interfacial layer structure than does the thinner precursor layer [Fig. 7(b)]. The frequency dispersion observed, which may be attributed to oxygen deficiency during the UVO oxidation of this thicker Zr precursor layer [24], can be removed by lengthening the UVO process duration.

B. UVO of HfO_2

MOS capacitors were fabricated on a (100)-oriented n-type Ge wafer with a net background concentration of $\sim 7 \times 10^{15}$ cm^{-3}. UVO HfO_2 was prepared on a DI-water-rinsed Ge surface. A nominal thickness of 2 nm of Hf precursor was deposited by UHV sputtering onto the rinsed surface followed by an *in situ* UVO oxidation at room temperature. Finally, the $Pt/HfO_2/Ge$ capacitors were made as described in Section IV-A and subjected to a forming gas anneal at 300 °C for 30 min.

C–V characteristics were measured from these UVO HfO_2 Ge MOS capacitors using the HP4275A multifrequency LCR meter with minimal bidirectional hysteresis and frequency dispersion as shown in Fig. 8. The CET values computed directly from the maximum accumulation capacitance were around 0.6–0.7 nm, which may constitute an underestimation owing to the inherent high-gate-leakage-induced C–V nonsaturation; a better extraction could be attained using quantum–mechanical simulation [25]. Recently, another HfO_2 gate stack on Ge with a sub-1.0-nm CET had also been demonstrated by atomic oxygen beam deposition [10].

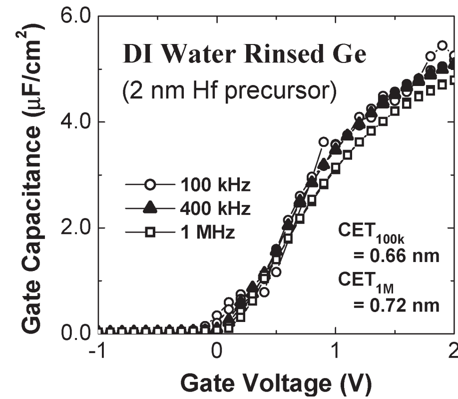

Fig. 8. Multifrequency bidirectional C–V characteristics measured from forming-gas-annealed $Pt/HfO_2/Ge$ capacitors fabricated on DI-water-rinsed Ge surface.

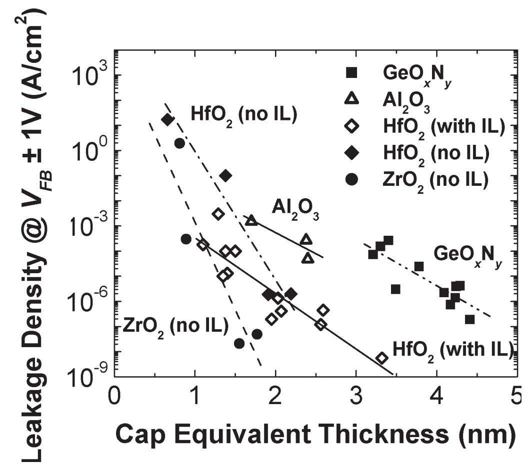

Fig. 9. Benchmarking the gate leakage levels from various nanoscale Ge MOS dielectrics. The CET values were lifted from the 100-kHz C–V data.

In good correlation with the thermodynamic prediction (Section II) and physical characterizations [16], [26], the minimal C–V hysteresis and sub-1.0-nm CETs measured on these UVO ZrO_2 and HfO_2 Ge capacitors unambiguously demonstrated the feasibility of low-permittivity interfacial layer-free high-κ dielectric growth on Ge substrate. Likewise, substantial improvements in electrical performance can be achieved by complete elimination of the poor-quality and readily removed GeO_x interfacial layer, followed by direct high-κ growth on Ge. In addition, the optimized forming gas anneals applied to these UVO Ge capacitors tend to improve electrical characteristics—a phenomenon that is contrary to

TABLE I
KEY COMPARISONS OF THE NANOSCALE Ge MOS DIELECTRICS

Nanoscale Ge MOS Dielectrics	Interface Trap Density	Frequency Dispersion	Gate Leakage	C-V Hysteresis
GeO_xN_y	High	~ 0	High	Very small
ALD High-κ				
without interfacial layer	High	Large	Low	Large
with interfacial layer	Medium-high	~ 0	Low	~ 0
UVO High-κ				
without interfacial layer	Medium-high	Very small	Low	Very small

the depassivation observed in the ALD Ge capacitors (Section III-B). Finally, the gate leakage current densities extracted from these UVO Ge capacitors are benchmarked in the following section.

V. Nanoscale Dielectrics Leakage and Scalability

From both the dielectric leakage and scalability perspectives, it is important to objectively assess the nanoscale Ge MOS gate dielectrics discussed in this paper and those published in the literature [6], [8]–[12], [27]. These dielectric stacks can be classified into five categories, namely:

1) germanium oxynitrides (GeO_xN_y);
2) aluminum oxide (Al_2O_3);
3) hafnium oxide with an intentionally prepared interfacial layer [HfO_2 (with IL)];
4) hafnium oxide without an intentionally prepared interfacial layer [HfO_2 (no IL)];
5) zirconium oxide without an intentionally prepared interfacial layer [ZrO_2 (no IL)].

Reasonable C–V characteristics had been first obtained on the MOS capacitors before their corresponding dielectric leakage data were further analyzed. As one of the most accepted benchmarking strategies, we recorded their leakage density at a voltage bias of 1 V into the accumulation from the flat-band voltage (V_{FB}) to achieve a similar carrier concentration for similar dielectric thickness and substrate doping [17]. In other words, the MOS dielectric leakage was taken at either 1 V above V_{FB} on the n-type substrate or 1 V below V_{FB} on the p-type substrate and then plotted against their respective CET values in Fig. 9.

Although the differences in metal gate electrode workfunction and substrate doping polarity may inevitably introduce errors in this benchmarking effort, a distinct trend can clearly be observed in each of the aforementioned categories. Among them, GeO_xN_y possesses the highest leakage followed by Al_2O_3, HfO_2, and ZrO_2—a sequence that corresponds well with their individual κ values. Even though small-CET HfO_2 stacks can be attained [12] without an intentionally prepared interfacial layer, their electrical qualities are usually not optimal, and they exhibit relatively high leakage current densities. As a result, the strategy of inserting an intentionally prepared interfacial layer has been widely adopted in many HfO_2 gate stacks on Ge [6], [8]–[11], which promises a better electrical performance. However, the added CET from the interfacial layer might limit the ultimate scalability of HfO_2 gate stacks on Ge.

On the other hand, the sub-1.0-nm CET ZrO_2 gate stacks on Ge without an intentionally prepared interfacial layer [4], [12] do reveal promising C–V characteristics and lower leakage current densities than the HfO_2 counterparts. These marked differences could primarily be attributed to the higher κ value of ZrO_2. On those interfacial layer-free local epitaxial ZrO_2 gate stacks on Ge [20], remarkably low gate leakage was evident even in the presence of high interface defect densities and subgrain boundaries. These findings suggest that it may be beneficial to employ crystalline MO_x dielectrics with a closer lattice match to Ge to avoid interfacial misfit dislocation formation.

Compared to many high-κ gate stacks on Si, those on Ge are, in fact, exhibiting a better scalability due to their larger dielectric–substrate conduction band offset [16], [19] and thinner low-κ interfacial layers. In addition to the ultrathin interfacial layer within the ZrO_2 gate stack reported earlier [16], [26], much thinner interfacial layers have been achieved for directly sputtered ZrO_2 [12], reactively sputtered HfO_2 [7], as well as metal–organic chemical vapor deposited HfO_2 [28].

Finally, we summarize in Table I the key comparisons between the nanoscale Ge MOS dielectrics discussed in this paper. Weighing the interface trap density (D_{it}), frequency dispersion, gate leakage, and C–V hysteresis, both the ALD high-κ with interfacial layer and UVO high-κ dielectrics are equally promising. It is worth noting that the D_{it} extraction method discussed in Part I of this paper has limited use on the small-CET high-κ dielectrics because the associated leakage current densities exceed those required for a reliable quasi-static C–V measurement. Instead, their D_{it} levels were determined using the Terman method to be about $2 \times 10^{12}\ \mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$ to $5 \times 10^{12}\ \mathrm{cm}^{-2} \cdot \mathrm{eV}^{-1}$. Therefore, further improvements in the deposition process and interface engineering are required for these gate stacks.

VI. Conclusion

In this paper, we first compared the contending high-κ dielectric candidates to be applied to Ge MOS device applications based on both the thermodynamic and electrical properties selection requirements. ZrO_2 and HfO_2 are promising owing to their thermodynamic stability in direct contact with Ge and the inherent large conduction band offsets between the dielectric and the substrate. Prior to their deposition onto Ge, various surface preparation strategies were employed to

investigate the resultant effects on the fabricated metal-gated MOS capacitors.

ALD of metal oxides and UVO of metal thin films were the two high-κ deposition techniques investigated. Although interfacial layer-free epitaxial growth of ALD high-κ could be obtained, a more stable interfacial GeO_xN_y layer is necessary to produce high-quality Ge MOS capacitors with ALD high-κ dielectrics. This may compromise future dimensional scalability of Ge devices with ALD metal oxide. Next, viable interfacial layer-free UVO high-κ growth on Ge was studied due to the reactive nature of metal precursors and the relative instability of GeO_x surface passivation. Experimental results suggested that ZrO_2 and HfO_2 gate stacks on Ge with minimal C–V hysteresis and sub-1.0-nm CET can, indeed, be achieved with a negligible interfacial layer contribution to the capacitance. In addition, considerable improvements in electrical performance were readily achieved by eliminating the poor-quality interfacial layer followed by direct high-κ growth on Ge.

When the leakage current densities of these nanoscale Ge MOS dielectrics were benchmarked together, an unambiguous trend can be observed in which the higher κ gate insulator gives lower leakage. Compared to similar high-κ gate stacks on Si, these high-κ gate stacks on Ge appear to have better scalability due to their larger conduction band offsets and the relative ease with which thinner low-permittivity interface layers can be produced. Besides our analysis, these advantages have also been reported by researchers worldwide, consolidating the future promise of “high-κ dielectric on Ge” technology.

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