On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates

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***Abstract*—"Conventional" techniques and related capacitance-voltage characteristic interpretation were established to evaluate interface trap density on Si substrates. We show that blindly applying these techniques on alternative substrates can lead to incorrect conclusions. It is possible to both under- and overestimate the interface trap density by more than an order of magnitude. Pitfalls jeopardizing capacitance– and conductance–voltage characteristic interpretation for alternative semiconductor MOS are elaborated. We show how the conductance method, the most reliable and widely used interface trap density extraction method for Si, can be adapted and made reliable for alternative semiconductors while maintaining its simplicity.**

***Index Terms*—III–V, alternative substrates, conductance method, electrical characterization, Ge MOSFET, interface trap density extraction, Nicollian–Goetzberger.**

I. Introduction

To CONTINUE increasing CMOS performance, alternative substrates are presently under consideration [1]. Germanium (Ge), either strained or unstrained, is predicted to provide superior drive current characteristics compared to Si [2]. Recently, a $\sim 3\times$ mobility superior to the universal Si one has been experimentally demonstrated in unstrained Ge-channel pFETs [3]. However, the nonoptimal dielectric–substrate interface remains a hurdle to be overcome for further improvement. Currently, one is working toward a Ge–dielectric interface of sufficient electrical quality [4]–[11]. Similarly, research is ongoing to electrically passivate dielectric interfaces of other semiconductors [12]–[16].

The conductance method [17] is one of the most reliable and commonly adopted interface trap density (D_{it}) extraction techniques used to evaluate the passivation of interfaces. In this paper, we show the interpretation pitfalls jeopardizing capacitance-voltage (*C–V*) interpretation and the application of the conductance method for alternative semiconductors based on the Ge case. We show how the conductance method can be adapted and reassured for alternative semiconductors.

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II. Devices and Experiments

Three groups of devices are analyzed. The first group consists of n-type Ge MOS capacitors with germanium oxynitride (GeO_xN_y) dielectric and W-gates [4] (doping $\sim 1 \times 10^{16}$ cm^{-3}, and area 1.77×10^4 μm^2). Effective silicon dioxide thickness (EOT) is 6.3 nm. The GeO_xN_y is grown by rapid thermal oxidation and consecutive nitridation. The second group of devices considered [5] are Si-passivated Ge pMOSFETs with TaN gates fabricated on n-type Ge-on-Si substrates with a doping level of $\sim 3 \times 10^{16}$ cm^{-3}. After appropriate surface cleaning, six monolayers of Si are deposited in an epi-reactor of ASM International to passivate the Ge surface followed by an ozone oxidation forming 0.4 nm of silicon oxide. Four nanometers of HfO_2 are deposited using atomic layer deposition (ALD). The MOSFETs and capacitors have a gate area of 100 μm^2, 4900 μm^2, resp. The EOT of these MOSFETs is 1.4 nm. The third group consists of n-type and p-type GaAs MOS capacitors with a Gd_2O_3 dielectric. Si doping and Be doping were used to obtain an n- and p-type doping of 1×10^{17} cm^{-2} , resp., in molecular beam epitaxy (MBE) grown 1-μm-thick GaAs layers on high doped p- and n-type GaAs substrates, resp. In an MBE tool, Gd_2O_3 was deposited on a 2×4 As-stabilized surface reconstruction of GaAs at 225 °C from a Gd E-gun cell and oxygen plasma. Pt gate electrodes with an area of 3.14×10^{-4} cm^2 were used. The EOTs extracted from these devices are 3.1–3.8 nm, resp.

The instrumentation used consisted of the Agilent 4294 A impedance analyzer and Agilent B1500 A semiconductor device analyzer. The used frequency range is 1 kHz–2 MHz and the used voltage ranges are within –2 to 2 V.

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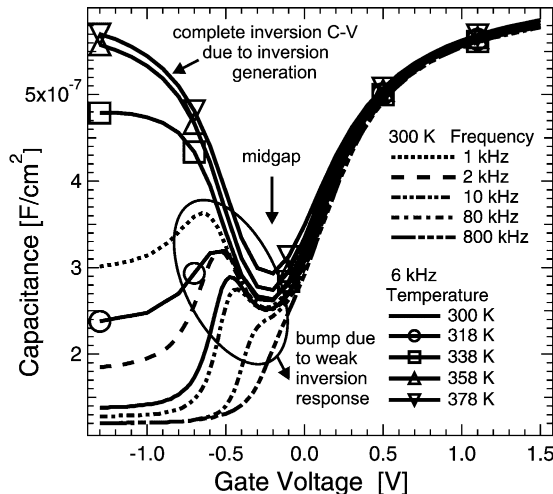

Fig. 1. Temperature and frequency dependence of the n-type GeO_xN_y/Ge *C–V* curve shows a "bump" at low frequency at lower temperature mainly due to a weak inversion response. Inversion generation can also be recognized, especially at higher temperature, where the complete inversion *C–V* characteristic due to inversion generation is present. This shows that the "bump" occurs in weak inversion.

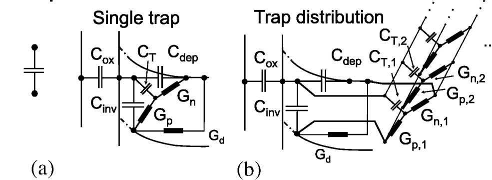

Fig. 2. General equivalent circuit used to model the MOS capacitor *C–V* and *G–V* characteristics across the bandgap for an n-type capacitor. The first circuit (a) models one trap only: C_{ox} is the oxide capacitance, C_{inv} the inversion capacitance, C_{dep} the depletion capacitance, C_T the trap capacitance, and G_n and G_p the electron and hole trap conductances, and G_d models the diffusion-induced inversion generation [17]. (b) For a distribution, a series of Y-circuits is used.

III. First Pitfall: MOS Weak Inversion and Strong Inversion Phenomena

A typical illustration of the first pitfall is the misinterpretation of the commonly observed bumps in Ge *C–V* [6], [10]–[13] (see Fig. 1) as contributions from large D_{it} at depletion bias (case 1). In reality, they can originate from relatively small D_{it} at weak inversion (WI) bias (case 2). The depletion (case 1) and WI (case 2) trap response for Ge are easily confused due to similar *C–V* and *G–V* characteristics at 300 K.

A. Modeling of the MOS Admittance With Interface Traps and Diffusion-Induced Inversion Generation in all Regimes

The Shockley–Read–Hall based theory is used to explain the admittance [measured as a parallel conductance and capacitance, $G + j\omega C$, see Fig. 6(f)] of MOS capacitors in all regimes including the strong inversion and weak inversion regimes.

For low-bandgap (E_g) semiconductors or high temperatures (*T*), an MOS capacitor biased in weak inversion will show an admittance contribution due to interface traps in the minority carrier half of the bandgap. This contribution results from a significant exchange of carriers between traps and both the majority and minority carrier bands at measurement frequencies (*f*) of 1 kHz–1 MHz. This exchange is possible due to the faster capture and emission of carriers. We will refer to this admittance contribution in capacitors as "weak inversion response" which causes the typical "bump" in the Ge *C–V*.

To include the weak inversion response in the model, the general equivalent circuit put forward in [17], Ch. 5 is used. This circuit makes use of Y-circuits representing a single energy level interface trap (see Fig. 2(a) for an MOS capacitor with a single trap). The presence of both G_{n} and G_{p} guarantees modeling of all exchanges of carriers with the minority and majority carrier bands. A continuous interface trap distribution is approximated by a series of discrete traps throughout the bandgap modeled by adding corresponding Y-circuits in parallel [see Fig. 2(b)].

The normal conductance method is based on a simplified equivalent circuit derived from Fig. 2(b) [17]. This simplified circuit is only valid in the depletion regime. For this simplified case, only the majority carrier band is assumed to interact with the interface traps. As a result, applying the conductance method on a WI response is not correct (see next section for experiments and simulations).

Another effect for smaller-bandgap semiconductors or higher temperatures is the increase of minority carrier diffusion from the bulk generating charges for surface inversion (for Ge, see [18]). The admittance contribution associated with this effect is referred to as the "diffusion-induced inversion response." This response increases with increasing intrinsic carrier concentration (n_i), which is much larger for Ge as compared to Si. In general, the admittance contribution due to inversion generation, not only due to diffusion [5], will be referred to as the "strong inversion (SIV) response."

The diffusion-induced inversion response is modeled by inserting a conductance, $G_d = q\mu_p ni^2/(L_p N_D)$ for n-type, which models the temperature-dependent supply of carriers to the inversion layer, into the circuit modeling the MOS capacitor [17] [see Fig. 2(a) and (b)]. In the equation, *q* is the electronic charge, μ_p is the minority carrier (hole) mobility, N_D is the substrate (donor) concentration, and L_p the minority carrier diffusion length. Other sources of inversion generation can be modeled by adding admittance in parallel to G_d [17].

B. Experiments and Simulations of the Diffusion-Induced Inversion and Weak Inversion Responses in the Ge MOS Admittance

The first pitfall is the possible confusion of a WI response or an SIV response with a depletion bias interface trap response or vice versa. A WI response of a relatively low amount of interface traps (case 2) shows a very similar *C–V* and *G–V* response as a function of frequency, as a depletion response of a peaked and high density of interface traps near midgap causing significant stretch-out (case 1).

We explain the measured Ge/GeO_xN_y capacitor *C–V* (Fig. 1) with the model [Fig. 2(b)] with relatively low and constant D_{it} (7×10^{11} eV^{-1} cm^{-2}, case 2) in Fig. 3(a). At temperatures

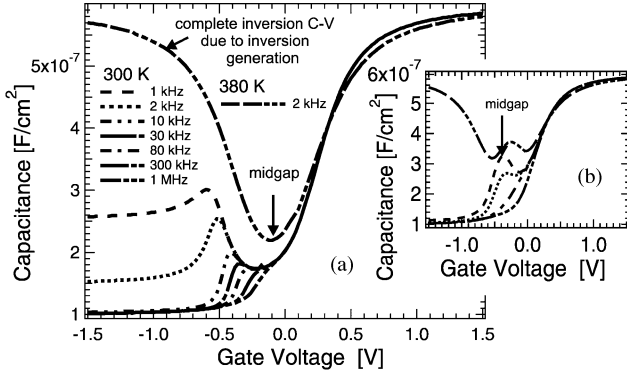

Fig. 3. (a) Simulated frequency dependence of a Ge MOS capacitor with a constant $D_{\rm it}$ ($=7\times10^{11}$ 1/eV/cm^2) at 300 K and including diffusion-induced inversion generation. The simulation corresponds to the measurement in Fig. 1 showing that the "bumps" can be explained by the weak inversion response (case 2). (b) A depletion response of a $D_{\rm it}$ peak (8×10^{12} cm^{-2}) near midgap has similar "bumps" at 300 K (case 2). At 380 K, the complete inversion *C–V* due to inversion generation reveals the difference between (a) and (b) showing the occurrence of case 2 in the measurements (Fig. 1).

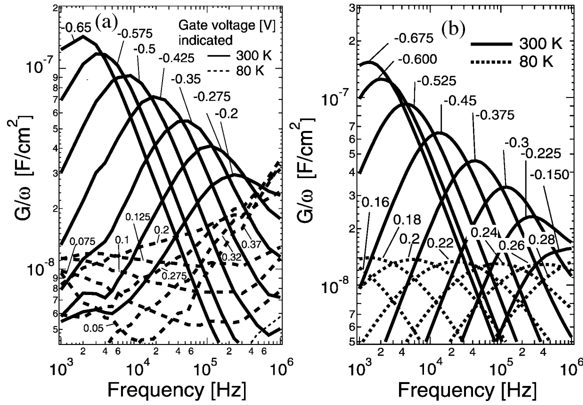

Fig. 4. (a) Measured parallel G/ω [Fig. 6(f)] versus frequency at different voltages at 80 K and 300 K for a GeO$_x$N$_y$/Ge capacitor. The large difference between the 300 K and 80 K G/ω is explained by the occurrence of a WI and a diffusion-induced inversion response at 300 K and not at 80 K. (b) Simulation corresponding to *C–V* of Fig. 3(a) explains G/ω at 80 and 300 K. The difference between model and measurement at 80 K at higher frequency is explained by a series resistance, which was not included in the model.

above 300 K, the observed complete inversion *C–V* characteristic due to inversion generation (see Figs. 1 and 3) clearly indicates the position of the WI regime. This shows that the *C–V* bump at 300 K in the measurements is located in WI excluding case 1 [see Fig. 3(b)] and confirming case 2. Moreover, the model explains the conductance as a function of frequency and voltage at 80 and 300 K (Fig. 4). The large G/ω peaks correspond to the *C–V* bumps at the same voltages. Furthermore, the model explains the *T*- and *f*-dependence of G/ω (Fig. 5).

Misinterpreting the WI response as a depletion response often leads to substantial overestimations of $D_{\rm it}$ with the normal conductance method, which implicitly assumes a depletion. The absent WI response in the G/ω measurement at 80 K (Fig. 4) allows extraction of $D_{\rm it}=7\times10^{11}$ cm$^{-2}\cdot$eV^{-1} with the conductance method and shows that an overestimation of up to an order of magnitude in $D_{\rm it}$ is possible at 300 K (maximum naively extracted $D_{\rm it}=8.5\times10^{12}$ cm$^{-2}\cdot$eV^{-1} at 300 K).

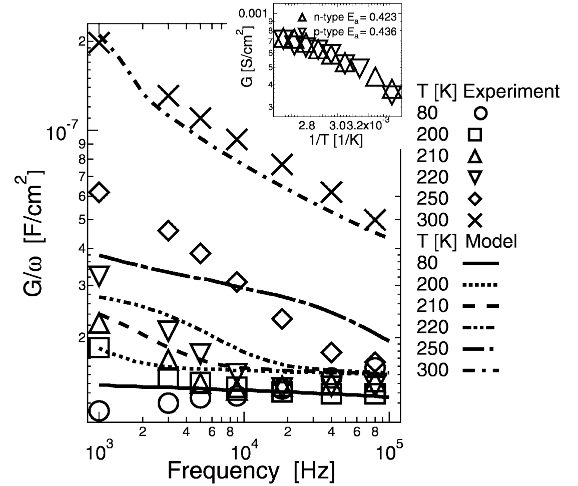

Fig. 5. Measured parallel peak value of G/ω taken as a function of voltage and plotted versus temperature and frequency of the Ge/GeO$_x$N$_y$ capacitor compared with simulation corresponding to Figs. 3(a) and 4(b). The major trends for model and measurement are the same showing the consistency with a weak inversion response. The inset shows the Arrhenius plot of measured Ge/GeO$_x$N$_y$ capacitor conductance and the extracted activation energies showing the presence of diffusion-induced inversion.

An SIV response can also be confused with a depletion response of a large amount of traps. The *C–V* and *G–V* responses as a function of frequency are similar again.

The diffusion-induced inversion response is shown to be present in the Ge/GeO$_x$N$_y$ capacitors by making use of an Arrhenius plot [17] of the conductance at 100 kHz and -1.4 V (300–378 K) (inset of Fig. 5). Diffusion-induced inversion gives rise to an activation energy (E_a) of E_g, while for generation-recombination induced inversion $E_a=E_g/2$. The presence of diffusion-induced inversion generation is indicated by $E_a=0.42$ eV $>E_g/2$ in Fig. 5 [17].

C. Full Conductance Solution to Reliably Extract $D_{\rm it}$ With Weak Inversion and Strong Inversion Responses

The WI response and SIV response dominate the conductance at 300 K for Ge (as shown by the similarity of experiment and model of the WI response in Fig. 4) and, hence, jeopardize the use of the conductance method, which assumes depletion. We show that a full conductance measurement solves the WI response and SIV response issues.

"Full conductance" is measured on a MOSFET or gated diode with the bulk and S/D shorted [see Fig. 6(b)]. The capacitance measured is referred to as "full capacitance." The short induces inversion deliberately and any conductance contribution due to SIV and WI responses will be avoided.

Applying the short [Fig. 6(b)] on the MOS capacitor circuit model [Fig. 6(a)] results in a simplified circuit, which is the same as the one used for the conventional conductance method [Fig. 6(c)], where $C_{\rm it}={\rm g}N_{\rm it}/((\omega\tau)^2+1)$ and $G_{\rm it}/\omega={\rm g}N_{\rm it}\omega\tau/((\omega\tau)^2+1)$. $N_{\rm it}$[cm^{-2}] is the density of the single-level interface traps, and ${\rm g}(E)=q^2f_0(1-f_0)/kT$ with $f_0(E)$ the Fermi–Dirac function, ω the pulsation, and *k* the Boltzman's constant.

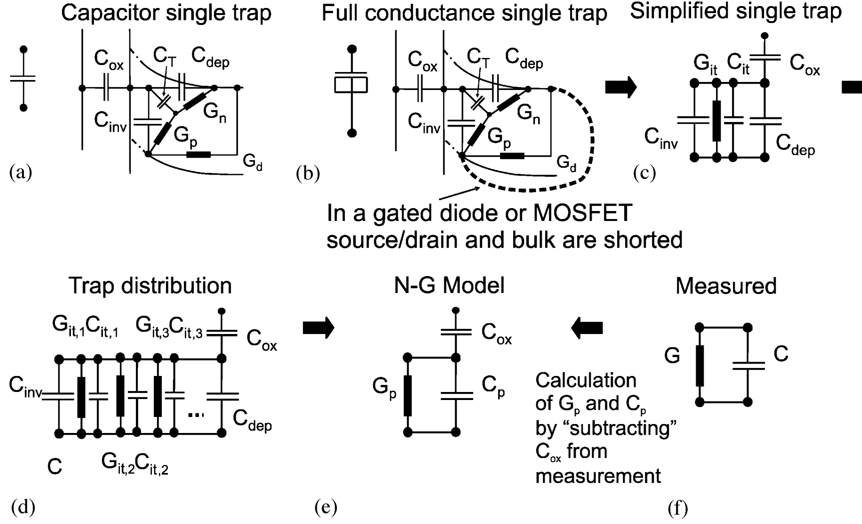

Fig. 6. (a) Capacitor single trap. (b) In a full conductance measurement, the source/drain and the bulk of a MOSFET or gated diode are shorted. This results in a simplified equivalent circuit. (c) A single trap is represented by a $G_{\rm it}$ and $C_{\rm it}$ pair. (d) A distribution of traps consists of a series of such pairs. A circuit, which is the same as the one on which the conductance method is based (see [17] for more details). (e) and (f) For a full conductance measurement, however, it is valid across the bandgap. G_p is used to extract $D_{\rm it}$ in the conductance method [17].

The simplified full conductance equivalent circuit, though, is valid across the bandgap, while that for the normal conductance method is only valid in depletion. For full conductance, the time constant is $\tau = \tau_{\rm n} \times \tau_{\rm p}/(\tau_{\rm n} + \tau_{\rm p})$, where $\tau_{\rm n}$ and $\tau_{\rm p}$ are the electron and hole interface-trap time constants, resp.

A continuous trap distribution is again approximated by a series of discrete states modeled by adding corresponding $G_{\rm it}$ and $C_{\rm it}$ elements in parallel for each trap level [Fig. 6(d)].

The conductance method uses equations based on an integral instead of a summation [Fig. 6(d)] to approximate continuous interface trap density [17]. A parameter known as the surface potential fluctuation ($\sigma_{\rm s}$), which determines the width of the G/ω peak is also included resulting in the following equations [see circuit in Fig. 6(e)] [17]:

$$C_p = C_{\rm dep} + C_{\rm inv} + q \int_{-\infty}^{\infty} \frac{D_{\rm it}}{\omega\tau} \tan^{-1}(\omega\tau) P(\sigma_s, E)\, dE \quad (1)$$

$$\frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau} \ln(1 + \omega^2\tau^2) P(\sigma_s, E)\, dE \quad (2)$$

where P is a Gaussian distribution with variance σ_s^2. These equations are valid across the bandgap for full conductance and one can apply the normal conductance method on a full conductance measurement to extract the interface trap density without WI and SIV response issues across the bandgap.

Fig. 7 shows a full conductance and a capacitor measurement at 300 K and 80 K of the Si-passivated Ge devices. The full conductance measurement at 80 K shows the typical Λ-shaped characteristic of $\tau(\mathrm{V})$, where τ determines the maximum in G/ω at each voltage ($f_{\max} = 1/2\ \pi\tau$). At 300 K, the WI response and inversion response, which show a peak G/ω increasing sharply toward lower voltage [as in Fig. 7(a) or Fig. 4(a)] are no longer present for a 300-K full conductance measurement [Fig. 7(b)] confirming the effectiveness of the full conductance solution.

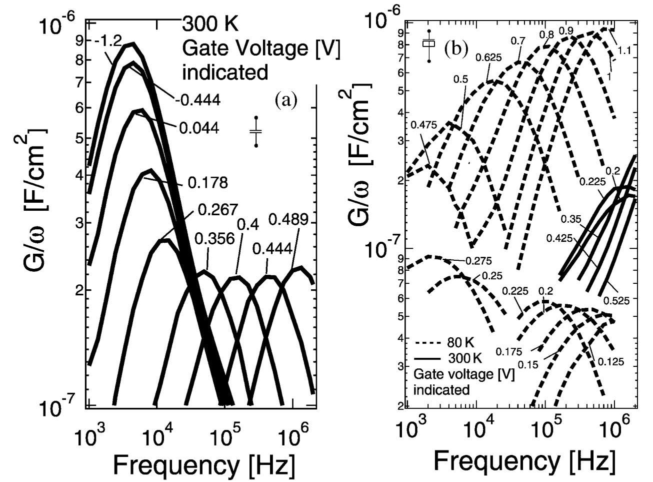

Fig. 7. (a) Measured parallel G/ω on an Si-passivated Ge n-type capacitor with HfO_2 at 80 K and 300 K. (b) Full conductance measurement on a pMOS with the same gate stack. The (weak)-inversion capacitor response is absent in the full conductance at 300 K. The small τ at 300 K causes a large part of $D_{\rm it}(E)$ to be unobservable. At 80 K, the traps near the band edges are observable.

IV. Second Pitfall: Relevance of the Interface Trap Time Constant in Alternative Semiconductor MOS

For Si/SiO_2, interface traps near the band edge only observable at 80 K and not observable at 300 K are not as important as for Ge. For Ge, $D_{\rm it}$ can be much higher near the band edge. This second pitfall is illustrated in Fig. 8. An apparent "frequency-dependent flatband voltage ($V_{\rm fb}$) shift," indicative of a high $D_{\rm it}$ ($> C_{\rm ox}/q$), is visible at 80 K but not at 300 K.

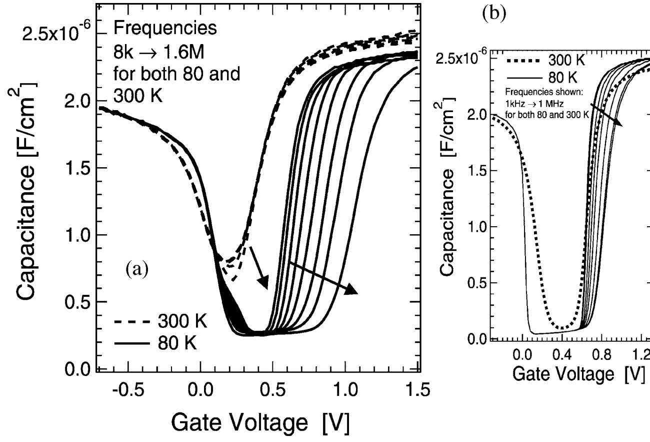

Fig. 8. (a) Frequency dependence of the *C–V* of the full conductance measurement of Si-passivated Ge with HfO_2 at 80 K and at 300 K. At 300 K, there is no significant *f*-dispersion, while, at 80 K, a "frequency-dependent flatband shift" occurs indicative of traps close to the band edge only observable at 80 K and not at 300 K. (b) The *C–V*s are explained by a simulation based on the equivalent circuit [Fig. 6 (d)], assuming an asymmetric $D_{\mathrm{it}}(E)$ with a high density of traps ($D_{\mathrm{it}} > C_{\mathrm{ox}}/q$) near the conduction band.

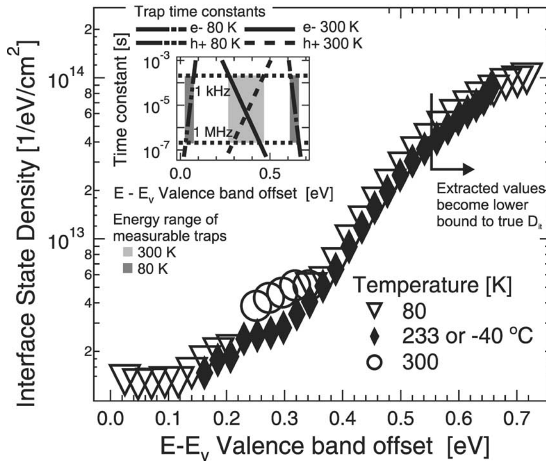

Fig. 9. Extracted D_{it} using the full conductance method at 80, 233, and 300 K for the Si-passivated Ge pMOSFETs. As the temperature is lowered, the interface traps nearer to the band edges are extracted and a large asymmetry in D_{it} over the bandgap becomes evident. The major trends in the range of traps measured at different temperatures are given in the inset.

The trap's time constant determines at which temperatures the trap can be observed because the time constant has to be within the limited frequency range of the measurement equipment (1/2 $\pi\tau = 1\ \mathrm{kHz} - 1$ MHz) (see inset of Fig. 9). Interface-trap time constants, $\tau(\Delta E) = (\sigma v_t N_c)^{-1} \exp(\Delta E/kT)$ for electrons, are mainly determined by the energy separation between the trap and the band edge (ΔE), the capture cross section (σ), and the temperature. v_t is the electron thermal velocity and N_c is the effective density of states of the conduction band, which are not more than an order of magnitude different for most semiconductors. This implies that the time constant is of the same order of magnitude at the same temperature and ΔE for most semiconductors assuming a constant σ. At 300 K, one cannot observe traps with the conductance method close to the band edges; however, at 80 K, this is possible (see inset of Fig. 9).

The trap time-constant should be accounted for by measuring at different temperatures to cover the entire bandgap. This will avoid large underestimations of D_{it}. The original conductance method was applied on a full conductance measurement (Fig. 7) to derive D_{it} reliably across the bandgap (Fig. 9). For the Si-passivated Ge MOS devices, the extracted D_{it} is more than an order of magnitude higher at 80 K compared to 300 K (Fig. 9), which clearly indicates the necessity of measurements at different temperature to extract D_{it} across the bandgap. For GaAs MOS [19], the time-constant effect necessitates measurements at higher temperatures.

The extracted asymmetric $D_{\mathrm{it}}(E)$ confirms the performance degradation due to interface traps in the Si-passivated Ge nMOSFETs, which does not occur for pMOSFETs [20]. The observed asymmetric $D_{\mathrm{it}}(E)$ further generalizes the hypothesis from [4] and [21], which were based on other gate stacks. The hypothesis states that an asymmetric $D_{\mathrm{it}}(E)$ with a high density of acceptor interface traps near the conduction band explains the inferior Ge nMOS compared to pMOS performance. These findings are consistent with a low-lying charge neutrality level [22]. The cause for this general asymmetric trap density in Ge MOS might be the result of properties of a type of Ge-oxide bonding at the interface. In the case of the Si-passivated stack, the Ge would be surface segregated. Potentially, the "interface traps" could be located not at but near the Si/SiO_2 interface, instead, for example, in the Si layer or the Si/Ge interface. The full conductance technique introduced here treats the interfaces of the Ge/Si/SiO_2/HfO_2 gate stack lying within less than 1 nm of each other as one single interface and, hence, the hypotheses regarding the location of the traps cannot be verified based on the full conductance technique. The presence of an asymmetric interface state density is shown for the Si-passivated stack explaining the nMOS performance degradation.

The full conductance measurement also allows to measure $D_{\mathrm{it}}(E)$ across the bandgap with a single measurement configuration on, e.g., an n-type device only. This allows comparison of $D_{\mathrm{it}}(E)$ across the bandgap for different doping types. An effect of doping on the interface has been reported [11].

Simulations of a full conductance measurement [using Fig. 6(d) circuit] show that an asymmetrical D_{it} with a dominant density ($qD_{\mathrm{it}} > C_{\mathrm{ox}}$) near the conduction band in Ge explains an *f*-dispersion free full *C–V* at 300 K and an *f*-dependent V_{fb}-shift at 80 K (see Fig. 8). The 300-K pseudoaccumulation *C–V* characteristic is dominated only by capacitance due to interface traps, and not majority carriers. *C–V* frequency dispersion is observed when τ is approximately within the equipment frequency range. The *f*-dependent V_{fb} shift at 80 K is explained by the dominant trap capacitance and faster traps toward the band edge that keep responding to higher frequencies.

V. Third Pitfall: Extraction of the Energy–Voltage Relationship

More pitfalls for alternative substrates are caused by the potentially much larger D_{it} than for Si/SiO_2. For high

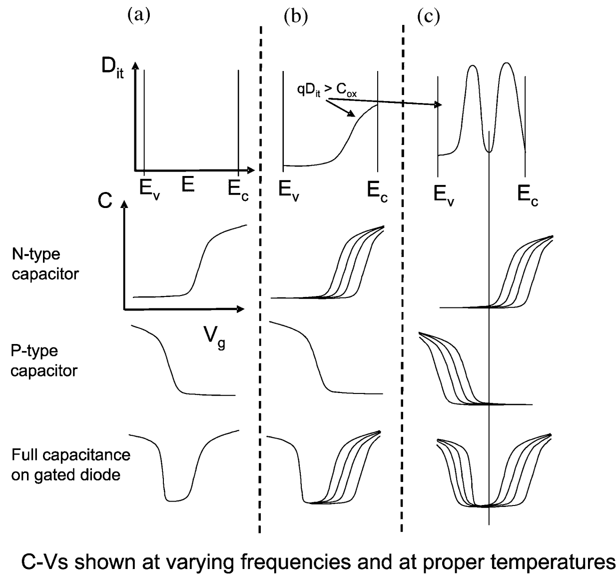

Fig. 10. (a)–(c) Schematic showing the effect of asymmetric and symmetric high $D_{\rm it}$ ($>C_{\rm ox}/q$) on capacitor and full capacitance characteristics. Temperature is chosen so that the traps are visible. It shows when a "frequency-dependent flatband shift" or "frequency-dependent threshold shift" will occur. These two phenomena, typical for a high $D_{\rm it}$, prevent the extraction of $V_{\rm fb}$ and V_t, resp. At least, either V_t or $V_{\rm fb}$, should be extractable to determine the *E–V* relation and, hence, for the symmetric case, it is not possible to determine *E–V*.

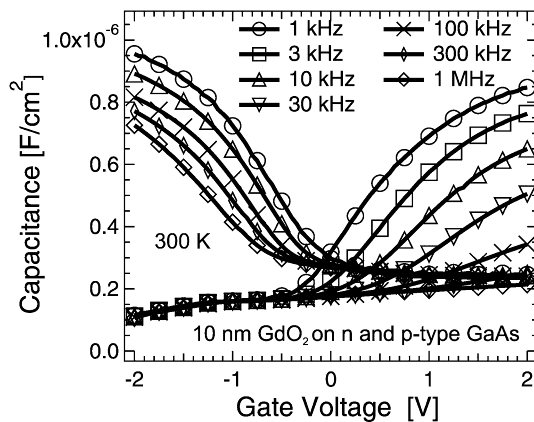

Fig. 11. N-type and p-type capacitor GaAs MOS *C–V* characteristics at 300 K. A "frequency-dependent flatband shift" occurs for both substrate types showing the relevance of the symmetric case in Fig. 13 for MOS admittance measurements in general. In this case, it is, hence, not possible to extract *E–V*.

$D_{\rm it}$ ($>C_{\rm ox}/q$), the energy–voltage relationship (*E–V*) can be difficult to extract because an apparant "*f*-dependent $V_{\rm fb}$-shift" or "frequency-dependent threshold voltage (V_t) shift" will occur in *C–V*, which prevents V_t or $V_{\rm fb}$ extraction. Making use of an extracted $D_{\rm it}(V)$, one needs to extract $V_{\rm fb}$ or V_t to anchor *E–V*. We show (Fig. 10) that for n-type with asymmetric high $D_{\rm it}$, as in some Ge MOS, the *E–V* problem can be solved by using full conductance (Fig. 10b). The full capacitance allows extracting V_t instead of $V_{\rm fb}$ when a frequency-dependent flatband shift occurs. For a $D_{\rm it}(E)$ in which the Fermi-level (E_f) is trapped between the acceptor and donor densities, neither $V_{\rm fb}$ nor $V_{\rm t}$ can be extracted [Fig. 10(c)]. We show this is the case for a typical GaAs MOS capacitor (Fig. 11) [23]–[26]. In this case, it is not possible to extract *E–V* and to position $D_{\rm it}$ in the bandgap.

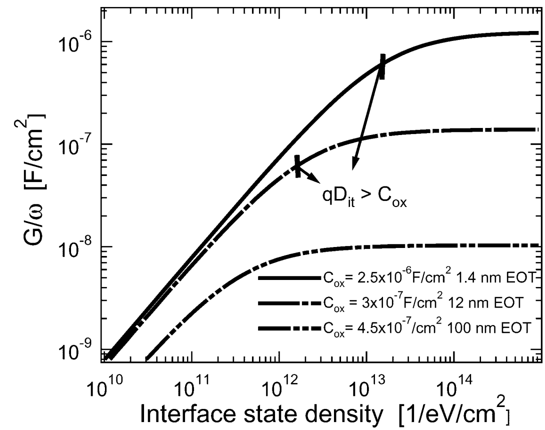

Fig. 12. Theoretical parallel G/ω [Fig. 6(f)] as a function of $D_{\rm it}$. G/ω starts saturating when $qD_{\rm it} > C_{\rm ox}$. This means that the extracted $D_{\rm it}$ value using the conductance technique becomes a lower bound of the sample $D_{\rm it}$ when the extracted $D_{\rm it} > 4C_{\rm ox}/q$ (G/ω reaches $\sim 80\%$ of saturation value).

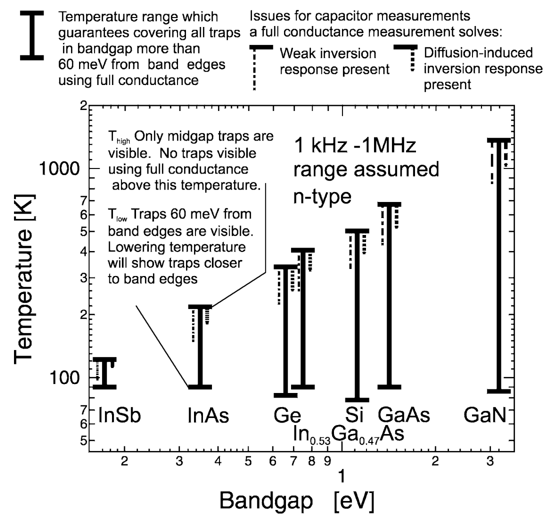

Fig. 13. Overview of the properties related to the conductance method for different semiconductors. The temperature needed to extract $D_{\rm it}$ up to midgap increases with increasing E_g. The WI and diffusion-induced inversion response occurs at increasing temperature with increasing bandgap. WI and diffusion-induced inversion response are indicated when their peak G/ω contribution was larger than a peak G/ω from a 1×10^{12} cm^{-2} eV^{-1} depletion interface trap response. A full conductance measurement is needed toward high temperature or when evaluating low trap densities to avoid WI and diffusion-induced inversion response issues and hence to avoid overestimation of $D_{\rm it}$. Generation-Recombination and surrounding surface charge induced inversion can occur at lower temperatures than diffusion-induced inversion and is not indicated and it can also be eliminated by using the full conductance technique.

Apart from the possible unfeasibility of extracting $V_{\rm fb}$ or V_t to position $D_{\rm it}(V)$ in energy, it is also possible that a very large stretch-out prevents the extraction of $D_{\rm it}$ over a sufficiently large energy range. A very high $D_{\rm it}$ ($\int qD_{\rm it}(E)/C_{\rm ox}dE > 5 - 10$ V) leads to a very large stretch-out (the extreme is Fermi-level pinning) and, then, only $D_{\rm it}$ in a small part of the bandgap can be extracted. Oxide breakdown limits the energy range.

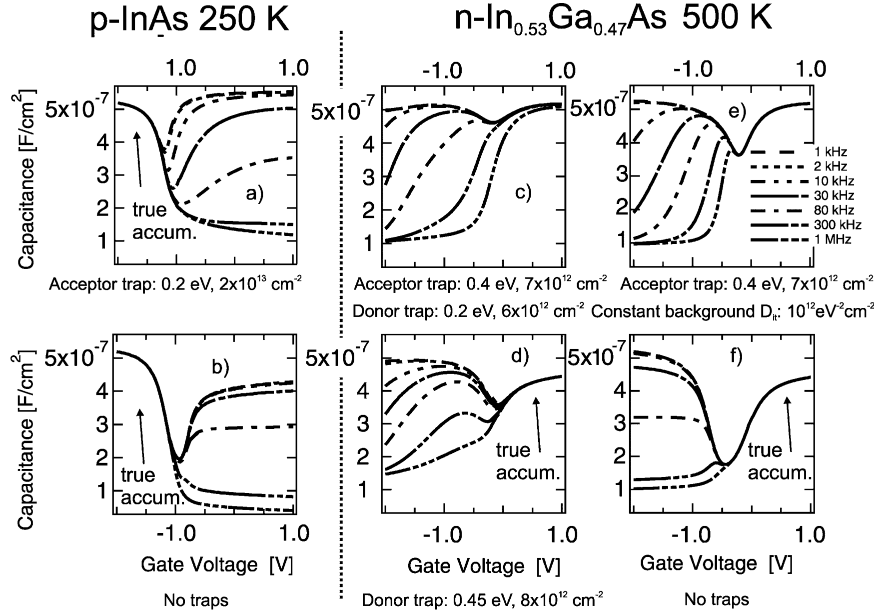

Fig. 14. (a)–(f) Simulations [with circuit model of Fig. 2(b)] illustrate the qualitative similarities of alternative MOS capacitor *C–V*s with different interface trap distributions, which can lead to misinterpretations ($D_{\rm it}$ indicated underneath graphs. Energy is relative to valence band edge). The presence of a WI response from a relatively small background $D_{\rm it}$ (c) or the SIV response in (b) and (f) can lead to confusion with distributions with more traps. Such issues are analogously present for *G–V* and are avoided with the full conductance technique. Note that pseudoaccumulation also occurs for (c) and (e), as in Fig. 8.

A conductance method using a fitting algorithm to find $D_{\rm it}(E)$ [20] enables the positioning of $D_{\rm it}$ in energy, for example, an n-type capacitor with $D_{\rm it}(E)$ with high density near the conduction band but with limited stretch-out ($\int qD_{\rm it}(E)/C_{\rm ox}dE < 1 - 2$ V). Fitting a complete MOS admittance model directly on a full conductance measurement will more accurately determine $D_{\rm it}(E)$ because the extraction of $D_{\rm it}$ and the *E–V* relationship are done simultaneously to extract *E–V* more precisely.

VI. Fourth Pitfall: Sensitivity of Conductance to High Interface Trap Density

We show that at high $D_{\rm it}$ ($qD_{\rm it} > C_{\rm ox}$), the conductance technique becomes insensitive to the trap density, as illustrated in Fig. 12 [27]. G/ω starts saturating when $D_{\rm it} > C_{\rm ox}/q$. This insensitivity is caused by the dominating $1/j\omega C_{\rm ox}$ in the MOS admittance. The saturation means that if the extracted $qD_{\rm it} > 4C_{\rm ox}$ (G/ω reaches ~80% of saturation value), the extracted value of $D_{\rm it}$ is only a lower bound of possible values. The insensitivity at higher $D_{\rm it}$ can lead to underestimation of the interface trap density for MOS on alternative substrates. In the extraction shown in Fig. 8, the threshold at which the extracted $D_{\rm it}$ becomes a lower bound is reached at ~0.55 eV.

VII. Summary of the Full Conductance Method for Extraction of the Interface Trap Density Across the Bandgap for High-Mobility Semiconductors

1) To extract $D_{\rm it}$ across the bandgap, measurements are needed in a temperature range that becomes larger with bandgap (Fig. 13). A minimal set of temperatures is selected in this range to cover the bandgap of the semiconductor. Temperatures below 300 K are required to extract near the band edges and temperatures above 300 K are required to be able to extract midgap $D_{\rm it}$ for higher bandgap materials like GaAs.
2) At each of these temperatures, a full conductance measurement is done as a function of voltage and frequency. Inversion region phenomena for non-Ge alternative semiconductor MOS were discussed recently [15], [28]. Fig. 14 shows the possible confusion in *C–V* interpretation caused by WI and SIV response for other semiconductors. The issues for *G–V* are analogous. Full conductance avoids overestimating $D_{\rm it}$ by avoiding the WI response, the diffusion-induced inversion response (see Fig. 13), and the *G–R*-induced and surrounding surface charge induced inversion response, which occur at lower temperatures than the diffusion-induced inversion response. Full conductance also enables extractions across the bandgap. On the full conductance measurement, the conductance method is applied:
   a) The oxide capacitance is subtracted from the measured admittance [see Fig. 6(e) and (f)] to derive G_p.
   b) At each voltage, the peak $G_{\rm p}/\omega$ is determined. This value is converted to a $D_{\rm it}$ value at each voltage using (2) and using an extracted $\sigma_{\rm s}$.
3) The *E–V* relationship is calculated by using the extracted $D_{\rm it}(V)$ combined with a V_t or $V_{\rm fb}$ extracted from the full capacitance characteristic. If the Fermi level is positioned in between two high ($D_{\rm it} > C_{\rm ox}/q$) interface trap peaks, it is no longer possible to position $D_{\rm it}$ in energy. At very high $D_{\rm it}$, stretch-out will prevent extraction of $D_{\rm it}$ across the bandgap.
4) If the extracted $D_{\rm it}$ is larger than $4C_{\rm ox}/q$, the extracted $D_{\rm it}$ should be marked as a lower bound to the true $D_{\rm it}$.

VIII. Conclusion

We show the pitfalls and limits of the conductance method for alternative semiconductor MOS. To demonstrate, a passivated dielectric–semiconductor interface $D_{\rm it}(E)$ needs to be extracted reliably across the bandgap. We show how the conductance method can be adapted to a full conductance method to extract interface trap density reliably and completely.

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