

Zhe (Frank) Feng, Ph.D. Candidate

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OBJECTIVE

- **Full-time; Software engineer; Available since Dec, 2011**

EDUCATION

- 2007-present University of California, Los Angeles
Ph.D. (pursuing) in **Electrical Engineering** Department (GPA: 3.8/4.0)
Committee: Lei He (advisor), Kung Yao, Puneet Gupta, Dejan Markovic, Rupak Majumdar
- 2004-2007 Tsinghua University, Beijing, China
Master in **Computer Science**
- 2000-2004 Northeastern University, Shenyang, China
Bachelor in **Computer Science**

RESEARCH INTRESTS

- Solving large scale, highly complex technical problems
- Computer-Aided Design algorithms for VLSIs
- High level synthesis/ESL design methodology
- Logic re-synthesis algorithms
- Placement and routing algorithms

WORK EXPERIENCE

- 2007-present Electrical Engineering Dept., University of California, Los Angeles
Graduate Student Researcher, participating research projects on FPGA synthesis for power reduction and soft errors mitigation.
- 06/2011-09/2011 Altera Corporation, San Jose
Intern, software development for Exclusive-OR optimization based on intersection algorithm for Quartus.
- 06/2010-09/2010 AutoESL Design Technologies, Inc. (Xilinx Inc.), Los Angeles
Intern, software development for synthesis performance prediction by fast compilation based on LLVM and Berkeley ABC.
- 06/2008-09/2008 Synopsys Inc., Sunnyvale, CA
Intern, software development for power experimental system and RTL power estimation for Synopsys low power flow.
- 2004-2007 Computer Science Dept., Tsinghua University, Beijing, China
Graduate Research Assistant, participating in fundamental research for VLSI CAD, especially on placement and routing
- 06/2006-09/2006 HT-EDA Corp. (ICScape Inc.), Beijing, P.R.China
Intern, software development for Engineering Change Order (ECO) router

PARTICIPATED RESEARCH PROJECTS

- ESL design methodology, funded by AutoESL.
- FPGA logic synthesis for fault tolerance, funded by National Scientific Foundation (NSF), CCR-0306682.
- FPGA logic synthesis for power reduction, funded by University of California Microelectronics Innovation and Computer Research Opportunities (UC MICRO 2007)
- Placement and routing algorithms considering obstacles, funded by National Scientific Foundation of China (NSFC), 60373012 (outstanding NSFC project award)
- Constrained balanced Steiner tree construction with buffer insertion, funded by HT-EDA Corp.

HONORS and AWARDS

- Best Paper Award Nomination of IEEE/ACM International Conference on Computer-Aided Design 2009 (14 out of 438 submissions) 2009
- Best Paper Award Nomination of IEEE/ACM International Conference on Computer-Aided Design 2008 (14 out of 458 submissions) 2008
- UCLA Chancellor's Prize 2008
- UCLA Chancellor's Prize 2007
- UCLA Electrical Engineering Departmental Fellowship 2007
- First Class Scholarship from Tsinghua University (top 2%) 2006
- Outstanding Student Award from Northeastern University (top 3%) 2004
- Outstanding Student Award from Liaoning Province (top 1%) 2002

PROFESSIONAL EXPERIENCES

- 09/2011-12/2011 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant, for course "Circuit Measurements Laboratory"
- 04/2011-06/2011 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant
- 01/2011-03/2011 Physics & Astronomy Dept., University of California, Los Angeles Teaching Assistant, for course "Physics for Life Sciences Majors: Waves, Electricity, and Magnetism"
- 09/2010-12/2010 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant
- 09/2010 invited talk in AutoESL Design Technologies Inc. (Xilinx Inc.)
- 04/2010-06/2010 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant, for course "Introductory Digital Design Laboratory"
- 04/2009-06/2009 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant, for course "VLSI Design Automation"
- 09/2008-12/2008 Electrical Engineering Dept., University of California, Los Angeles Teaching Assistant, for course "Computer Science Architecture"
- 09/2008 invited talk in Synopsys Inc.
- 09/2004-07/2005 Computer Science Dept. Tsinghua University, Beijing, China Teaching Assistant, for course "Fundamentals of Programming"

PROFESSIONAL ACTIVITIES

- Reviewer for leading conferences, including IEEE/ACM Design Automation Conference (DAC), IEEE/ACM International Conference on Computer-Aided Design (ICCAD), International Symposium on Physical Design (ISPD), IEEE/ACM International Symposium on Field Programmable Gate Array (ISFPGA), IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), International Conference on Field-Programmable Technology (FPT), and International Conference on Field Programmable Logic and Applications (FPL).
- Invited reviewer for top journals in the field of VLSI design and CAD, including IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- Technical Program Committee Member for International Conference on Field-Programmable Technology (FPT) 2011.

PROFESSIONAL AFFILIATIONS

- Student member of ACM (Association for Computing Machinery)

COURSE ENROLLMENT

- CS193 Algorithms and Its Complexity Theory (L. Huang)
- CS183 Computational and Combinatorial Geometry (J. Deng)
- MATH174 Modern Method for Optimal Calculation (W. Xing)
- EE236B Nonlinear Programming (L. VANDENBERGHE)
- CS124 Operations Research (L. Wang)
- CS139 Artificial Intelligence (G. Wang)
- CS152 Computer Architecture (X. Dong)
- CS134 Operating System (L. Shi)
- CS148 Computer Network (J. Liu)
- CS135 Compiler Construction Principles (L. Zhang)
- CS162 The Layout Theories and Algorithms for VLSI (X. Hong, Q. Zhou)
- EE201A VLSI Design Automation (L. He)
- CS174 Design Automation for Digital System (J. Bian)
- CS443 Computer-Aided Design of Digital Circuits and Systems (S. Dong)
- EE201C Modeling of VLSI Circuits and Systems (L. He)
- CS234 Computer-Aided Verification (R. MAJUMDAR)

COMPUTER SKILLS

- Extensive experience with C/C++ on Unix and Windows for 11 years
- Development experience on CAD optimization algorithms for 8 years
- Skillful in Perl, Shell, TCL etc. script languages
- High levels of creativity and quick problem solving capabilities

PEER REVIEWED JOURNAL PAPERS

- J1. Tong Jing, Yu Hu, Zhe Feng, Xian-Long Hong, Xiaodong Hu, Guiying Yan, A Full-scale Solution to the Rectilinear Obstacle-Avoiding Steiner Problem, Elsevier Integration, the *VLSI Journal*, 2008, 41(3): pp. 413-425.
- J2. Zhen Cao, Tom Tong Jing, Jinjun Xiong, Yu Hu, Zhe Feng, Lei He, Xian-Long Hong, Fashion: A Fast and Accurate Solution to Global Routing Problem, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2008, 27(4): pp.726-737.
- J3. Tong Jing, Zhe Feng, Yu Hu, Xianlong Hong, Xiaodong Hu, Guiying Yan, λ -OAT: λ -Geometry Obstacle-Avoiding Tree Construction with $O(n \log n)$ Complexity, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2007, 26(11): pp.2073-2079.
- J4. Yu Hu, Tong Jing, Zhe Feng, Xianlong Hong, Xiaodong Hu, Guiying Yan, ACO-Steiner: Ant Colony Optimization Based Rectilinear Steiner Minimal Tree Algorithm, *Journal of Computer Science and Technology*, 2006, 21(1): pp.147-152.
- J5. Yu Hu, Zhe Feng, Tong Jing, Xianlong Hong, Yang Yang, Ge Yu, Xiaodong Hu, Guiying Yan, FORst: A 3-Step Heuristic for Obstacle-Avoiding Rectilinear Steiner Minimal Tree Construction, *Journal of Information & Computational Science*, 2004, 1(3): pp.107-116.

PEER REVIEWED CONFERENCE PAPERS

- C1. Zhe Feng, Naifeng Jing, Yu Hu, and Lei He, IPF: In-Place X-Filling to Mitigate Soft Errors in SRAM-based FPGAs, *IEEE International Conference on Field Programmable Logic and Applications*, 2011
- C2. Naifeng Jing, Ju-Yueh Lee, Zhe Feng et al., Quantitative SEU Fault Analysis for SRAM-Based FPGA Architectures and Synthesis Algorithms, *IEEE International Conference on Field Programmable Logic and Applications*, 2011.
- C3. Ju-Yueh Lee, Zhe Feng and Lei He, In-Place Decomposition for Robustness in FPGA, *IEEE/ACM International Conference on Computer Aided Design*, 2010.
- C4. Zhe Feng, Yu Hu, Lei He and Rupak Majumdar, IPR: In-Place Reconfiguration for FPGA Fault Tolerance, *IEEE/ACM International Conference on Computer Aided Design*, 2009, pp.105-108. **(Best Paper Award nomination)**
- C5. Yu Hu, Zhe Feng, Lei He, and Rupak Majumdar, Robust FPGA Resynthesis Based on Fault Tolerant Boolean Matching, *IEEE/ACM International Conference on Computer Aided Design*, 2008, pp. 706-713. **(Best Paper Award nomination)**
- C6. Zhe Feng, Yu Hu, Tong Jing, Xianlong Hong, Xiaodong Hu, Guiying Yan, An $O(n \log n)$ Algorithm for Obstacle-Avoiding Routing Tree Construction in the λ -Geometry Plane, *ACM International Symposium of Physical Design*, 2006, pp.48-55.
- C7. Yiyu Shi, Tong Jing, Lei He, Zhe Feng, Xianlong Hong, CDCTree: Novel Obstacle-Avoiding Routing Tree Construction Based on Current Driven Circuit Model, *IEEE/ACM Asia and South Pacific Design Automation Conference*, 2006, pp.630-635.

- C8.Yu Hu, Tong Jing, Xianlong Hong, Zhe Feng, Xiaodong Hu, Guiying Yan, An-OARSMAN: Obstacle-Avoiding Routing Tree Construction with Good Length Performance, *IEEE/ACM Asia and South Pacific Design Automation Conference*, 2005, pp.7-12.
- C9.Yu Hu, Zhe Feng, Tong Jing, Xianlong Hong, Yang Yang, Ge Yu, Xiaodong Hu, Guiying Yan, A 3-Step Heuristic for Obstacle-Avoiding Rectilinear Steiner Minimal Tree Construction, *ISC&I*, 2004, pp. 1017-1021.
- C10.Yu Hu, Tong Jing, Xianlong Hong, Zhe Feng, Xiaodong Hu, Guiying Yan, An Efficient Rectilinear Steiner Minimum Tree Algorithm Based on Ant Colony Optimization, *IEEE International Conference on Communications, Circuits and Systems*, 2004, pp.1276-1280.

PEER REVIEWED WORKSHOP PAPERS

- W1.Zhe Feng and Lei He, Logic Synthesis for Soft Error Resilience in FPGAs, *Ph.D. Forum at DAC*, 2011.
- W2.Zhe Feng, Yu Hu, Rupak Majumdar and Lei He, IPR: InPlace Reconfiguration for FPGA Fault Tolerance, *International Workshop on Logic and Synthesis*, 2009.
- W3.Yu Hu, Zhe Feng, Rupak Majumdar and Lei He, Templates and Algorithms of Boolean Matching for Fault Tolerance in FPGAs, *International Workshop on Logic and Synthesis*, 2008.

PATENTS

- P1.A method for obstacle-avoiding routing tree construction with good wire-length performance. (Chinese patent pending 200410090885.5. published on 2005/04/06), By Xianlong Hong, Tong Jing, Yu Hu, Zhe Feng, and Yang Yang.
- P2.A method for obstacle-avoiding rectilinear Steiner minimum tree construction. (Chinese patent 200410069118.6, granted), By Xianlong Hong, Tong Jing, Yu Hu, Zhe Feng, and Yang Yang.

REFERENCE

- Available on request.