

# **Virtex-II™ V2MB1000 Development Board User's Guide**



**Version 1.4  
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PN# DS-MANUAL-V2MB1000



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## 1 Overview

The Virtex-II V2MB1000 Development Kit provides a complete solution for developing designs and applications based on the Xilinx Virtex-II FPGA family. The kit bundles an expandable Virtex-II based system board with a power supply, user guide and reference designs. Also available from Insight, optional P160 expansion modules enable further application specific prototyping and testing. Xilinx ISE software and a JTAG cable are available as kit options.

The Virtex-II system board utilizes the 1-million gate Xilinx Virtex-II device (XC2V1000-4FG456C) in the 456 fine-pitch ball grid array package. The high gate density and large number of user I/Os allows complete system solutions to be implemented in the advanced platform FPGA. The system board includes a 16M x 16 DDR memory, two clock sources, RS-232 port, and additional user support circuits. An LVDS interface is provided with a 16-bit transmit and 16-bit receive port plus clock, status, and control signals for each. The board also supports the Insight P160 expansion module standard, allowing application specific expansion modules to be easily added.

The Virtex-II FPGA family has the advanced features needed to fit demanding, high-performance applications. The Virtex-II Development Kit provides an excellent platform to explore these features so that you can quickly and effectively meet your time-to-market requirements.

## 2 The Virtex-II System Board

The Virtex-II System Board provides the FPGA, support circuits and the expansion slot for realizing MicroBlaze based designs. Of course, the platform can be easily used for non-MicroBlaze applications just as well. Figure 1 shows a picture of the board and its features.

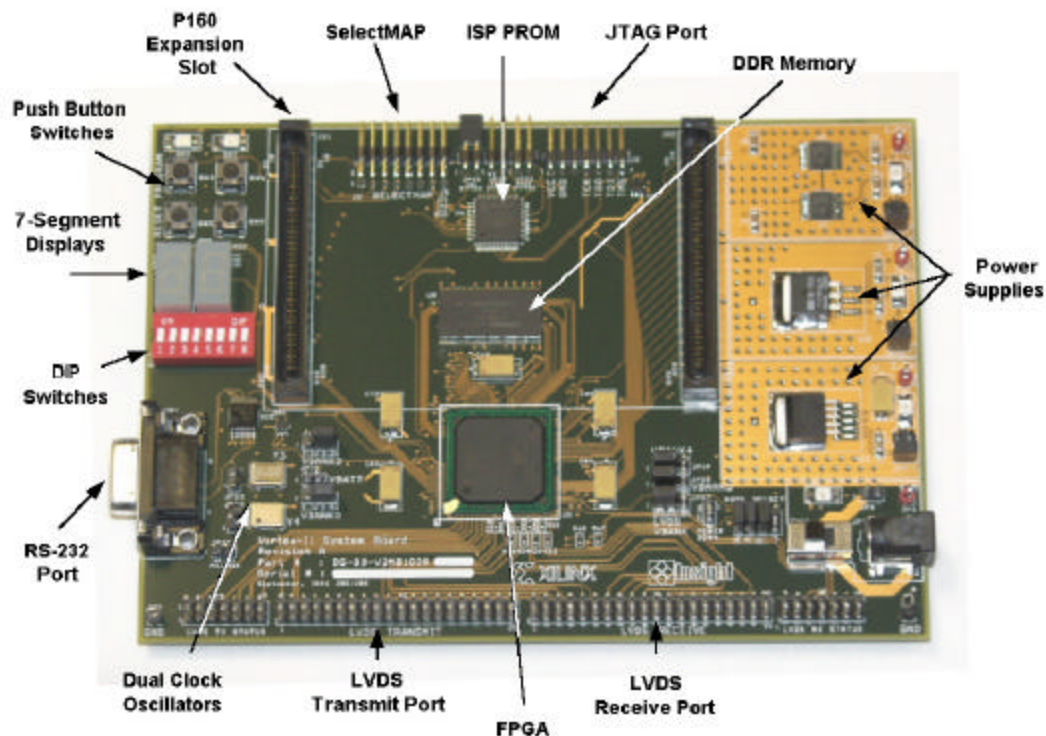


Figure 1 – Virtex-II System Board

## 2.1 Virtex-II System Board Description

A high-level block diagram of the Virtex-II development board is shown in Figure 2 followed by a brief description of each sub-section.

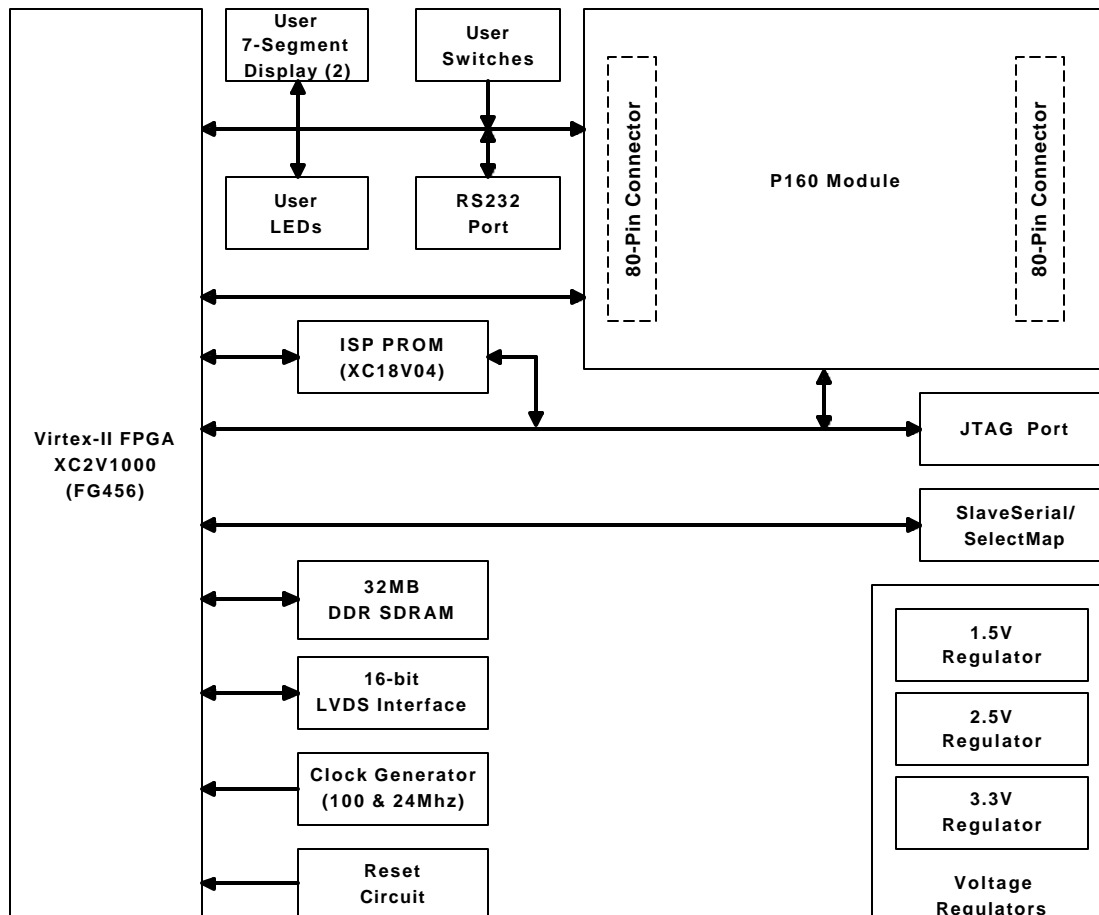


Figure 2 – Virtex-II System Board Block Diagram

## 2.2 Virtex-II Device

The Virtex-II board utilizes the Xilinx Virtex-II XC2V1000-4FG456C. The Virtex-II family is a platform FPGA developed for high performance, low to high-density designs utilizing IP cores and customized modules. The Virtex-II family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications. The performance and density of the Virtex-II family along with its supported I/O standards such as LVDS, PCI, and DDR enables FPGA designers to meet the design requirements of the next generation Networking and telecommunication applications. Although, designed to support the Xilinx MicroBlaze soft processor development, this development platform can be used to prototype a variety of applications. The Xilinx Virtex-II FPGA along with its supporting I/O devices on this development board, will assist FPGA designers to prototype high-performance memory and I/O interfaces such as complete high-performance Packet Over SONET Level 4 (PL4) over a 16-bit LVDS bus, high speed DDR memory interface, and a variety of other I/O interfaces via the on-board I/O module.

### 2.3 DDR Memory

The Virtex-II development board provides 32MB of DDR memory on the System board. This memory is implemented using the Toshiba TC59WM815BFT 16Mx16 DDR device. A high-level block diagram of the DDR interface is shown below followed by a table describing the DDR memory interface signals.

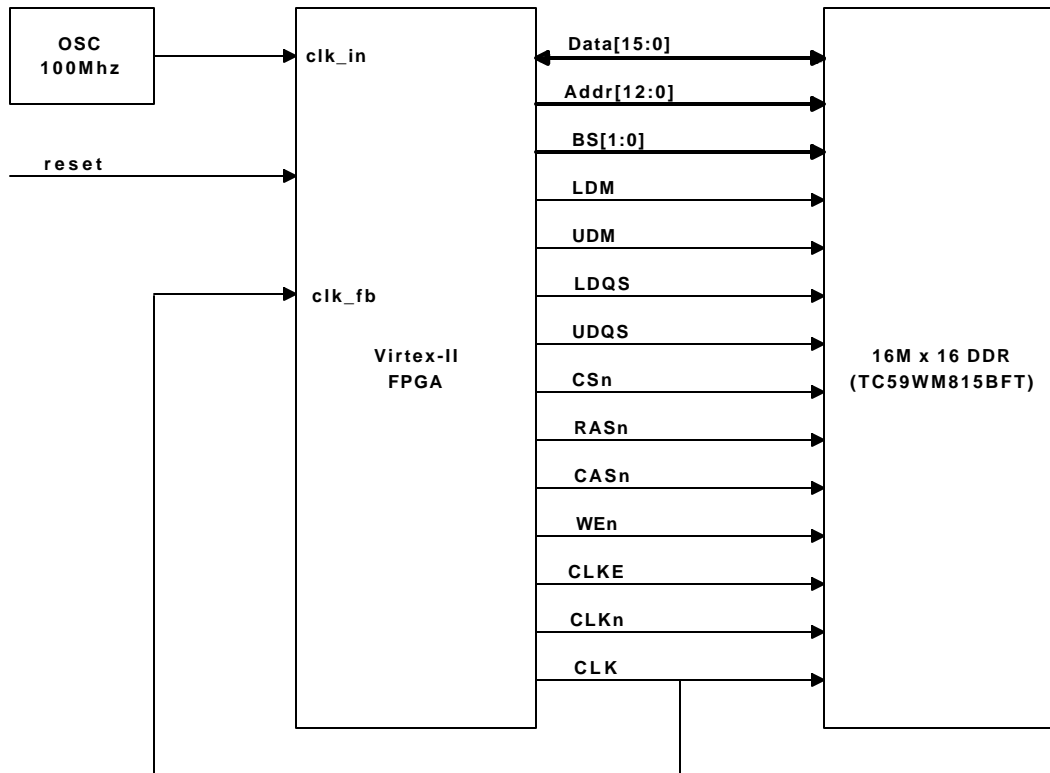


Figure 3 – DDR Interface

Table 1 - DDR Memory Interface Signal Descriptions

Signal Name	Description	FPGA Pin #	DDR Pin #
A0	Address 0	B18	29
A1	Address 1	A18	30
A2	Address 2	B17	31
A3	Address 3	A17	32
A4	Address 4	N17	35
A5	Address 5	P18	36
A6	Address 6	P17	37
A7	Address 7	M18	38
A8	Address 8	M19	39
A9	Address 9	M20	40
A10	Address 10	A19	28
A11	Address 11	N18	41

A12	Address 12	N20	42
DQ0	Data 0	Y21	2
DQ1	Data 1	Y22	4
DQ2	Data 2	W21	5
DQ3	Data 3	V21	7
DQ4	Data 4	V22	8
DQ5	Data 5	U21	10
DQ6	Data 6	U22	11
DQ7	Data 7	T21	13
DQ8	Data 8	R20	54
DQ9	Data 9	R19	56
DQ10	Data 10	T20	57
DQ11	Data 11	T19	59
DQ12	Data 12	U19	60
DQ13	Data 13	V20	62
DQ14	Data 14	V19	63
DQ15	Data 15	W20	65
BS0	Bank Select 0	M21	26
BS1	Bank Select 1	B19	27
LDM	Low Write Mask	R21	20
UDM	High Write Mask	T22	47
LDQS	Low Write/Read Data Strobe	P20	16
UDQS	High Write/Read Data Strobe	P19	51
CSn	Chip Select	N22	24
RASn	Row Address Strobe	N21	23
CASn	Column Address Strobe	P21	22
WEn	Write Enable	R22	21
CLK	Clock	D12	45
CLKn	Clock	E12	46
CKE	Clock Enable	N19	44

## 2.4 Clock Generation

The Virtex-II system board provides two on-board oscillators running at 100Mhz (CLK.CAN2) and 24Mhz (CLK.CAN1). The 100Mhz oscillator is enabled when the JP24 jumper is open and disabled when JP24 is closed. JP23 controls the 24MHz oscillator, enabling it when open and disabling it when closed. The following table provides a brief description of these clock signals.

**Table 2 – Virtex-II Development Board Master Clocks**

Signal Name	Virtex-II Pin #	Direction	Description
CLK.CAN2	B11	Input	On-board 100 MHz Oscillator
CLK.CAN1	A11	Input	On-board 24 MHz Oscillator

## 2.5 Reset Circuit

The Virtex-II system board uses the TI TPS3125 voltage supervisory device to monitor the Virtex-II FPGA core voltage (1.5V). This circuit asserts a reset signal (FPGA\_RESEn) to the Virtex-II device when the 1.5V core voltage falls below its minimum specifications (1.425V). The reset

signal to the FPGA is a fixed 100ms active low pulse. In addition to monitoring the core voltage, this circuit can be used to generate a reset pulse by activating the Master Reset (MRn) signal to the TPS3125 device via the on-board push-button switch (SW3). The following figure shows the reset circuit on the Virtex-II development board.

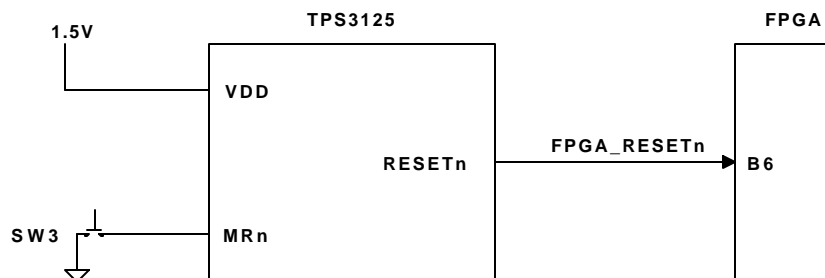


Figure 4 – Reset Circuit

## 2.6 User 7-Segment Display

The Virtex-II system board utilizes two common-cathode 7-segment LED displays that can be used during the test and debugging phase of a design. The user can turn a given segment on by driving the associated signal high. The following figure shows the user 7-segment display interface to the Virtex-II FPGA.

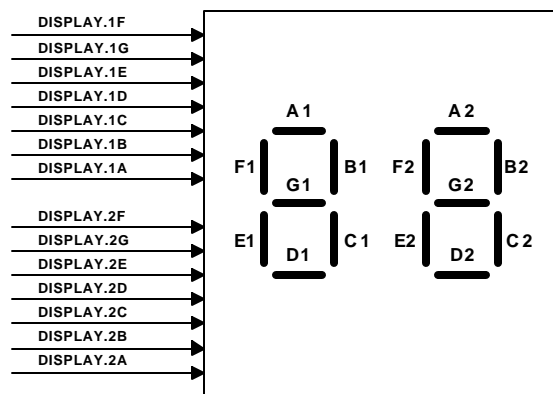


Figure 5 - 7-Segment LED Display Interface

### 2.6.1 7-Segment Display Signal Description

The following table shows the 7-Segment LED display pin descriptions.

**Table 3 - 7-Segment Display Signal Descriptions**

<b>Signal Name</b>	<b>Virtex-II Pin #</b>	<b>Description</b>
DISPLAY.1A	D9	7-Segment LED Display1, Segment A
DISPLAY.1B	C9	7-Segment LED Display1, Segment B
DISPLAY.1C	F11	7-Segment LED Display1, Segment C
DISPLAY.1D	F9	7-Segment LED Display1, Segment D
DISPLAY.1E	F10	7-Segment LED Display1, Segment E
DISPLAY.1F	D10	7-Segment LED Display1, Segment F
DISPLAY.1G	C10	7-Segment LED Display1, Segment G
DISPLAY.2A	B9	7-Segment LED Display2, Segment A
DISPLAY.2B	A8	7-Segment LED Display2, Segment B
DISPLAY.2C	B8	7-Segment LED Display2, Segment C
DISPLAY.2D	E7	7-Segment LED Display2, Segment D
DISPLAY.2E	E8	7-Segment LED Display2, Segment E
DISPLAY.2F	E10	7-Segment LED Display2, Segment F
DISPLAY.2G	E9	7-Segment LED Display2, Segment G

## 2.7 User LED

The Virtex-II system board provides a single user LED. Pin A9 of the Virtex-II FPGA is used to drive this active high signal.

## 2.8 User Push Button Switches (SW5, and SW6)

The Virtex-II system board provides two user push button switch inputs to the Virtex-II FPGA. Each push button switch can be used to generate an active low signal.

### 2.8.1 User Push Button Switch Signal Assignments

The following table shows the pin assignments for the user push button switches.

**Table 4 - User Push Button Switch Signal Assignments**

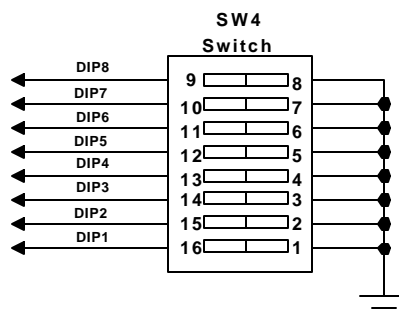
<b>Signal Name</b>	<b>Virtex-II Pin #</b>	<b>Description</b>
FPGA.PUSH1	D7	User Push Button Switch Input 1 (SW5)
FPGA.PUSH2	A6	User Push Button Switch Input 2 (SW6)

## 2.9 User DIP Switch (SW2)

The Virtex-II system board provides 8 user switch inputs. These switches can be statically set to a low or high logic level.

### 2.9.1 User DIP Switch Interface

The following figure shows the user DIP switch interface to the Virtex-II FPGA.



**Figure 6 – User DIP Switch Interface**

### 2.9.2 User DIP Switch Signal Assignments

The following table shows the user switch pin assignments.

**Table 5 - User DIP Switch Signal Assignments**

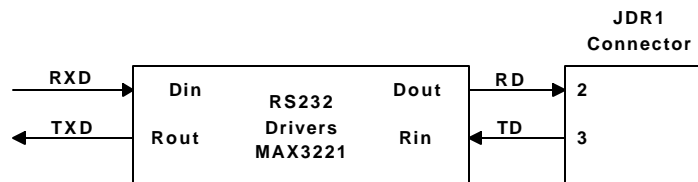
Signal Name	Virtex-II Pin #	Description
DIP8	C6	User Switch Input 8
DIP7	D6	User Switch Input 7
DIP6	A5	User Switch Input 6
DIP5	B5	User Switch Input 5
DIP4	C5	User Switch Input 4
DIP3	C4	User Switch Input 3
DIP2	A4	User Switch Input 2
DIP1	B4	User Switch Input 1

## 2.10 RS232 Port

The Virtex-II system board provides an RS232 port that can be driven by the Virtex-II FPGA. A subset of the RS232 signals is used on the Virtex-II development board to implement this simple interface (RD and TD signals).

### 2.10.1 RS232 Interface

The Virtex-II system board provides a DB-9 connection for a simple RS232 port. The board utilizes the TI MAX3221 RS232 driver for driving the RD and TD signals. The user provides the RS232 UART code, which resides in the Virtex-II FPGA.



**Figure 7 – RS232 Interface**

### 2.10.2 RS232 Signal Descriptions

The following table shows the RS232 signals and their pin assignments to the Virtex-II FPGA.

**Table 6 - RS232 Signal Descriptions**

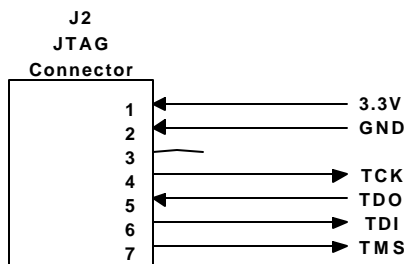
Signal Name	Virtex-II Pin #	Description
RXD	A7	Received Data, RD to DB9
TXD	B7	Transmit Data, TD from DB9

### 2.11 JTAG Port

The Virtex-II development board provides a JTAG port that can be used to configure and/or program various devices on the board and any JTAG devices located on the P160 Expansion module.

#### 2.11.1 JTAG Connector

The Virtex-II development board provides a JTAG connector that can be used to program the on-board ISP PROM, configure the Virtex-II FPGA, and program and/or configure JTAG devices located on the P160 Expansion module. The following figure shows the pin assignments for the JTAG connector on the Virtex-II development board.



**Figure 8 – JTAG Connector**

#### 2.11.2 JTAG Signal Descriptions

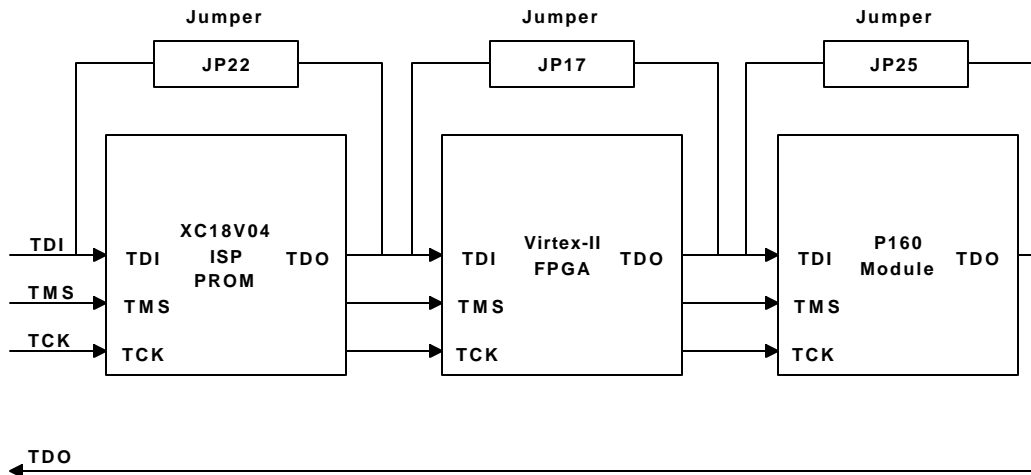
The following table provides a brief description of the JTAG signals and their pin assignments to the Virtex-II FPGA.

**Table 7 - JTAG Signal Descriptions**

Signal Name	Description
TDI	JTAG Data Input
TCK	JTAG Clock Input
TMS	JTAG Test Mode Input
TDO	JTAG Data Output

### 2.11.3 JTAG Chain

The following figure shows the JTAG chain on the Virtex-II development board. If any of the devices in the chain is not populated, its associated jumper must be closed in order to maintain the chain integrity. If the P160 Expansion module is not present, the JP25 jumper must be closed in order to bypass the P160 module TDI pin to its TDO pin.



**Figure 9 – Virtex-II System Board JTAG Chain**

### 2.11.4 JTAG Chain Jumper Settings

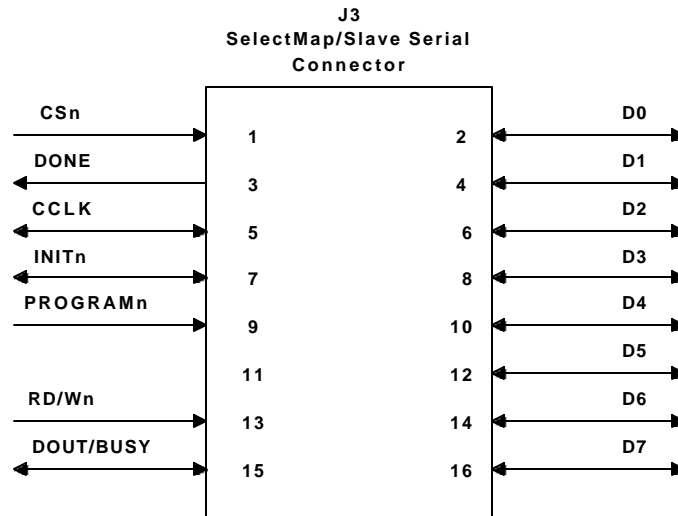
The following table shows the JTAG chain jumper setting on the Virtex-II development board.

**Table 8 - JTAG Chain Jumper Settings**

Jumper	Setting	Description
JP22	Open	XC18V04 ISP PROM is present
	Closed	XC18V04 ISP PROM is not present
JP17	Open	Virtex-II FPGA is present
	Closed	Virtex-II FPGA is not present
JP25	Open	P160 module is present
	Closed	P160 module is not present

### 2.12 SelectMap/Slave Serial Port

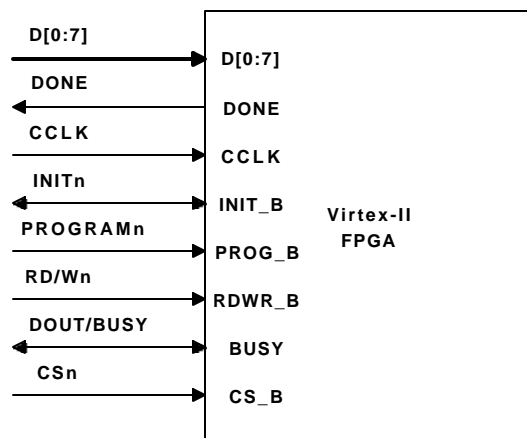
In addition to the JTAG mode, the Virtex-II FPGA on the development board can be configured using the Slave Serial or the SelectMap mode of configuration. The following figure shows the connector pin assignments for the Slave Serial/SelectMap port.



**Figure 10 – SelectMap/Slave Serial Connector**

### 2.12.1 Slave SelectMap

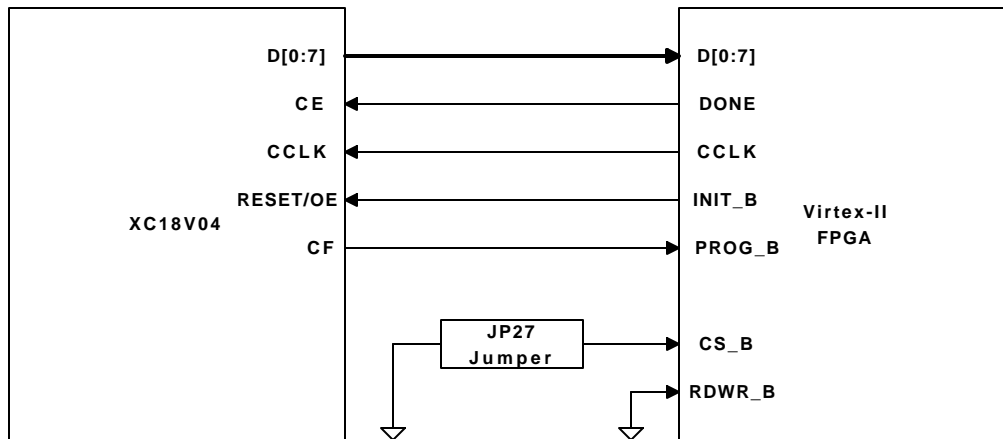
In the Slave SelectMAP configuration mode, a byte of configuration data is loaded into the Virtex-II FPGA during each CCLK clock cycle. In this mode, an external source drives the CCLK clock and the data bus containing the configuration data. The following figure shows the Slave SelectMap configuration mode interface to the Virtex-II FPGA.



**Figure 11 – Slave SelectMap Mode Configuration**

### 2.12.2 Master SelectMap

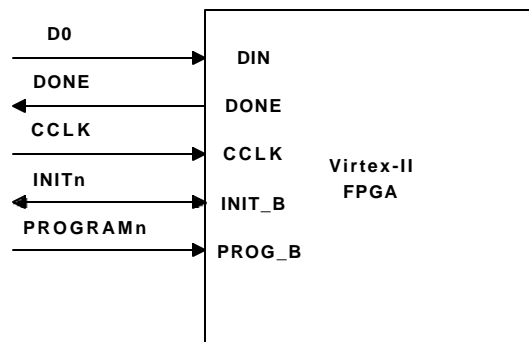
In the Master SelectMAP configuration mode, a byte of configuration data is loaded into the Virtex-II FPGA during each CCLK clock cycle. In this mode, the Virtex-II FPGA drives the CCLK clock while receiving configuration data from the PROM. The following figure shows the Master SelectMap configuration mode interface to the Virtex-II FPGA. The JP27 jumper must be installed when configuring the Virtex-II FPGA in the Master SelectMap mode.



**Figure 12 – Master SelectMap Mode Configuration**

### 2.13 Slave Serial Port

In the Slave Serial configuration mode, a bit of configuration data is loaded into the FPGA during each CCLK clock cycle. In this mode, an external source places the most significant bit of each byte on the DIN pin first and then drives the CCLK clock to store data into the FPGA. The following figure shows the Slave Serial configuration mode interface to the Virtex-II FPGA.



**Figure 13 – Slave Serial Mode Configuration**

### 2.14 Bank I/O Voltage

The Virtex-II development board allows the Virtex-II I/O pins to be configured for 2.5V or 3.3V operation. All Virtex-II user I/O pins are grouped in 8 different banks. Each bank of I/O pins on the board can be configured to operate in the 2.5V or the 3.3V mode.

#### 2.14.1 Bank I/O Voltage Jumper Settings

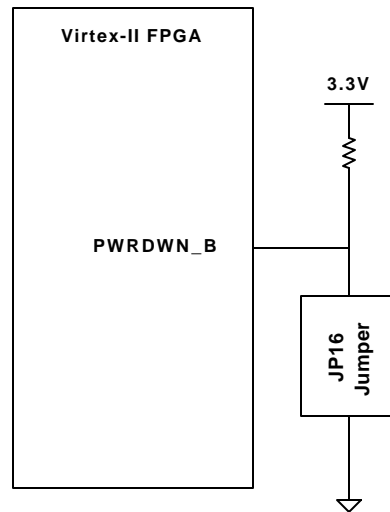
The following table shows the jumper settings for the Virtex-II bank I/O voltage (VCCO) selection. Each bank can be set to 2.5V or 3.3V.

**Table 9 - Bank I/O Voltage Jumper Settings**

Bank #	Virtex-II VCCO Pin #	Jumper		I/O Voltage	
0		<b>JP18</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V
1		<b>FIXED</b>		2.5V	
2		<b>JP26</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V
3		<b>FIXED</b>		2.5V	
4		<b>J19</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V
5		<b>J20</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V
6		<b>J21</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V
7		<b>J21</b>			
		1-2	2-3		
		Closed	Open		3.3V
		Open	Closed		2.5V

### 2.15 Virtex-II Power Down Mode

The Virtex-II FPGA family utilizes a dedicated pin called PWRDWN\_B that can be used to place the Virtex-II FPGA into a low-power and inactive state. In the normal operating mode, the PWRDWN\_B pin would be pulled up. Forcing the PWRDWN\_B pin to logic 0 would place the Virtex-II FPGA in power-down mode. The following figure shows the Virtex-II Power Down on the Virtex-II development board.



**Figure 14 – Virtex-II Power Down Mode**

As shown in the above figure, the Virtex-II FPGA can be placed in the power-down mode on the Virtex-II system board by closing the JP16 jumper (permanently placing it in the power-down mode until the jumper is removed), or by forcing the pin 2 of the JP16 to a logic 0 under user control. The Virtex-II board users can use this pin to place the Virtex-II FPGA in the power-down mode momentarily.

The Virtex-II FPGA provides Power-Down status information via the DONE pin if the PWRDWN\_STAT option is selected using BitGen. The DONE pin is asserted upon entry to the power-down mode. After a successful wake-up, the DONE status pin is de-asserted (The wake-up sequence is the reverse of the power-down sequence). While in power-down mode, the only active pins are the PWRDWN\_B and DONE. All inputs are off and all outputs are 3-stated.

While in the Power-Down state, the Power On Reset (POR) circuit is still active, but it does not reset the device if VCCINT, VCCO, or VCCAUX falls below its minimum value. The POR circuit waits until the PWRDWN\_B pin is released before resetting the device. Also, the PROG\_B pin is not sampled while the device is in the Power-Down state. The PROG\_B pin becomes active when the PWRDWN\_B pin is released. Therefore, the device cannot be reset while in the Power-Down state.

## 2.16 Virtex-II VBAT

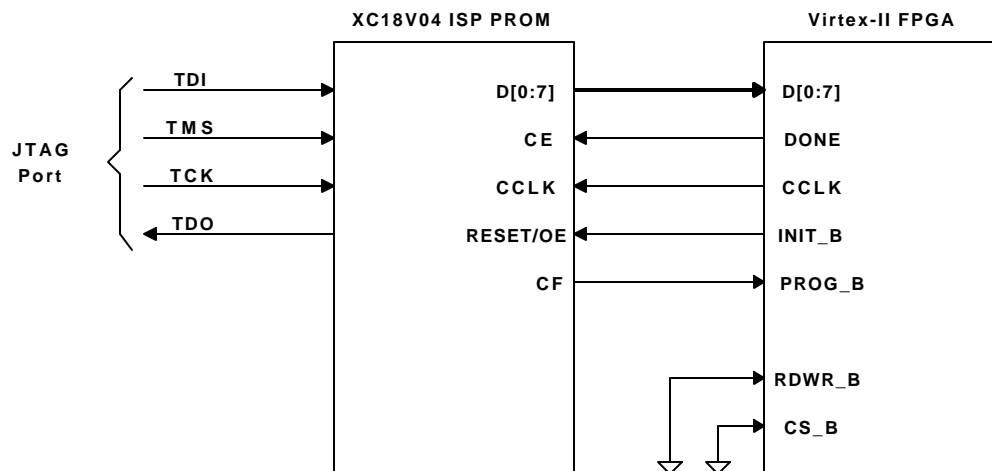
The Virtex-II VBAT input pin (pin A21) is connected to the 3.3V supply on the Virtex-II development board through the JP15 jumper.

## 2.17 ISP PROM

The Virtex-II system board utilizes the Xilinx XC18V04 ISP PROM, allowing FPGA designers to quickly download revisions of a design and verify the design changes in order to meet the final system-level design requirements. The XC18V04 ISP PROM uses two interfaces to accomplish the configuration of the Virtex-II FPGA.

The JTAG port on the XC18V04 device is used to program the PROM with the design bit file. Once the XC18V04 has been programmed, the user can configure the Virtex-II device in Master Serial or Master SelectMap mode. The configuration of the Virtex-II device is initiated by asserting the PROGn signal. Upon activation of the PROGn signal (by pressing the SW2 switch), the XC18V04 device will use its FPGA Configuration Port to configure the Virtex-II FPGA.

If the Virtex-II configuration mode is set to Master Serial, the PROM D0, CE, CCLK, RESET/OE, and the CF signals are used to configure the Virtex-II FPGA. In the Master SelectMap mode, in addition to the above signals, the Virtex-II FPGA will use the PROM D1-7 to obtain a byte of configuration data during each CCLK clock cycle. The following figure shows the ISP PROM interface to the JTAG port and the Virtex-II FPGA configuration port.



**Figure 15 – ISP PROM Interface**

## 2.18 LVDS Port

The Virtex-II development board provides a complete high-performance differential signaling (LVDS) interface, enabling the designers to prototype high-speed serial communication links. The Virtex-II I/Os are designed to comply with the IEEE electrical specifications for LVDS to make system and board design easier. With the addition of an LVDS current-mode driver in the IOBs, which eliminates the need for external source termination in point-to-point applications, and with the choice of two different voltage modes and an extended mode, Virtex-II devices provide the most flexible solution for doing an LVDS design in an FPGA.

### 2.18.1 LVDS Interface

The Virtex-II development board provides a 16-bit LVDS port (Transmit and Receive) with 6 additional control signals that can be used to implement a high-speed Packet Over SONET Level 4 (PL4) interface. The following figure shows the LVDS interface on the Virtex-II development board. LVDS termination networks are provided between the Virtex-II FPGA and the LVDS user connectors. It should be noted that no LVDS source terminations are needed when using the Virtex-II FPGA family in point-to-point applications.

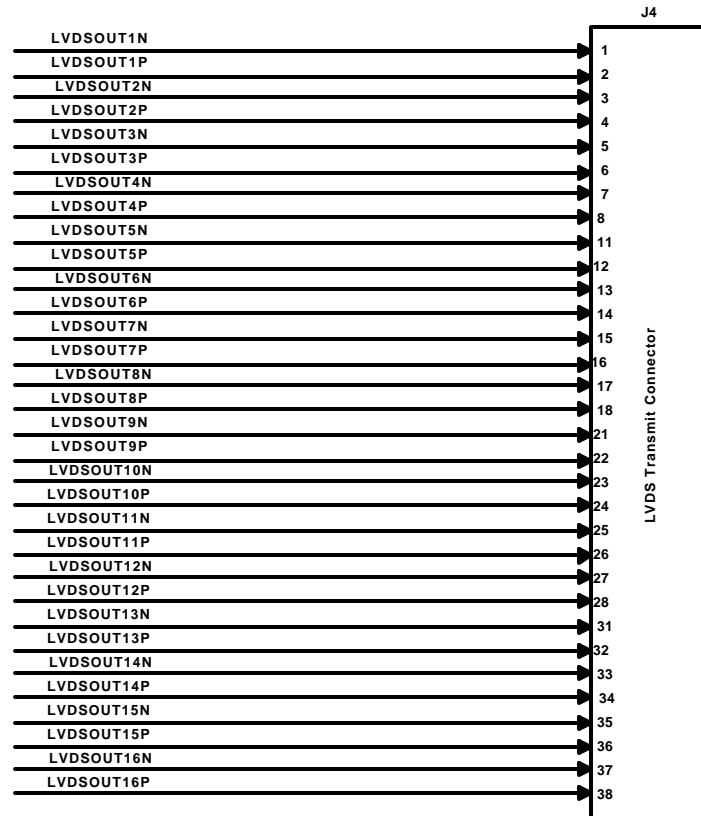


Figure 16 – LVDS Transmit Port

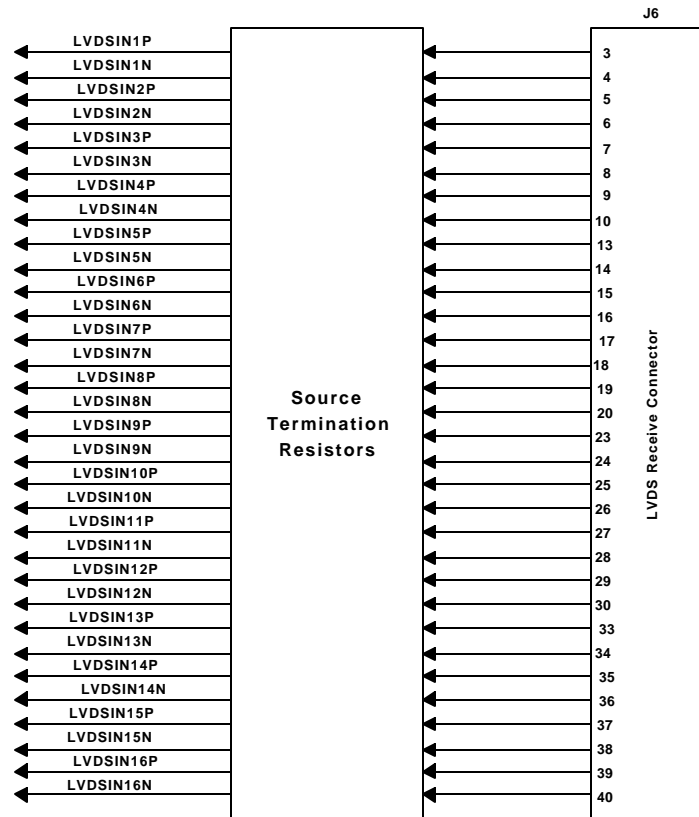
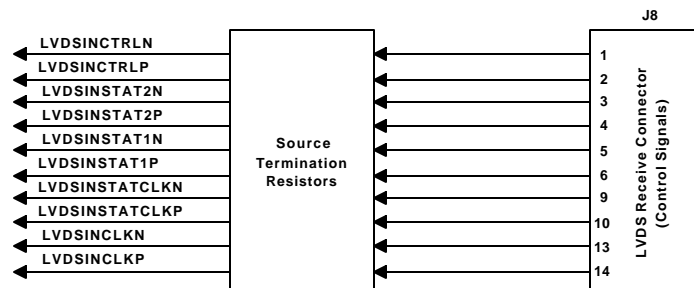
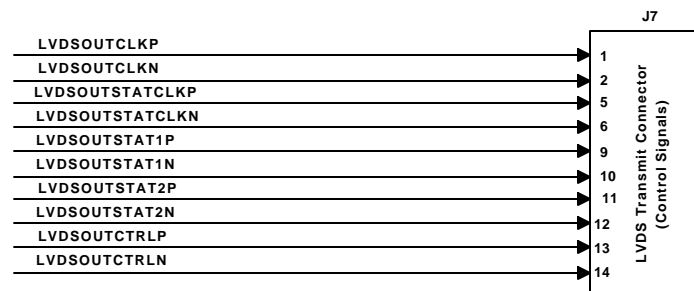


Figure 17– LVDS Receive Port



**Figure 18– LVDS Transmit and Receive Control Ports**

2.18.2 LVDS Port Signal Descriptions

The following table shows the LVDS port signal descriptions and the port signal assignments to the Virtex-II FPGA.

**Table 10 - LVDS Transmit Port Signal Descriptions**

Signal Name	Virtex-II Pin #	J4 Pin #	Description
LVDSOUT1N	H2	1	Negative Data Transmit Bit 1
LVDSOUT1P	H1	2	Positive Data Transmit Bit 1
LVDSOUT2N	J2	3	Negative Data Transmit Bit 2
LVDSOUT2P	J1	4	Positive Data Transmit Bit 2
LVDSOUT3N	K2	5	Negative Data Transmit Bit 3
LVDSOUT3P	K1	6	Positive Data Transmit Bit 3
LVDSOUT4N	E4	7	Negative Data Transmit Bit 4
LVDSOUT4P	E3	8	Positive Data Transmit Bit 4
<b>GND</b>	NA	9	Ground
<b>GND</b>	NA	10	Ground
LVDSOUT5N	F4	11	Negative Data Transmit Bit 5
LVDSOUT5P	F3	12	Positive Data Transmit Bit 5
LVDSOUT6N	G4	13	Negative Data Transmit Bit 6
LVDSOUT6P	G3	14	Positive Data Transmit Bit 6
LVDSOUT7N	H4	15	Negative Data Transmit Bit 7
LVDSOUT7P	H3	16	Positive Data Transmit Bit 7
LVDSOUT8N	J4	17	Negative Data Transmit Bit 8
LVDSOUT8P	J3	18	Positive Data Transmit Bit 8
<b>GND</b>	NA	19	Ground
<b>GND</b>	NA	20	Ground
LVDSOUT9N	K4	21	Negative Data Transmit Bit 9
LVDSOUT9P	K3	22	Positive Data Transmit Bit 9
LVDSOUT10N	L3	23	Negative Data Transmit Bit 10
LVDSOUT10P	L2	24	Positive Data Transmit Bit 10
LVDSOUT11N	L5	25	Negative Data Transmit Bit 11
LVDSOUT11P	L4	26	Positive Data Transmit Bit 11
LVDSOUT12N	E6	27	Negative Data Transmit Bit 12
LVDSOUT12P	E5	28	Positive Data Transmit Bit 12
<b>GND</b>	NA	29	Ground
<b>GND</b>	NA	30	Ground
LVDSOUT13N	F5	31	Negative Data Transmit Bit 13
LVDSOUT13P	G5	32	Positive Data Transmit Bit 13
LVDSOUT14N	H5	33	Negative Data Transmit Bit 14
LVDSOUT14P	J6	34	Positive Data Transmit Bit 14
LVDSOUT15N	J5	35	Negative Data Transmit Bit 15
LVDSOUT15P	K5	36	Positive Data Transmit Bit 15
LVDSOUT16N	K6	37	Negative Data Transmit Bit 16
LVDSOUT16P	L6	38	Positive Data Transmit Bit 16
<b>GND</b>	NA	39	Ground
<b>GND</b>	NA	40	Ground

**Table 11 - LVDS Receive Port Signal Descriptions**

Signal Name	Virtex-II Pin #	J6 Pin #	Description
<b>GND</b>	NA	1	Ground
<b>GND</b>	NA	2	Ground
LVDSIN1P	M2	3	Positive Data Receive Bit 1
LVDSIN1N	M1	4	Negative Data Receive Bit 1
LVDSIN2P	N2	5	Positive Data Receive Bit 2
LVDSIN2N	N1	6	Negative Data Receive Bit 2
LVDSIN3P	P2	7	Positive Data Receive Bit 3
LVDSIN3N	P1	8	Negative Data Receive Bit 3
LVDSIN4P	R2	9	Positive Data Receive Bit 4
LVDSIN4N	R1	10	Negative Data Receive Bit 4
<b>GND</b>	NA	11	Ground
<b>GND</b>	NA	12	Ground
LVDSIN5P	T2	13	Positive Data Receive Bit 5
LVDSIN5N	T1	14	Negative Data Receive Bit 5
LVDSIN6P	U2	15	Positive Data Receive Bit 6
LVDSIN6N	U1	16	Negative Data Receive Bit 6
LVDSIN7P	V2	17	Positive Data Receive Bit 7
LVDSIN7N	V1	18	Negative Data Receive Bit 7
LVDSIN8P	W2	19	Positive Data Receive Bit 8
LVDSIN8N	W1	20	Negative Data Receive Bit 8
<b>GND</b>	NA	21	Ground
<b>GND</b>	NA	22	Ground
LVDSIN9P	Y2	23	Positive Data Receive Bit 9
LVDSIN9N	Y1	24	Negative Data Receive Bit 9
LVDSIN10P	M6	25	Positive Data Receive Bit 10
LVDSIN10N	M5	26	Negative Data Receive Bit 10
LVDSIN11P	M4	27	Positive Data Receive Bit 11
LVDSIN11N	M3	28	Negative Data Receive Bit 11
LVDSIN12P	N4	29	Positive Data Receive Bit 12
LVDSIN12N	N3	30	Negative Data Receive Bit 12
<b>GND</b>	NA	31	Ground
<b>GND</b>	NA	32	Ground
LVDSIN13P	P4	33	Positive Data Receive Bit 13
LVDSIN13N	P3	34	Negative Data Receive Bit 13
LVDSIN14P	R4	35	Positive Data Receive Bit 14
LVDSIN14N	R3	36	Negative Data Receive Bit 14
LVDSIN15P	T4	37	Positive Data Receive Bit 15
LVDSIN15N	T3	38	Negative Data Receive Bit 15
LVDSIN16P	U4	39	Positive Data Receive Bit 16
LVDSIN16N	U3	40	Negative Data Receive Bit 16

**Table 12- LVDS Transmit Control Port Signal Descriptions**

Signal Name	Virtex-II Pin #	J7 Pin #	Description
LVDSOUTCLKP	C1	1	Positive Transmit Clock
LVDSOUTCLKN	C2	2	Negative Transmit Clock
<b>GND</b>	NA	3	Ground
<b>GND</b>	NA	4	Ground
LVDSOUTSTATCLKP	D1	5	Positive Transmit Status Clock
LVDSOUTSTATCLKN	D2	6	Negative Transmit Status Clock
<b>GND</b>	NA	7	Ground
<b>GND</b>	NA	8	Ground
LVDSOUTSTAT1P	E1	9	Positive Transmit Status1
LVDSOUTSTAT1N	E2	10	Negative Transmit Status1
LVDSOUTSTAT2P	F1	11	Positive Transmit Status2
LVDSOUTSTAT2N	F2	12	Negative Transmit Status2
LVDSOUTCTRLP	G1	13	Positive Transmit Control
LVDSOUCTRLN	G2	14	Negative Transmit Control

**Table 13- LVDS Receive Control Port Signal Descriptions**

Signal Name	Virtex-II Pin #	J8 Pin #	Description
LVDSINCTRLN	V3	1	Negative Receive Control
LVDSINCTRLP	V4	2	Positive Receive Control
LVDSINSTAT2N	N5	3	Negative Receive Status2
LVDSINSTAT2P	N6	4	Positive Receive Status2
LVDSINSTAT1N	P5	5	Negative Receive Status1
LVDSINSTAT1P	P6	6	Positive Receive Status1
<b>GND</b>	NA	7	Ground
<b>GND</b>	NA	8	Ground
LVDSINSTATCLKN	W11	9	Negative Receive Status Clock
LVDSINSTATCLKP	V11	10	Positive Receive Status Clock
<b>GND</b>	NA	11	Ground
<b>GND</b>	NA	12	Ground
LVDSINCLKN	AA11	13	Negative Receive Clock
LVDSINCLKP	Y11	14	Positive Receive Clock

### 2.18.3 Packet Over SONET Level 4 (PL4) application

One of the possible applications of the LVDS port on the Virtex-II development board is to prototype a high-speed Packet Over SONET Level 4 (PL4) interface. PL4 is used in point-to-point applications supporting OC-192 (10 Gbit/s) aggregate bandwidth.

The following figure shows how the Virtex-II along with the LVDS port on the Virtex-II development board can be used to implement the PL4 interface. This interface supports 16 bits of data and various miscellaneous signals to control the flow of the data transmission in each direction. Specifically, the status\_data\_tx[1:0] and status\_clk\_tx signals are used to control the transmit FIFO, while the status\_data\_rx[1:0] and status\_clk\_rx signals are used to control the receive FIFO.

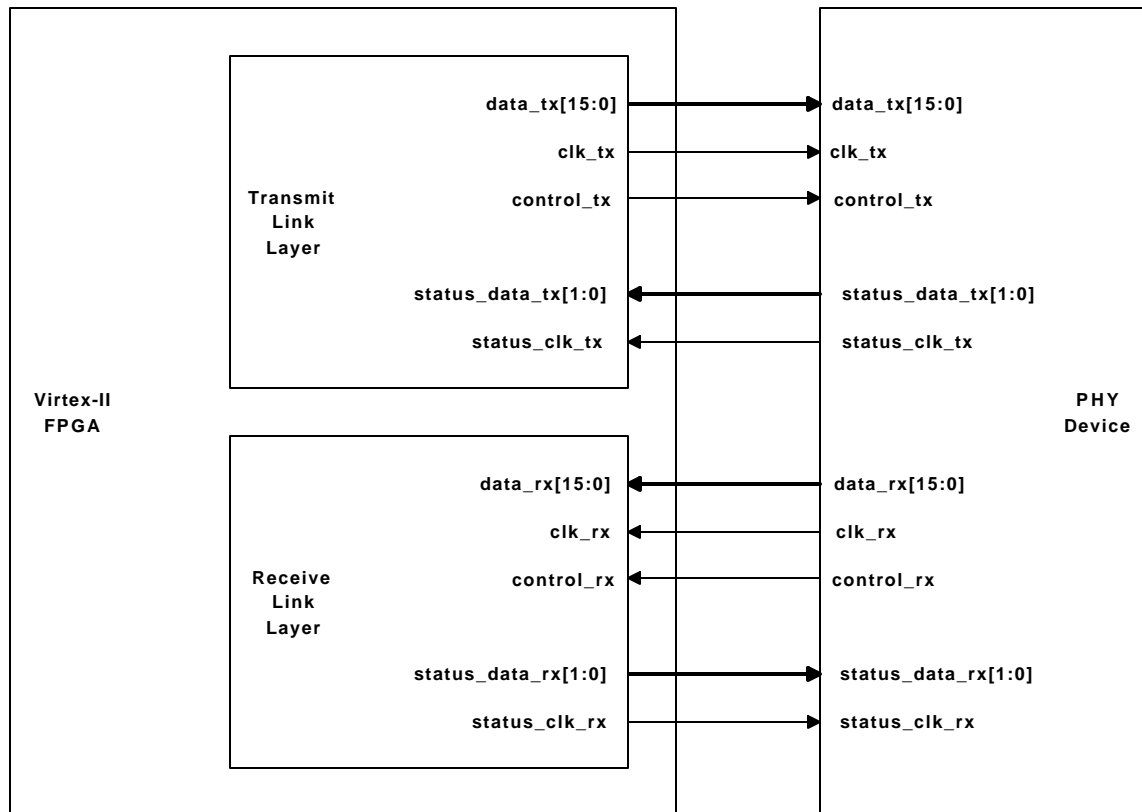


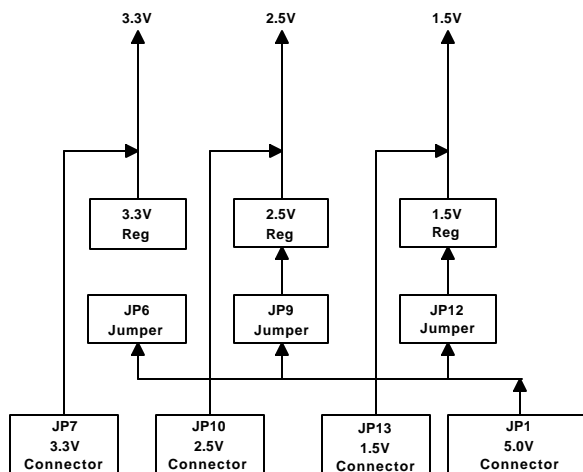
Figure 19 – Packet Over SONET Level 4 (PL4) Interface

### 2.19 Program Switch (SW2)

The Virtex-II system board provides a push button switch for initiating the configuration of the Virtex-II FPGA. This switch is used when the XC18V04 ISP PROM configures the Virtex-II FPGA. After programming of the XC18V04 ISP PROM, this switch can assert the PROGn signal. Upon activation of the PROGn signal, the XC18V04 ISP PROM initiates the configuration of the Virtex-II FPGA.

### 2.20 Voltage Regulators

The following figure shows the voltage regulators that are used on the Virtex-II development board to provide various on-board voltage sources. As shown in the following figure, JP1 connector is used to provide the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.5V, 2.5V, and 3.3V voltages.



**Figure 20 – Virtex-II Development Board Voltage Regulators**

For any one of the on-board voltages (1.5V, 2.5V, and 3.3V), if the current provided by the on-board regulator is not sufficient for some applications, the user can directly drive the voltage source and bypass the on-board regulators. This can be accomplished by removing jumpers JP6, JP9, and JP12 for voltages 3.3V through 1.5V respectively.

#### 2.20.1 Voltage Regulators Jumper Settings

The following table shows the jumper setting for the 3.3V, 2.5V, and the 1.5V supply voltages on the Virtex-II development board.

**Table 14 - Voltage Regulators Jumper Settings**

Jumper	Jumper Setting	3.3V Source	2.5V Source	1.5V Source
JP6	Open	External 3.3V supply via JP7 connector	NA	NA
	Closed	On-board 3.3V regulator	NA	NA
JP9	Open	NA	External 2.5V supply via JP10 connector	NA
	Closed	NA	On-board 2.5V regulator	NA
JP12	Open	NA	NA	External 1.5V supply via JP13 connector
	Closed	NA	NA	On-board 1.5V regulator

## 2.21 Virtex-II Configuration Mode Select

The following table shows the Virtex-II Configuration Mode Select jumper settings. The jumper position 7-8 (M3) is connected to the HSWAP\_EN pin of the Virtex-II FPGA. When this jumper is closed, the Virtex-II internal I/O pull-ups are enabled during the configuration.

**Table 15 - Virtex-II Configuration Mode Select**

Mode	PC Pull-up	J1			
		1-2 (M0)	3-4 (M1)	5-6 (M2)	7-8 (M3)
Master Serial	No	Closed	Closed	Closed	Closed
Master Serial	Yes	Closed	Closed	Closed	Open
Slave Serial	No	Open	Open	Open	Closed
Slave Serial	Yes	Open	Open	Open	Open
Master SelectMap	No	Closed	Open	Open	Closed
Master SelectMap	Yes	Closed	Open	Open	Open
Slave SelectMap	No	Open	Open	Closed	Closed
Slave SelectMap	Yes	Open	Open	Closed	Open
JTAG	No	Open	Closed	Open	Closed
JTAG	Yes	Open	Closed	Open	Open

## 2.22 P160 Expansion Module Signal Assignments

The following tables show the Virtex-II pin assignments to the P160 Expansion Module connectors (JX1 & JX2) located on the Virtex-II development board.

**Table 16 – JX1 User I/O Connector**

FPGA Pin #	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	FPGA Pin #
C19	TCK	A1	B1	FPGA.BITSTREAM	V18
NA	<b>GND</b>	A2	B2	SM.DOUT/BUSY	AB19
B20	TMS	A3	B3	FPGA.CCLK	Y19
NA	<b>Vin</b>	A4	B4	DONE	AB20
NA	TDI	A5	B5	INITn	AA19
NA	<b>GND</b>	A6	B6	PROGRAMn	A2
NA	TDO	A7	B7	NC	NA
NA	<b>3.3V</b>	A8	B8	LIOB8	L22
K22	LIOA9	A9	B9	LIOB9	L21
NA	<b>GND</b>	A10	B10	LIOB10	K21
J21	LIOA11	A11	B11	LIOB11	J22
NA	<b>2.5V</b>	A12	B12	LIOB12	H22
G22	LIOA13	A13	B13	LIOB13	H21
NA	<b>GND</b>	A14	B14	LIOB14	G21
F21	LIOA15	A15	B15	LIOB15	F22
NA	<b>Vin</b>	A16	B16	LIOB16	E22
D22	LIOA17	A17	B17	LIOB17	E21
NA	<b>GND</b>	A18	B18	LIOB18	D21
C21	LIOA19	A19	B19	LIOB19	C22
NA	<b>3.3V</b>	A20	B20	LIOB20	L18
L20	LIOA21	A21	B21	LIOB21	L19
NA	<b>GND</b>	A22	B22	LIOB22	K18
K19	LIOA23	A23	B23	LIOB23	K20
NA	<b>2.5V</b>	A24	B24	LIOB24	J20
H20	LIOA25	A25	B25	LIOB25	J19
NA	<b>GND</b>	A26	B26	LIOB26	H19
G19	LIOA27	A27	B27	LIOB27	G20
NA	<b>Vin</b>	A28	B28	LIOB28	E19
F20	LIOA29	A29	B29	LIOB29	E20
NA	<b>GND</b>	A30	B30	LIOB30	L17
F19	LIOA31	A31	B31	LIOB31	K17
NA	<b>3.3V</b>	A32	B32	LIOB32	J17
D11	LIOA33	A33	B33	LIOB33	J18
NA	<b>GND</b>	A34	B34	LIOB34	H18
C11	LIOA35	A35	B35	LIOB35	G18
NA	<b>2.5V</b>	A36	B36	LIOB36	F18
C8	LIOA37	A37	B37	LIOB37	E18
NA	<b>GND</b>	A38	B38	LIOB38	E11
D8	LIOA39	A39	B39	LIOB39	A10
NA	<b>Vin</b>	A40	B40	LIOB40	B10

Table 17 – JX2 User I/O Connector

FPGA Pin #	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	FPGA Pin #
AB18	RIOA1	A1	B1	<b>GND</b>	NA
AA16	RIOA2	A2	B2	RIOB2	Y15
AA17	RIOA3	A3	B3	<b>Vin</b>	NA
AB16	RIOA4	A4	B4	RIOB4	W14
AB17	RIOA5	A5	B5	<b>GND</b>	NA
AA15	RIOA6	A6	B6	RIOB6	Y14
W17	RIOA7	A7	B7	<b>3.3V</b>	NA
AB15	RIOA8	A8	B8	RIOB8	W13
Y17	RIOA9	A9	B9	<b>GND</b>	NA
AA14	RIOA10	A10	B10	RIOB10	Y13
W16	RIOA11	A11	B11	<b>2.5V</b>	NA
AB14	RIOA12	A12	B12	RIOB12	V13
Y16	RIOA13	A13	B13	<b>GND</b>	NA
AA13	RIOA14	A14	B14	RIOB14	Y12
V16	RIOA15	A15	B15	<b>Vin</b>	NA
AB13	RIOA16	A16	B16	RIOB16	W12
W15	RIOA17	A17	B17	<b>GND</b>	NA
AA12	RIOA18	A18	B18	RIOB18	V12
V14	RIOA19	A19	B19	<b>3.3V</b>	NA
AB12	RIOA20	A20	B20	RIOB20	V10
U14	RIOA21	A21	B21	<b>GND</b>	NA
AB9	RIOA22	A22	B22	RIOB22	Y10
U13	RIOA23	A23	B23	<b>2.5V</b>	NA
AA9	RIOA24	A24	B24	RIOB24	W10
U12	RIOA25	A25	B25	<b>GND</b>	NA
AB8	RIOA26	A26	B26	RIOB26	Y9
U11	RIOA27	A27	B27	<b>Vin</b>	NA
AA8	RIOA28	A28	B28	RIOB28	W9
U10	RIOA29	A29	B29	<b>GND</b>	NA
AB7	RIOA30	A30	B30	RIOB30	Y8
U9	RIOA31	A31	B31	<b>3.3V</b>	NA
AA7	RIOA32	A32	B32	RIOB32	W8
V9	RIOA33	A33	B33	<b>GND</b>	NA
AB6	RIOA34	A34	B34	RIOB34	Y7
V8	RIOA35	A35	B35	<b>2.5V</b>	NA
AA6	RIOA36	A36	B36	RIOB36	W7
V7	RIOA37	A37	B37	<b>GND</b>	NA
AB5	RIOA38	A38	B38	RIOB38	Y6
V6	RIOA39	A39	B39	<b>Vin</b>	NA
AA5	RIOA40	A40	B40	RIOB40	W6

### 3 Design Download

The Virtex-II development board supports multiple methods of configuring the Virtex-II FPGA. The JTAG port on the Virtex-II development board can be used to directly configure the Virtex-II FPGA, or to program the on-board XC18V04 ISP PROM. Once the ISP PROM is programmed, it can be used to configure the Virtex-II FPGA. The SelectMap/Slave Serial port on this development board can also be used to configure the Virtex-II FPGA. The following figure shows the setup for all Virtex-II FPGA configuration modes that are supported on the Virtex-II development board.

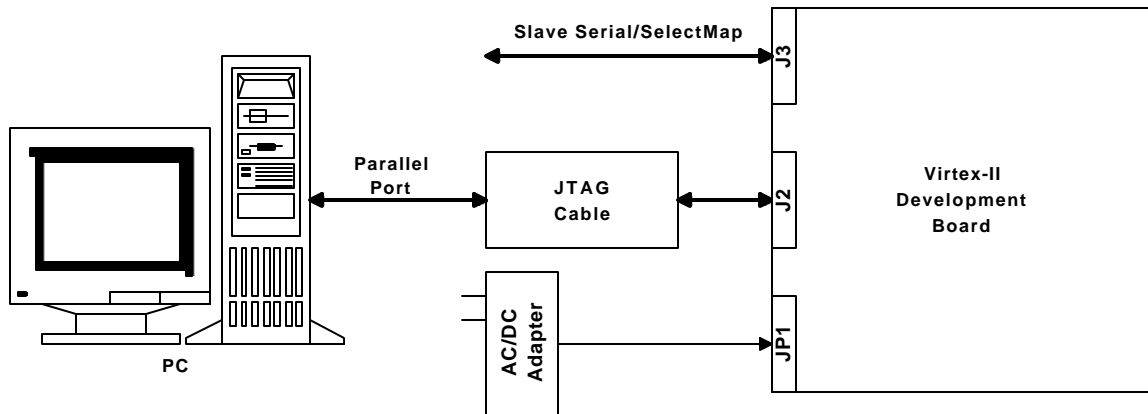


Figure 21 – Download Setup

#### 3.1 JTAG Interface

The J2 JTAG connector on the Virtex-II development board can be used to configure the Virtex-II or to program the on-board XC18V04 ISP PROM. The Insight JTAG cable is connected to the Virtex-II development board via J2 at one end and to the PC parallel port at the other end.

##### 3.1.1 Configuring the Virtex-II FPGA

When the JTAG port is used to configure the Virtex-II FPGA, the following steps must be taken:

- Using Table 15 set the Configuration Mode of the Virtex-II FPGA to JTAG Mode.
- Install the JP25 jumper if the P160 module is not present
- Use the Xilinx JTAG programmer utility (iMPACT) to load the design bit file into the Virtex-II FPGA. You will need to associate the ISP PROM with either a dummy .mcs file, or a .bsd file to allow the JTAG programming software to pass data through the ISP PROM.

##### 3.1.2 Programming the XC18V04 ISP PROM

When the JTAG port is used to program the ISP PROM, the following steps must be taken:

- Using Table 15 set the Configuration Mode of the Virtex-II FPGA to Master Serial or Master SelectMap Mode.
- Install the JP25 jumper if the P160 module is not present
- Use the Xilinx JTAG programmer utility (iMPACT) to load the design mcs file into the ISP PROM. You will need to associate the FPGA with either a dummy .bit file or a .bsd file to allow the JTAG programming software to pass data through the FPGA.

- Upon programming of the 18V04 ISP PROM, the on-board PROGn push button switch (SW2) is used to initiate the Virtex-II FPGA configuration.

### **3.2 Slave Serial Interface**

In this mode, an external source provides the configuration bit stream and the configuration clock (CCLK) to the Virtex-II FPGA. Refer to Table 15 for setting up the Configuration Mode pins.

### **3.3 Master SelectMap Interface**

In this mode, the following steps must be taken:

- Using Table 15 set the Configuration Mode of the Virtex-II FPGA to Master SelectMap Mode.
- Install the JP25 jumper if the I/O module is not present
- Install the JP27 jumper
- Use the Xilinx JTAG programmer utility to load the design mcs file into the ISP PROM. You will need to associate the FPGA with either a dummy .bit file or a .bsd file to allow the JTAG programming software to pass data through the FPGA.
- Upon programming of the 18V04 ISP PROM, the on-board PROGn push button switch (SW2) is used to initiate the Virtex-II FPGA configuration.

### **3.4 Slave SelectMap Interface**

In this mode, an external source provides the configuration bit stream and the configuration clock (CCLK) to the Virtex-II FPGA. Refer to Table 15 for setting up the Configuration Mode pins.

## Revision History

<b>V1.0</b>	<b>Initial release</b>	<b>12/5/01</b>
<b>V1.1</b>	<b>Update</b> Section 2.1 heading changed Section 5 references to table 17 corrected to table 15 Figure 19 corrected	<b>12/19/01</b>
<b>V1.2</b>	<b>Update</b> Figure 7 and table 6 corrected	<b>12/30/01</b>
<b>V1.3</b>	<b>Update</b> Figure 16-18 and table 10-11 corrected Table 15 corrected for PC Pull-up settings Removed P160 Module Documentation (Now as separate documents)	<b>2/14/02</b>
<b>V1.4</b>	<b>Update</b> Corrected 24MHz/100MHz wording in section 2.4 Updated Memec Design logo	<b>5/29/02</b>

## **Appendix A – Virtex-II System Board Schematics**