

# FPGA Resynthesis for Area and Reliability

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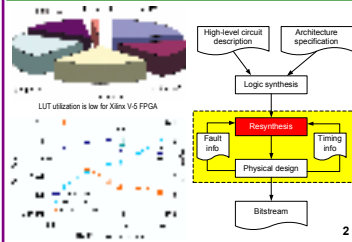
## Abstract

Resynthesis, a circuit rewriting technique in FPGA CAD flow, has emerged to cope with the inherent NP-hardness of many CAD tasks and the ever increasing design complexity and logic capacity of FPGAs. Targeting area and reliability optimization, this project proposed two logic resynthesis algorithms by applying an efficient SAT-based Boolean matching as the optimization engine. In contrast to existing resynthesis, our proposed algorithms explore multiple design freedoms and architecture features in order to achieve better quality.

## Motivations

- Heuristic FPGA synthesis results in sub-optimal
  - 500X gap exists between optimal and heuristic technology mapping [Cong, FPGA'06]
  - Growing design complexity and FPGA capacity increases the optimality gap
- Resynthesis is needed to improve quality (area/performance/power/reliability)
  - Rewrite the logic or physical design
  - Perform iterations for design closure

## Resynthesis for Area & SER



## Proposed Resynthesis

- Resynthesis based on LUT reconfiguration
  - Leverage the inherent flexibility in LUT-based FPGA
  - Reduce area without performance degradation
  - Increase reliability with negligible area overhead
- A SAT-based Boolean matching is the key
  - A formal method ensuring correct-by-construction
  - Flexible enough to deal with heterogeneous FPGA
  - Efficient proposed implementation for scalability

## SAT-based Boolean Matching

Boolean matching answers a Yes-No question

- Can PLB  $p$  implement Boolean function  $f$ ?
- If yes, give the configuration bits for all LUTs in  $p$ .

## Exploring Symmetries in BM

- SAT-BM can be much faster if we explore symmetries in
  - Boolean function, e.g.,  $b$  and  $c$  are symmetric in  $a(b+c)$
  - FPGA PLB architecture, e.g., pins in an LUT are symmetric

## Area Reduction Results

Circuit	ABC	Comb	LUT#	Seq	Comb	Seq
bigkey	1261	1261	(0.00%)	1244	(-1.35%)	11693
cdma	4510	4167	(-1.02%)	4116	(-2.23%)	2697
ell-est	874	874	(0.00%)	873	(-0.15%)	855
gaip	1554	1350	(-14.41%)	1350	(-13.90%)	705
golfic	441	418	(-4.99%)	418	(-4.99%)	32
hmc	2841	2362	(-17.21%)	2362	(-17.21%)	1264
h201	44	41	(-6.82%)	37	(-16.81%)	186
h20477	3134	3105	(-0.93%)	3117	(-0.94%)	3466
h3894	3700	3654	(-1.27%)	3650	(-1.27%)	2997
henny	949	935	(-1.16%)	934	(-1.27%)	1331
hve	1883	1820	(-3.35%)	1811	(-5.07%)	1601
hwo	1	1	(0.00%)	1	(0.00%)	1

Sequential resynthesis obtains up to 9% area

Factors to sequential resynthesis quality

- Sequential structure
- PLB templates, the number of iterations

## Stochastic Resynthesis

Both faults in LUT configuration and interconnect are considered and modeled as random variables.

Different synthesis algorithms lead to different area-robustness tradeoffs

Stochastic resynthesis maximizes the yield rate under random faults

- No testing overhead, negligible area/performance overhead

## Fault-Tolerant Boolean Matching

- Input:
  - PLB template  $H$  and Boolean function  $F$
  - Fault rate for the inputs and SRAM bits of PLB  $H$
- Output:
  - Either that  $F$  cannot be implemented by PLB  $H$
  - Or that the configuration of  $H$  which minimizes the probability that faults are observable in the output of the PLB under all input vectors
- Fault-Tolerant BM task breakdown
  - Find multiple Boolean matching
  - Evaluate the stochastic fault rate

## Deterministic SAT vs. SSAT

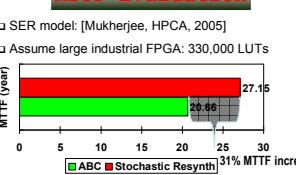


## Robust PLB Structure

Robust PLB structure introduces more potential for don't-cares

Stochastic resynthesis maximizes don't-cares w/ FTBM and robust PLB

## MTTF Evaluation



## References

- Y. Hu, V. Shih, R. Majumdar and L. He, "Exploiting Symmetries to Speedup SAT-based Boolean Matching for Logic Synthesis of FPGAs", TCAD 2008.
- Y. Hu, V. Shih, R. Majumdar and L. He, "FPGA Area Reduction by Multi-Output Function Based Sequential Resynthesis", DAC 2008.
- Y. Hu, Z. Feng, R. Majumdar and L. He, "Robust FPGA Resynthesis Based on Fault-Tolerant Boolean Matching", ICCAD 2008.