

# Minimizing Skew Clock Considering Time-Variant Temperature Gradient

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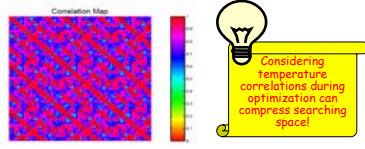
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## Abstract

Considering the time-variant temperature gradient with automatic correlation extraction, we develop a PERTurbation based Clock Optimization (PECO). For a given clock topology, we minimize the worst case skew without asking for the worst case temperature map. We optimize the clock embedding by a parameterized model, which is compressed considering the temperature correlation. The experimental results show that our algorithm reduces worst-case skew by up to 5X compared to the existing zero-skew based ZST/DME method with small (up to 1%) wirelength overhead.

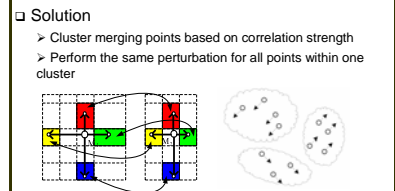
## Temperature Correlation

- Spatial and Time Correlation: Strong correlations exist between temperature for different workloads and different regions on chip.
  - Resource sharing between different workloads cause temporal correlation.

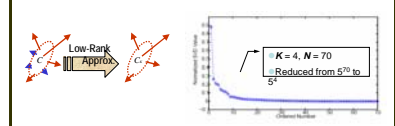


## Perturbation Compression

- Motivations
  - Spatial and temporal correlation of the temperature values excludes the need to exhaustively calculate all perturbation combinations
  - Highly correlated merging points should be perturbed in the same fashion.

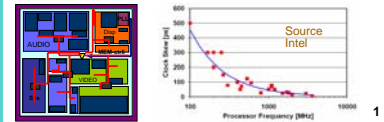


- Solution
  - Cluster merging points based on correlation strength
  - Perform the same perturbation for all points within one cluster
- Problem formulation
  - Partition  $N$  merging points into  $K$  clusters
  - Correlation matrix  $C$  of them is a low-rank matrix,  $N \gg K$
- Partition Algorithm
  - Decide the clustering number  $K$  [Singular Value Decomposition (SVD) reveal the real rank ( $K$ ) information from  $C$ ]
  - Partition the merging points into  $K$  clusters [K-Means clustering]



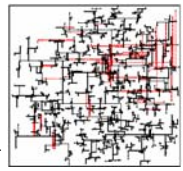
## Clock Tree Synthesis

- Clock signals synchronize data transfer between functional elements in synchronous design.
- Clock skew becomes the No. 1 concern in clock tree synthesis for high performance designs.



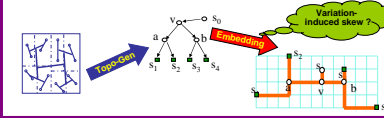
## Problem Formulation

- Given:
  - The source, sinks and an initial embedding of the clock tree
  - Each region is modeled by mean and variance for temperature and correlation (co-variance) between variations.
- To find:
  - An re-embedding of the clock tree.
- Objective:
  - Minimize the worse case skew under the temperature variation.

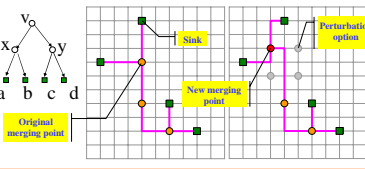


## Clock Skew Minimization

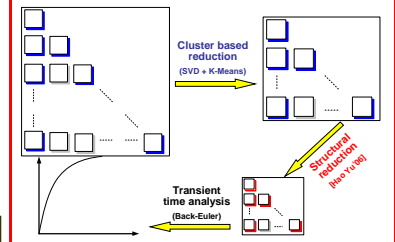
- Source of clock skew
  - Un-balanced clock tree topology
  - Process, supply voltage and temperature variations
  - Uncertainty from workload
- Methodologies for skew minimization
  - Active de-skew circuit using micro-controller [Rusu'00]
  - Passive balanced embedding by CAD [Tsay'91 [Edahiro'91] [Chao'92] [Boese'92] [Cong'98]



## Re-embedding Process

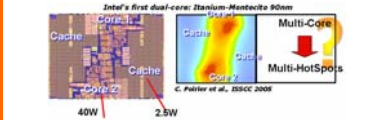


## Structural Reduction



## Spatial Temperature Variation

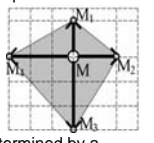
- Non-uniform power density generates on-chip temperature gradient



- Clock tree embedding considering the temperature variation TACO [Cho'05]
  - Ignore the time-variant temperature under different workloads

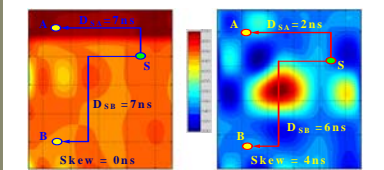
## Merging point relocation

- The impact of temperature variation to merging point is confined by a perturbation radius
  - Consider east, west, north, south and origin to minimize wire-length overhead
  - The radius is determined by the local temperature gradient similar to TACO
- The embedding path is determined by a shortest standard deviation path
- The resistance is extracted as the sum of the mean values on the embedding path



## Temporal Temperature Variation

- Significantly different temperature maps from two SPEC2000 applications: Ammp, Gzip



Dilemma: Optimizing skew for one application hurts the other...

## State matrix construction

- Clock tree by perturbed Modified Nodal Analysis (MNA)
  - $x$  is for source and merging points
  - $L$  selects sink response
  - Defining a new state variable with both nominal ( $x$ ) and perturbed state variable ( $\delta x$ )
- Structured and parameterized state matrix

$$\begin{cases} [(G_0 + \delta G_1) + s(C_1 + \delta C_1)] \cdot (x + \delta x_1) = B_1 u \\ [(G_0 + \delta G_2) + s(C_2 + \delta C_2)] \cdot (x + \delta x_2) = B_2 u \\ [(G_0 + \delta G_3) + s(C_3 + \delta C_3)] \cdot (x + \delta x_3) = B_3 u \end{cases} \quad Gp = \begin{bmatrix} G_1 & 0 & \dots & 0 & 0 & 0 \\ 0 & G_2 & \dots & 0 & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & G_N & 0 & 0 \\ 0 & 0 & \dots & 0 & 0 & 0 \end{bmatrix}$$

Number of perturbation options  $1 - 5^N$  is huge! ( $N$  is the merging point number)

## Experimental Results

- Worst-case skew distributions
  - Simulated under 100 temperature maps
- PECO reduces the worst-case skew by up to 5x compared to ZST/DME with less than 1% wire length overhead.
  - Skew measured in higher-order delay model considering temperature variations for all applications
  - Skew reduction increases for larger clock nets

## References

Hao Yu, Yu Hu, Chun-Chen Liu and Lei He, "Minimal Skew Clock Embedding Considering Time-Variant Temperature Gradient", International Symposium on Physical Design, 2007.