A Fully Differential Wide-Band Operational Amplifier

EE215A Final Project Report

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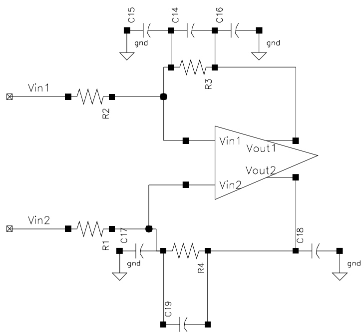

Fig. 1. A low-pass filter

Gain	$5 \pm 1\%$
3-dB Bandwidth	9.95MHz$\pm 1\%$
Diff. output swing	1.6V
HD3	$< 1\%$
Open loop phase margin	$> 60°$
Supply voltage	1.8V
Power dissipation	minimum

TABLE I
DESIGN SPECIFICATIONS

I. DESIGN SPECIFICATIONS AND INITIAL DECISION

A fully differential wide-band operational amplifier is designed for a 1st-order RC low-pass filter. The low-pass filter and specifications are shown in Fig. 1 and Table I. The output is used to drive an identical stage. Given the low load resistance ($R_1 = 2k\Omega$), we realized that using a single-stage amplifier is impossible to achieve a reasonably high gain (for example, DC gain of 594 is required to reach 1% error on the closed loop gain). Thus, a two-stage structure is mandatory. Initially, we design the first stage to be a fully differential pairs with active load, which provides most of the required gain. The second stage is a simple common source stage which provides large output swing and additional gain. The detailed analysis is presented in the next section.

II. ANALYSIS UNDER IDEAL CONDITIONS

We model the operational amplifier as a voltage-controlled voltage source with finite gain. The diagram is shown in Figure 2. The open loop voltage gain is A, output resistance R_o. We want to find the conditions on A and R_{out} to satisfy the gain requirement.

A. Loaded Gain and Output Resistance

Since this is a shunt-shunt feedback, it is convenient to convert the input voltage source into an input current source and compute the transimpedence R_o. We break the feedback loop in Fig. 3. First, we ignore all the capacitance to compute the DC gain. The DC transimpedence is given as

$$R_o = -\frac{A(R_2 \parallel R_L)(R_1 \parallel R_2)}{R_{out} + (R_2 \parallel R_L)}. \tag{1}$$

The feedback factor is

$$f = -\frac{1}{R_2}. \tag{2}$$

Thus the overall gain is

$$A_{fb} = \frac{R_o}{(1 + fR_o)R_1} = \left(\frac{A(R_2 \parallel R_L)(R_1 \parallel R_2)}{A(R_2 \parallel R_L)(R_1 \parallel R_2) + R_{out} + (R_2 \parallel R_L)}\right) \times \left(-\frac{R_2}{R_1}\right). \tag{3}$$

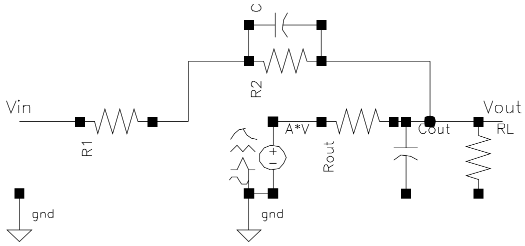

Fig. 2. Ideal Op-Amp

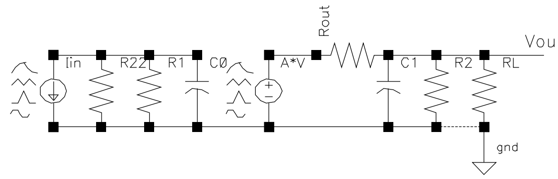

Fig. 3. diagram for gain and output resistance calculation

Since $4.95 \leq |A_{fb}| \leq 5.0$, the first term in (3) must be greater than 99%. This results in the following inequality.

$$A \geq 0.3564 R_{out} + 594 \tag{4}$$

Eq. 4 relates the open loop gain and output resistance of the op-amp. For example, if $R_{out} = 10k$, then $A \geq 4158$.

B. Dominant Pole

In order to satisfy the 3-dB bandwidth requirement, we want to compute the dominant pole of the close loop system and find the conditions on the open loop gain A and bandwidth. This can be done by including capacitance in the previous calculation. Denote $R_3 = R_2 \parallel R_L = R_2 \parallel R_1$, $C_2 = C1 \parallel C_{out}$. Eq. 3 becomes

$$\begin{aligned} A_{fb} &= \left(\frac{A(R_3 \parallel \frac{1}{sC_2})(R_3 \parallel \frac{1}{sC_1})(R_2 \parallel \frac{1}{sC_1})}{A(R_3 \parallel \frac{1}{sC_2})(R_3 \parallel \frac{1}{sC_1}) + (R_{out} + (R_3 \parallel \frac{1}{sC_2})(R_2 \parallel \frac{1}{sC_1})} \right) \times \left(-\frac{1}{R_1} \right) \\ &= -\frac{AR_3^2 R_2 / R_1}{s^2(R_3^2 C_1 C_2 R_{out} R_2) + s(AR_3^2 R_2 C_1 + R_{out} R_2 R_3 (C_1 + C_2)) + (AR_3^2 + R_{out} R_2 + R_3 R_2)}. \end{aligned} \tag{5}$$

The dominant pole is given by

$$\begin{aligned} \omega_p &= \frac{AR_3^2 + R_{out} R_2 + R_3 R_2}{AR_3^2 R_2 C_1 + R_{out} R_2 R_3 (C_1 + C_2) + R_3^2 R_2 C_1} \\ &= \frac{1}{R_2 C_1} \left(\frac{1 + R_{out} R_2 / (AR_3^2) + R_2 / (AR_3)}{1 + R_{out}(C_1 + C_2)/(AR_3 C_1) + 1/A} \right). \end{aligned} \tag{6}$$

The second term in (6) must be greater than 99% which gives the following inequality.

$$A \geq 99 \frac{R_{out}(C_1 + C_2)}{R_3 C_1} - \frac{600 R_{out}}{R_3}. \tag{7}$$

Notice $C_1 = 1.6pF, C_2 = C_1 + C_{out}$, we have the following requirement on the gain 3-dB frequency product:

$$A f_{3dB} \geq 3.13 \text{ GHz} \tag{8}$$

C. Phase Margin

Two-stage amplifier has two proximate dominant poles at the outputs of both stages. Proper compensation is needed to obtain a $60°$ phase margin. In our design, this is done by adding a capacitor C_0 and a resistor R_0 between the outputs of the two stages. Adding C_0 splits the two low frequency poles. Inserting R_0 introduces a left half plane (LHP) zero to help prevent the phase drop at low frequency. The exact value of the compensation capacitance is decided through simulations. The frequency of zero is finely tuned so that it is located near the second pole, and this gives rise to the best possible phase margin. Again, this is done through parametric simulation with Cadence.

III. SIMPLE DIFFERENTIAL AMPLIFIER

A. Design Summary

The main circuitry of a simple two-stage amplifier is shown in Fig. 4. The compensation circuitry consists of R_0 and C_0. The gate of M2 and M3 are controlled by the bias circuitry, and the gate of M11 is connected to the output of common mode feedback circuitry. The bias currents for the first and second stages are 0.6mA and 1.92mA respectively. The relatively high current is due to the high bandwidth requirement. This places a stringent condition on the amplifier pole locations. The bias circuitry is shown in Fig. 5. A ideal current source is used. Wire vg2, vg26, and vg15 are connected to the gate of M2, M26, and M15. The common mode feedback circuit uses differential pairs, as shown in Fig. 6. The differential outputs of the amplifier are connected to vg21 and vg24. Wire vg11 is routed to the gate of M11, which controls the tail current of the different pair at first stage. The common mode voltage vcm is set to 0.9V using a ideal voltage source. Caution is needed in sizing transistors M21∼M24. Their overdrive voltages should be high enough such that the different pairs in common mode feedback circuitry remain on for the entire differential output range. In order to minimize the power dissipation, the bias current in common mode feedback is kept low by adjusting the transistor sizes.

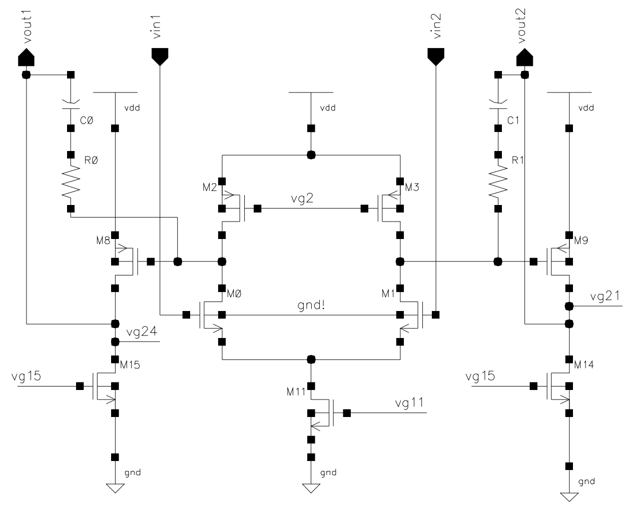

Fig. 4. Main circuitry for simple differential pair

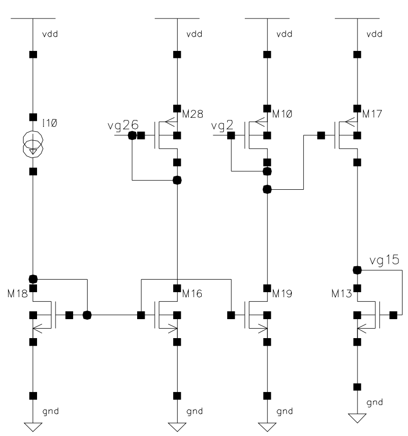

Fig. 5. Bias circuitry for simple differential pair

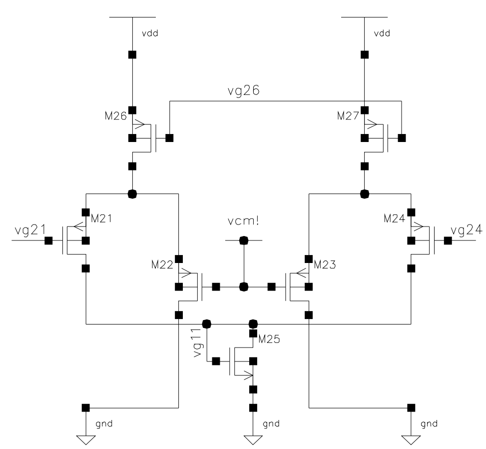

Fig. 6. Common mode feedback

TABLE II
TRANSISTORS IN SIMPLE DIFFERENTIAL PAIR

Device	$W/L(\mu m/\mu m)$	m	v_{sat} (mV)	g_m (mA/V)	current (mA)
M0,M1	$1.26/0.315$	60	126.1	8.969	0.5992
M2,M3	$3.6/0.9$	15	469.4	1.739	0.5992
M8,M9	$0.72/0.18$	160	216.9	14.1	2.001
M10	$3.6/0.9$	1	469.4	0.1179	0.0406
M11	$0.72/0.18$	60	144.7	13.61	1.198
M13	$1/0.25$	1	337.5	0.3625	0.1206
M14, M15	$1/0.25$	17	337.5	6.121	2.029
M16	$2/0.5$	1	130.3	0.1527	0.010
M17	$3.6/0.9$	3	469.4	0.350	0.120
M18	$2/0.5$	1	67.41	0.2076	0.010
M19	$2/0.5$	4	130.3	0.588	0.041
M21$\sim$ M24	$0.72/0.18$	1	202.8	0.082	0.010
M25	$0.72/0.18$	1	145.4	0.2394	0.021
M26, M27	$2/0.5$	40	67.39	0.404	0.021

TABLE III
SIMULATION RESULT FOR TWO STRUCTURES

	Simple	Cascode
Open-loop gain	621	1415
Closed-loop gain	4.95	4.978
Open-loop 3-dB BW	2.969 MHz	1.221 MHz
Closed-loop 3-dB BW	9.724 MHz	9.694 MHz
Diff. output swing	1.6V	1.6V
HD3	0.5%	0.17%
Compensation	$R_o = 200\Omega$	$R_o = 510\Omega$
	$C_o = 580$fF	$C_o = 156$fF
CMFB	$V_{cm} = 0.9$ V	$V_{cm} = 0.95$ V
Open-loop phase margin	$60.04°$	$60.03°$
Power dissipation	9.7832 mW	8.9532 mW

B. Simulation

The transistor sizes, DC current, and small signal parameters (g_m, v_{sat}) are listed in Table II. The channel lengths of transistors on the second stage are minimized $0.18\mu m$because the load resistor dictates the gain on the second stage. The channel lengths of the transistors on the first stage is determined by the tradeoff between gain and bandwidth (phase margin). Increasing channel length leads to higher gain but introduces more capacitance on the intermediate output. We will have more on these tradeoffs in the discussion section. The circuit was simulated and the result is reported in Table III. The output with a full 1.72V swing is shown in Fig. 7, when the input was a sinusoid at 2MHz. The 3rd harmonics distortion is obtained using the discrete Fourier transform. While all other requirements are satisfied, we only reach a close loop bandwidth of 9.724 MHz. We conceive that increasing the current on the second stage may lead to a better result, but we did not pursue further on the direction. Table III also includes the result of a design using telescopic cascode at the first stage, which we will discuss in the next section.

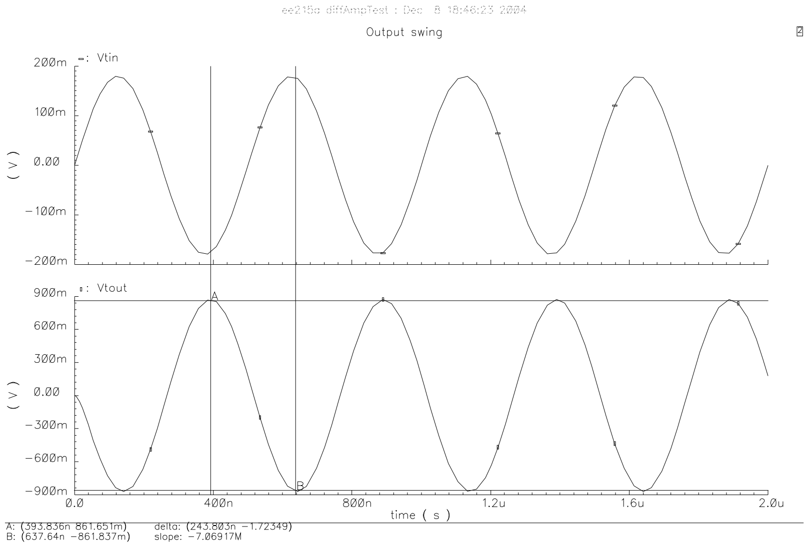

Fig. 7. Output Swing for simple differential pair

IV. Cascoded Differential Amplifier

In the previous design, we used a simple differential pair as the first stage. Since the cascode structure can achieve higher gain, it is interesting to see if power dissipation can be improved by using this structure. We also implemented a cascode differential pair design. The main circuitry and bias circuitry are given in Fig. 8 and Fig. 9 respectively. In this high swing bias circuitry, transistor M31 is design to be in triode region, and it sets the V_{ds} of M2 and M3. Bias vg20 needs to be appropriately chosen such that M19 and M20 work in saturation region. The corresponding transistor sizes and their operational conditions are listed in Table IV. The common mode feedback is the same as the previous one as shown in Fig. 6, so we choose not to list their transistors.

The best result we got is presented in Table III. Although using a cascode at the first stage helps enhance the gain substantially, the bandwidth becomes slight worst than our previous design. This is understandable since the dominant pole in the cascode design is located at lower frequency than the simple design.

TABLE IV
Transistors in the Cascoded Amplifier

Device	$W/L(\mu m/\mu m)$	m	v_{sat} (mV)	g_m (mA/V)	current (mA)
M0,M1	$0.72/0.18$	16	148.9	3.296	0.303
M2,M3	$0.72/0.18$	40	186.8	2.573	0.303
M8,M9	$0.72/0.18$	160	216.5	14.23	2.02
M14, M15	$0.72/0.18$	40	204.9	3.144	0.5
M16	$2/0.5$	1	130.3	0.1527	0.010
M17, M18	$0.72/0.18$	20	250.1	1.818	0.303
M19, M20	$0.72/0.18$	20	126	4.036	0.303
M29	$1/18$	1	396	0.1	0.028
M30, M33	$0.72/0.18$	2	250.7	0.1811	0.030
M35 $\sim$ M37	$0.72/0.18$	2	118.1	0.376	0.027
M31 (triode)	$4/1$	1	424	64.84	0.027
M32	$0.72/0.18$	4	186.7	0.2569	0.03
M34	$16/1$	1	196	0.221	0.028

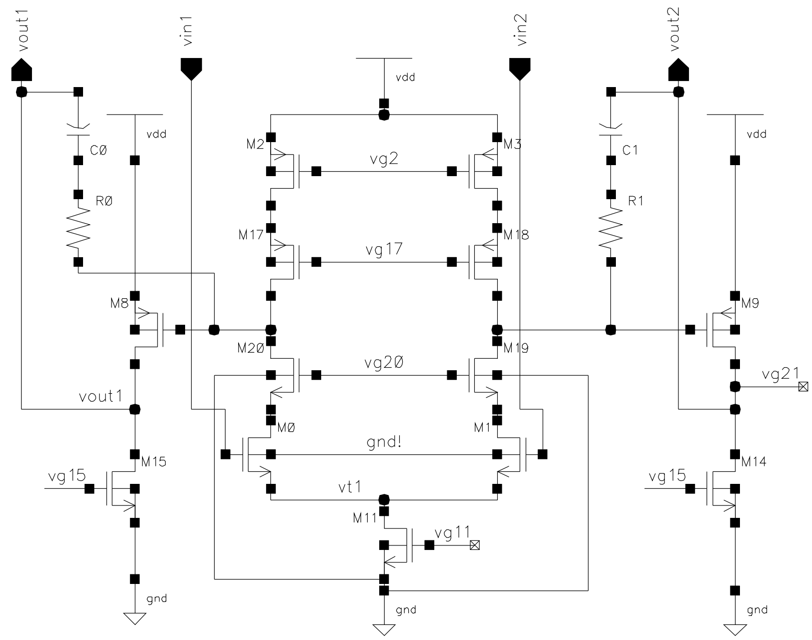

Fig. 8. Cascoded main circuitry

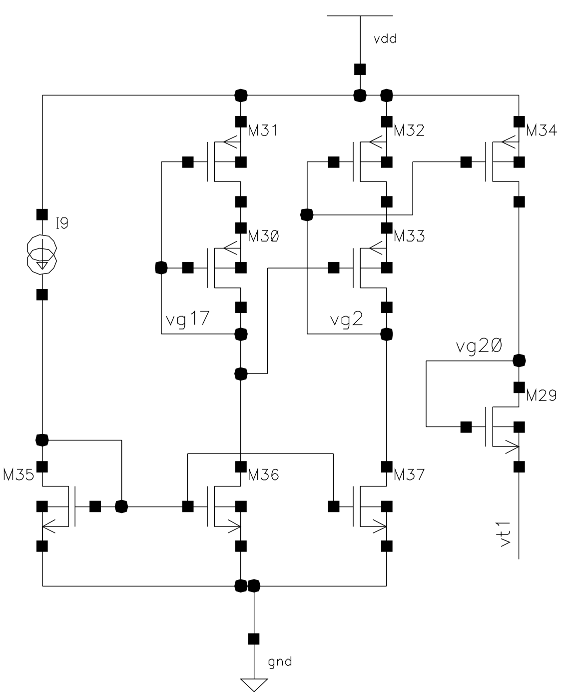

Fig. 9. Bias circuitry for the cascode

V. Discussion

In this section we discuss the tradeoffs involved in adjusting the designing parameters such as the device sizes and bias current when the simple design in section III is used. The results are summarized in Table V. We use g_{m1} and g_{m2} to denote the transconductance of the first and second stages. p_1 and p_2 indicate the dominant and secondary poles. R_{out1} and R_{out2} mean the output resistances of first and second stages. We have:

$$p_1 \approx \frac{1}{g_{m2}R_{out1}(R_{out2}||R_L)C_0}$$

$$p_2 \approx \frac{g_{m2}}{C_i + C_L}$$

$$G_{open} = g_{m1}R_{out1}g_{m2}(R_{out2}||R_L)$$

1) When the bias current on the first stage I_{D1} increases, g_{m1}, p_1 increases and R_{out1} decreases. This results in PM$\searrow$, BW$\nearrow$ and $G_{close}\searrow$.
2) When m_0 (multiplier of transistor M0) increases, g_{m1} and C_i increase and p_2 drops. Thus, PM$\searrow$, BW$\nearrow$ and $G_{close}\nearrow$.
3) Raising L_0 (channel length of transistor M0) leads to larger R_{out1}, C_i, and smaller p_1, p_2. Consequently, PM$\searrow$, BW$\searrow$ and $G_{close}\nearrow$.
4) When the bias current on the second stage I_{D2} rises, g_{m2} and p_2 increase, and p_1 decreases. Hence, PM$\nearrow$, BW$\nearrow$, and $G_{close}\nearrow$.
5) Using a larger multiplier m_8 on transistor M8 results in larger g_{m2}, C_i, C_L. Therefore, BW$\searrow$, $G_{close}\nearrow$. The behavior of PM can be more complicated since g_{m2} and C_i cause opposite changes on phase margin.
6) When increase m_8 (the channel length of M8), R_{out2}, C_i, C_L increase, and p_2 decreases. As a result, PM$\searrow$, BW$\searrow$. G_{close} changes slightly since R_{out2} is in parallel with R_L.

Other parameters such as bias current and the sizes of transistors in CMFB circuitry has less effect on the performance of the amplifier.

TABLE V

Tradeoffs on adjusting designing parameters

		Phase Margin	Bandwidth	Gain
Stage 1	$I_{D1}\nearrow$	$\searrow$	$\nearrow$	$\searrow$
	$m_0\nearrow$	$\searrow$	$\nearrow$	$\nearrow$
	$L_0\nearrow$	$\searrow$	$\searrow$	$\nearrow$
Stage 2	$I_{D2}\nearrow$	$\nearrow$	$\nearrow$	$\nearrow$
	$m_8\nearrow$	$\nearrow\searrow$	$\searrow$	$\nearrow$
	$L_8\nearrow$	$\searrow$	$\searrow$	$\longrightarrow$