EE 215b Final Project
256 x 64 CAM

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Maximum achievable clock rate: 166.7 MHz/6 ns
Testing clock rate: 100MHz/10ns

	Operations		
	Read	Write	Match
Delay	1.70ns	1.75ns	2.60ns
Energy/cycle	0.462nJ	0.109nJ	5.60nJ
Energy- Delay (10^{-18} Js)	0.785	0.191	14.56

I. Logical Architecture

The overall block diagram of the CAM SRAM is shown in fig. 1. It models the functionality of a 256x64 single- ported CAM with eight row address bits.

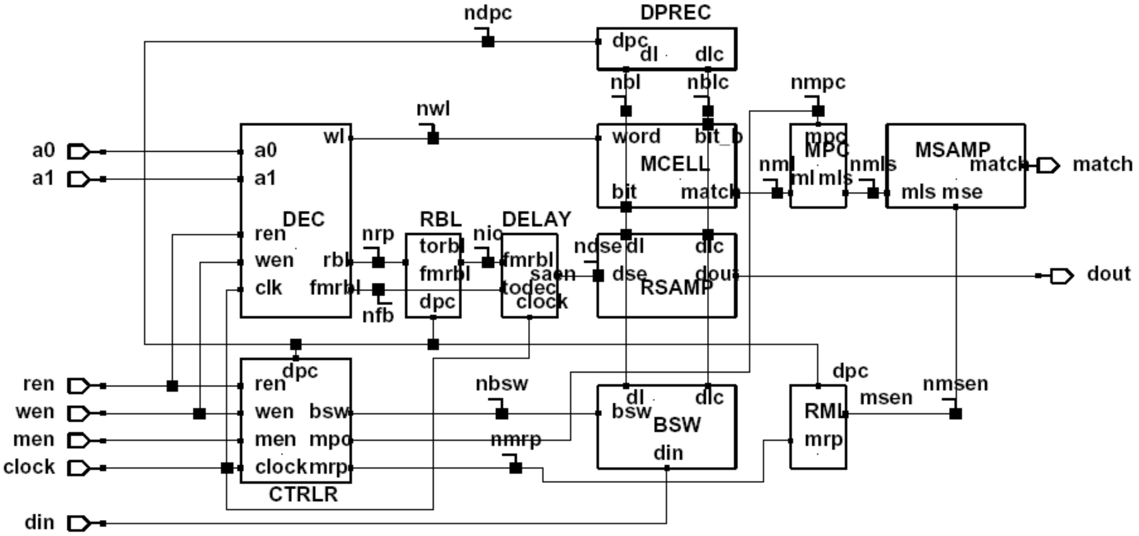

Figure 1. CAM SRAM Logical Functional Block Diagram

Two incoming address bits a0 and a1 are read into the decoder block (DEC). The decoder drives the memory cell block (MCELL) on the wordline. The control bits for the CAM are generated by the controller block (CTRLR). During a read operation, the wordline pulsewidth and data sense amplifier enable is controlled by the replica bitline (RBL) and delay (DELAY) blocks. During a match, the match sense amplifier timing is controlled by the replica match line (RML) blocks. (RSAMP) and (MSAMP) represent the data and match sense amplifiers blocks. (DPREC) and (MPC) represent the bitline and match line precharge circuitry, respectively. (BSW) are the bitline switches.

II. Control Signals

All internal control signals used in the CAM were derived from ren, wen, and men using the logic shown in fig. 2. Control signal outputs are shown in fig. 3. Signals READ_EN, WRITE_EN, and MATCH_EN are asserted for one full clock cycle each. During all three operations, bit lines are precharged by signal DPREC during the first half of the clock cycle. During a match operation, the match line precharge is enabled by MPREC during first half of clock cycle. Read sense (DSEN) and match sense enable (MSEN) are asserted during the second half of the read and match cycles, respectively, and are delayed to ensure proper differential input signal amplification. BSW controls the writing of data to the bitlines and is enabled during the second half of the clock cycle of a match and write operation. The READ_EN signal enables the replica feedback in the decoder to control the wordline pulsewidth during a read operation.

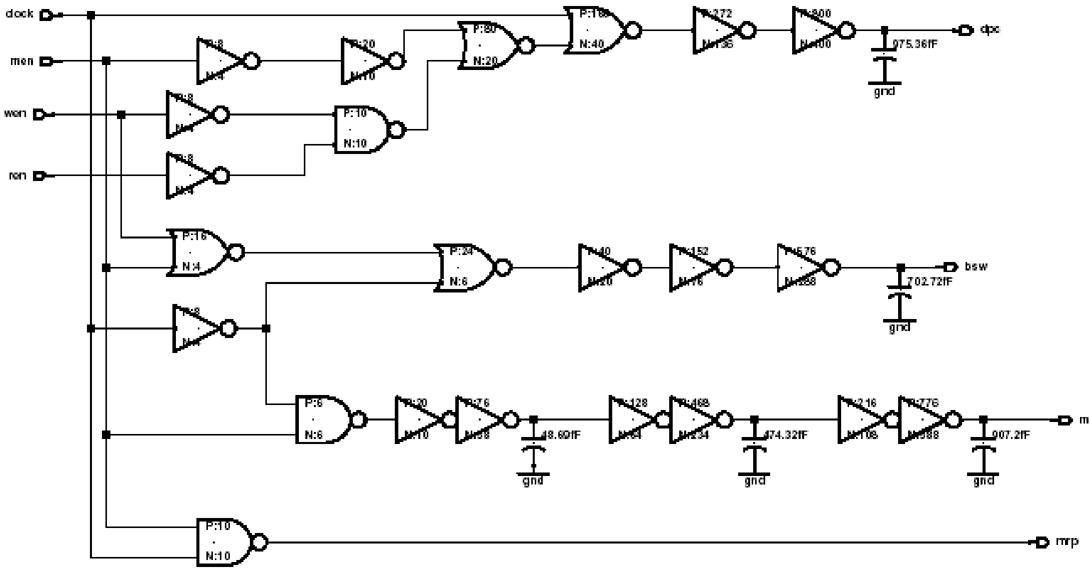

Figure 2. Control Logic

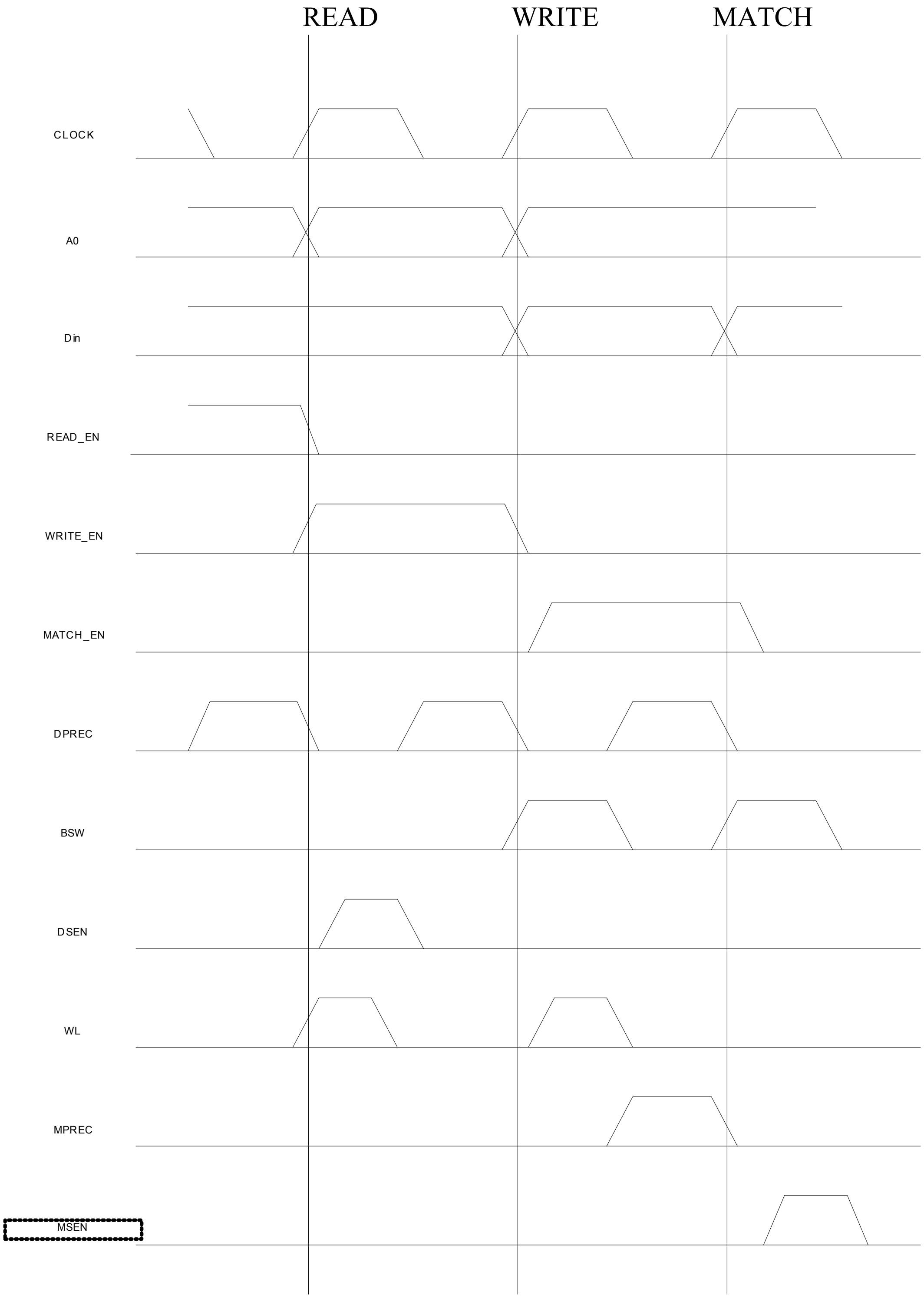

Figure 3. Control Signal Outputs

III. Decoder

The decoder topology used in this project is shown in fig. 3. We used six stages in our decoder to optimize for fanout ~ 4. The decoder path was skewed to favor the rising edge transition of the final decoder stage. The predecode utilizes domino nand's to minimize logical effort for optimum delay.

To limit bitline swings during read access we utilized the power- efficient method of pulsed wordlines, and further minimized power by limiting the bitline pulsewidth just wide enough to guarantee correct read operation. To set the bitline pulsewidth, we used the replica bitline method shown in fig. 3 to obtain good delay matching across various process corners.

The replica structure is based upon the cell- current ratioing technique as shown in fig. 4 [2]. Ten current sources represented by block DCELL pull down the replica bitline. Therefore, the replica bitline slew rate is 10 times faster than the main bitline. By generating local reset timing for the wordline in the final decoder stage, we are able to control the desired bitline voltage swing to ~VDD/10 during a read operation.

Further, by matching the delay of F1, S2, S3 to the wire delay bs, the sense amp is fired only after the bitline has been discharged by the desired amount.

*The replica bitline feedback is disabled during match and write operation.

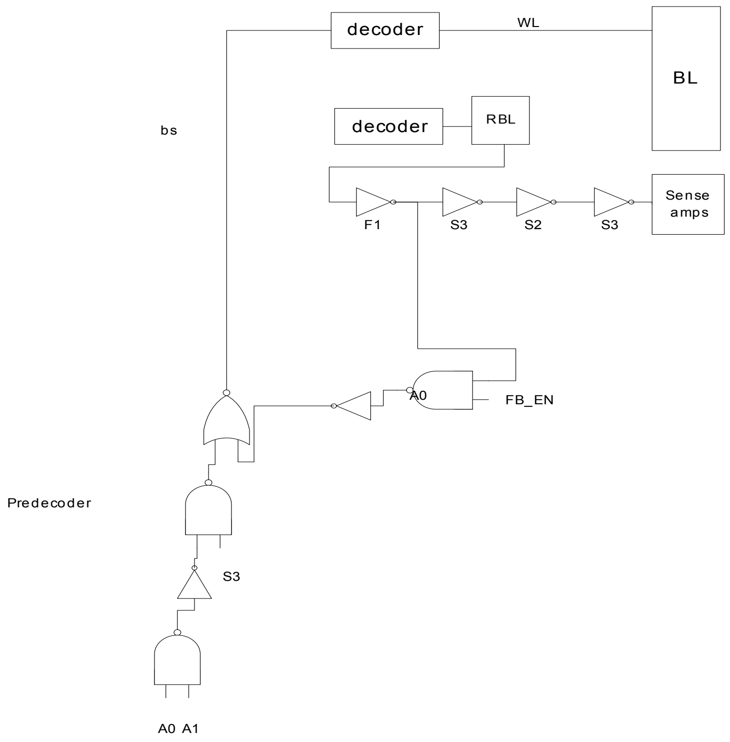

Figure 3. Decoder and Control for Wordline Pulse Width and Sense Clock Activation

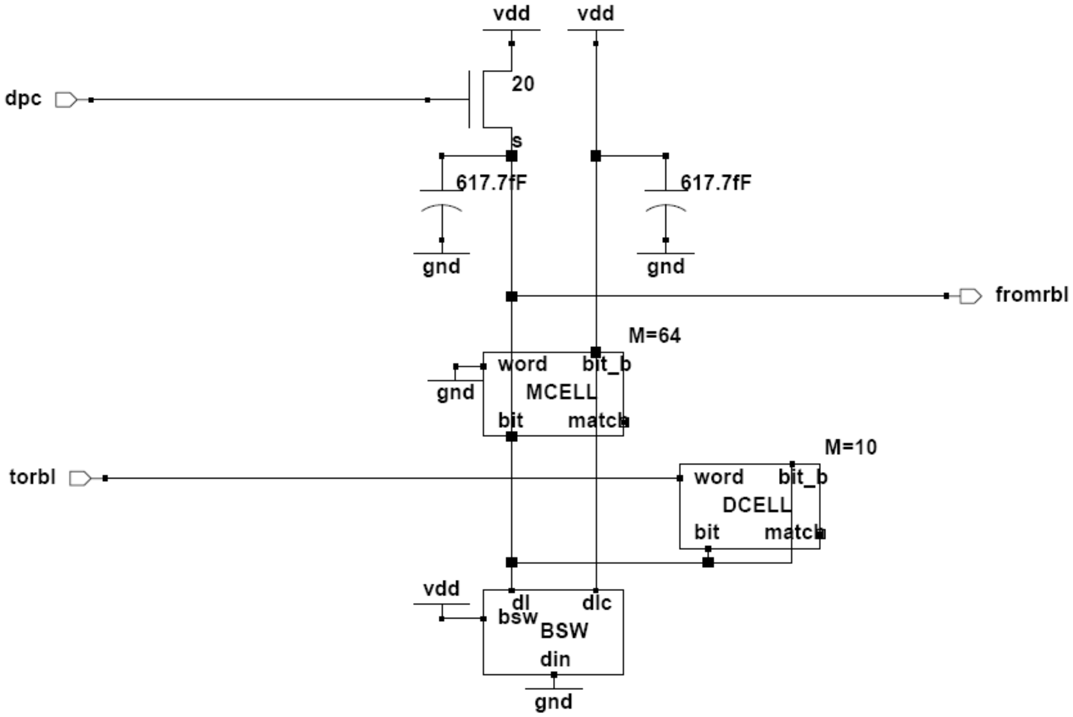

Figure 4. Replica Bitline Structure based on Current Cell Ratio

IV. Memory Cell Structure

The CAM used in our project is shown in fig. 5. [1] It contains the six transistor SRAM cell to store the data, two nmos comparator transistors, as well as a pmos bit match device. Fig. 6 shows the CAM word circuit topology. The word match line is precharged to vdd and is discharged to Vdd- |Vtp| in the case of a word mismatch. The firing of the match sense amplifier was designed to accommodate the worse case delay of a one bit match and is controlled via a replica bitline structure shown in fig. 7. The replica bitline structure was based on the capacitance ratioing technique. The number of cells on the replica bitline is cut to 256/4 ~ 60 and the number of cells on the wordline is cut to 64/4 = 16 in order to fire the sense amplifier after the bitline has been discharged by ~VDD/4. By using a pmos device for pulldown instead of an nmos device, the match line discharge level is elevated from ground to the threshold voltage of the pmos, reducing voltage swing and thus decreasing power consumption.

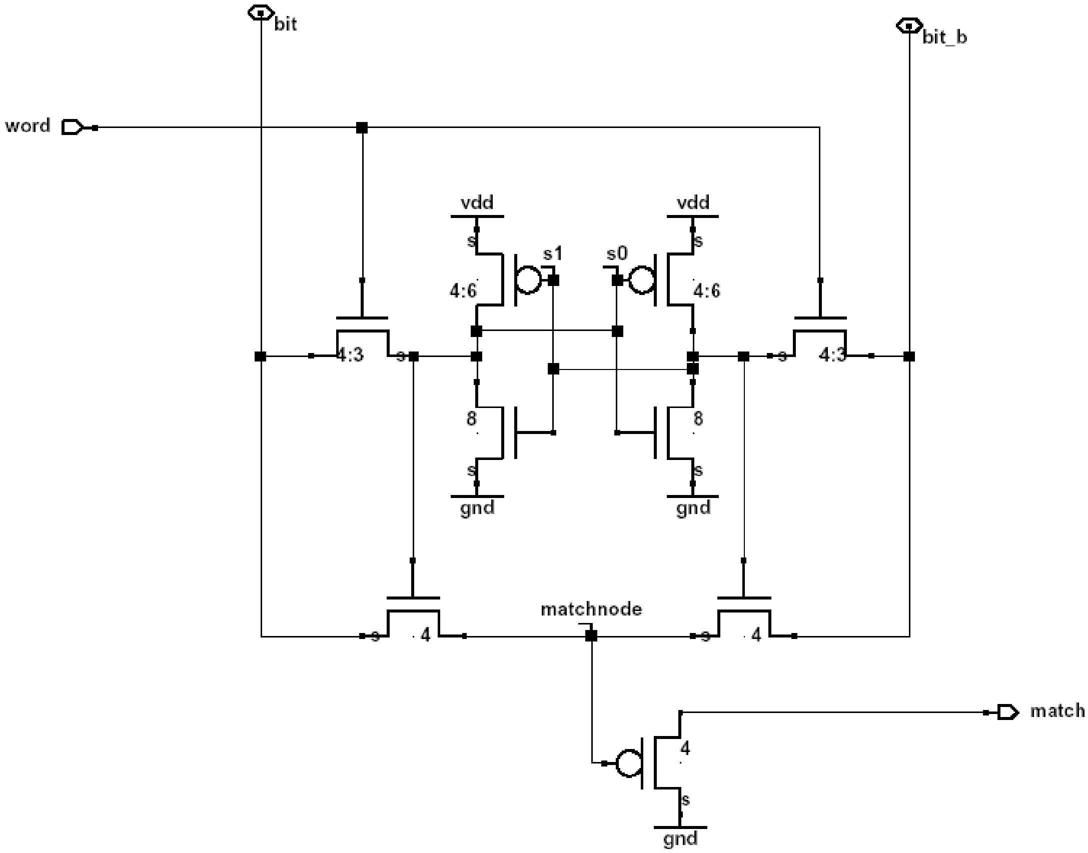

Figure 5. CAM Cell Structure

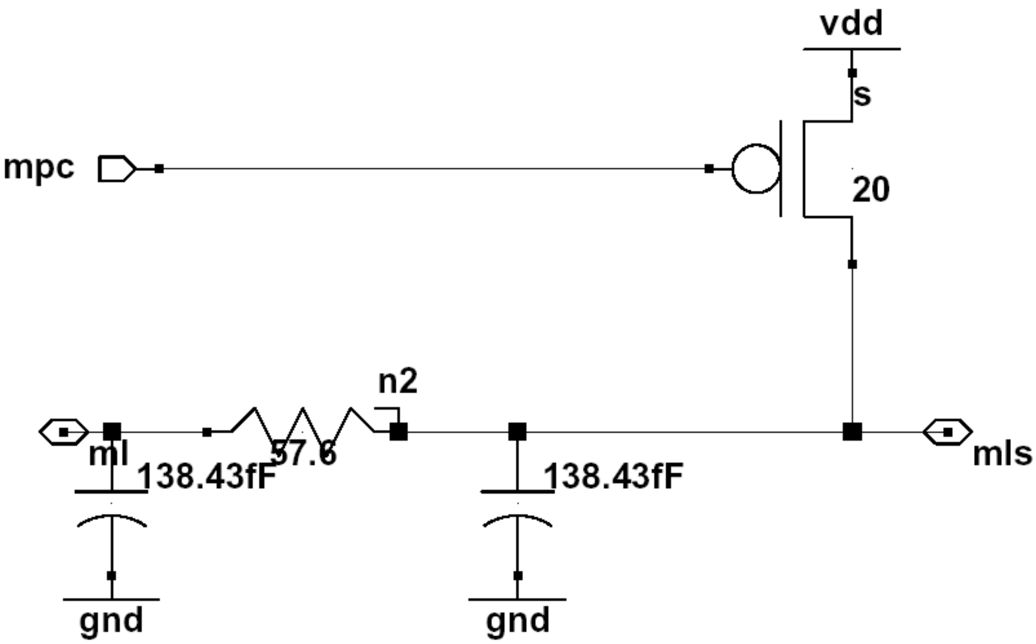

Figure 6. CAM Match Line Precharge Circuit

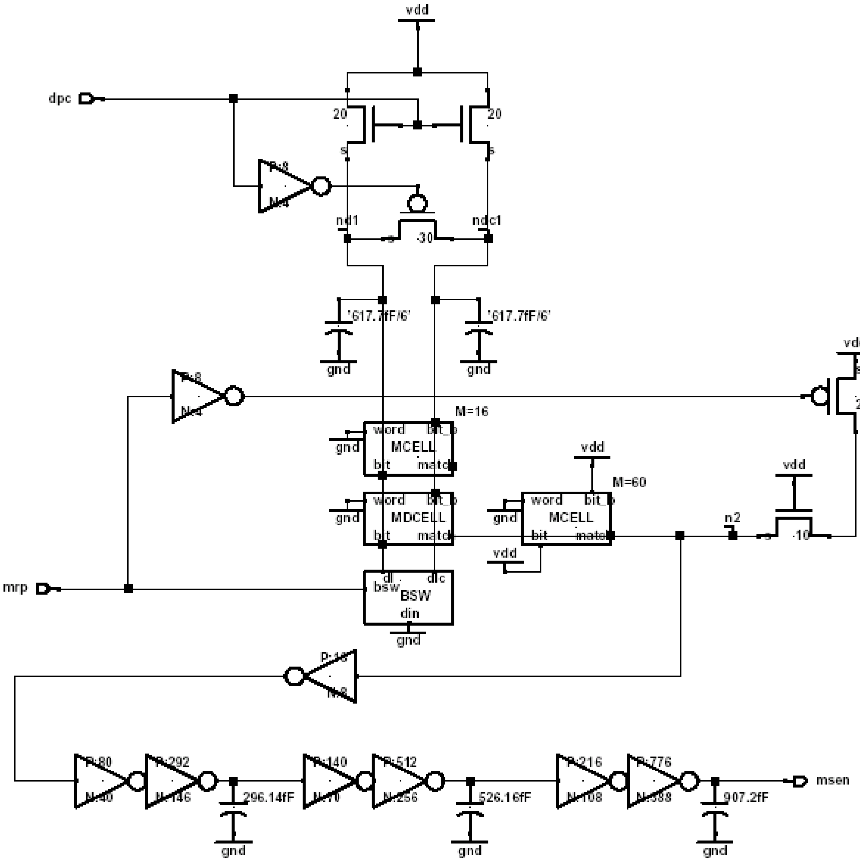

Figure 7. Replica Bitline Structure for Match Sense Enable

V. Sense Amplifiers

The data and match sense amplifier topologies are shown in fig. 8 a and b, respectively. The structures have similar configuration, except that the data sense amplifier is differential with symmetric device sizes where the match sense amplifier is asymmetric with one of the reference nodes tied to vdd. The latter also contains an equalizer between its internal match and matchb nodes to stabilize the sense threshold voltage. Both amplifiers use the cross- coupled feedback mechanism to amplify and latch the sensed data. The amplifier topology is characterized by high speed and highly sensitive amplification and provides rail to rail output swing. This topology minimizes power since there exists no direct dc current path from vdd to ground except during the short switching period. The data sense amplifier we used in fig. 8a is designed to be sensitive enough to detect the worst- case scenario of the heaviest case differential signal where one cell on one of the differential bitlines needs to discharge all other bitline pairs storing a “1.” The match- line sense amplifier has an asymmetric topology with imbalanced driving implemented via (W/L) ratioing. By ratioing device sizes instead of utilizing identical device sizes with a diode connected gate of the nmos comparator device, we save power by avoiding dc power consumption Optimum ratioing was obtained via circuit simulations to maximize speed and to obtain reasonable sensitivity levels.

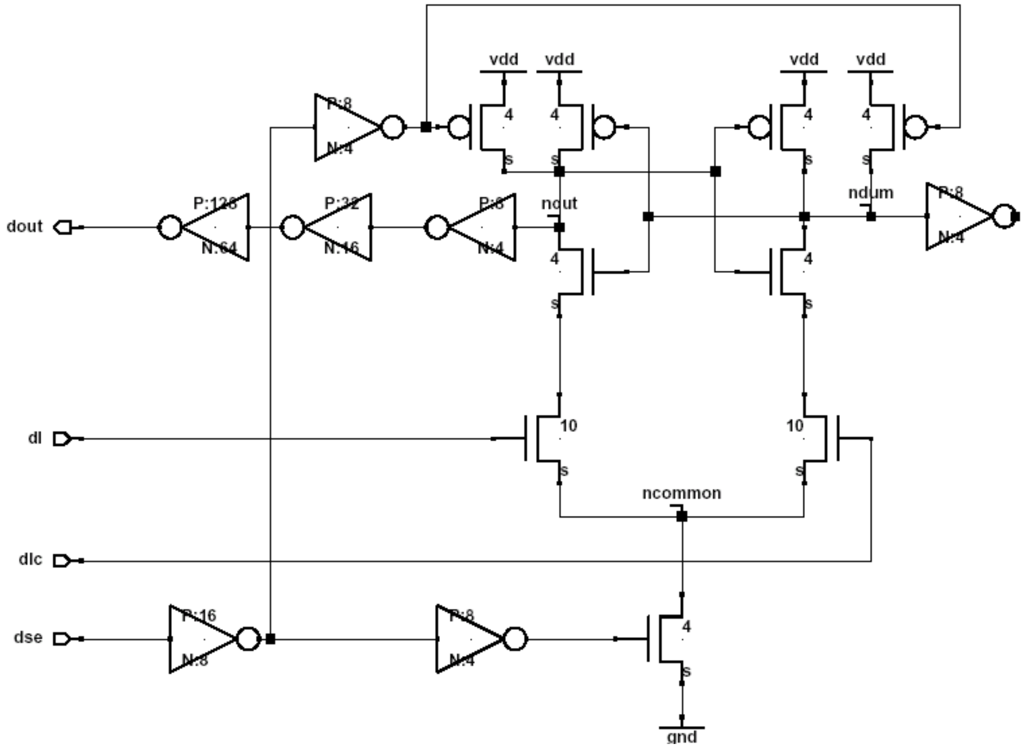

Figure 8a. Data Sense Amplifier

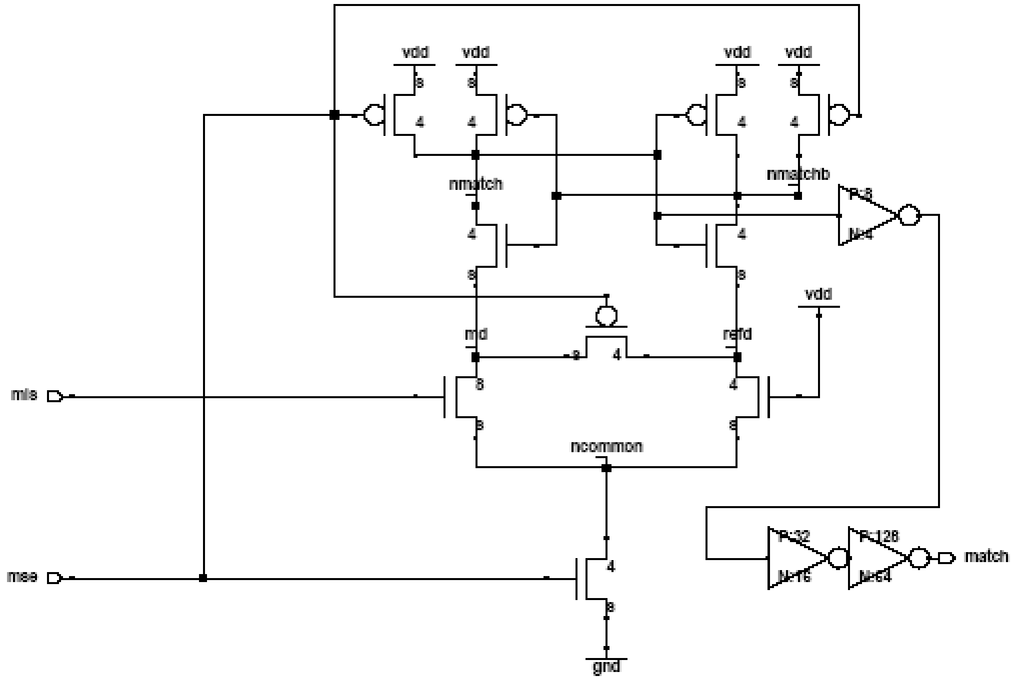

Figure 8b. Match Sense Amplifier

VI. Modeling

To accurately model the capacitances of the CAM SRAM, we accounted for both the wire and the source/gate/drain capacitances of the cells.

Cwire:

Cwl = 0.4fF/um*9um*64 = 230.4fF
Cbl = 0.4fF/um*6um*256=614.4fF

To find the source/gate/drain capacitances of our cells, we used a chain of FO-4 inverters to match the delay of a linear capacitance to that of the gate capacitances of the CAM cells on the wordline, the source/drain capacitances of the CAM cells on the bitline and found the following results:

CAM cell Capacitances:

Cbitline = 1.450 fF/cell (worst-case) where a "1" is stored on cell
Cbitline = 3.148 fF/cell (best-case) where a "0" is stored on cell
Cmatch = 1.667 fF/cell

- ➔ Cbitline_total = Cbl + Cbitlinecells = 1.450fF/cell * 128 + 3.148fF/cell * 128 + 230.4fF = 818.9fF
- ➔ Cwordline_total = Cwl + Cmatch = 614.ffF + 1.667fF/cell * 64 = 721.088fF

*Similar capacitance analysis was utilized during simulation to appropriately load the CAM cell under test.

VII. Measured Results

Fig. 9 shows five complete clock cycles to represent the functionality of the CAM. During the first cycle, a "1" is written to the bitline under test. A read is performed during the second cycle, and during the third cycle, a "0" is written to the bitline. In fourth cycle, we write a "1" to the bitline and perform a match, and in the fifth cycle, we write a "0" to the bitline and perform a match. V(nbl) and v(nblc) represent the bitline and bitline bar voltages, respectively, v(Dout) represents data out voltage, v(nwl) represents wordline voltage, and v(match) represents match out.

Fig. 10 shows the first, second, and third, cycles in greater detail. In the first cycle, we can see that a "1" has been written to the bitline since v(nbl) goes high and v(nblc) goes low while the wordline is enabled. In the second cycle, a "1" is read from the CAM cell since bitline stays high while bitline bar swings low by about 100mV. The voltage swing of bitline bar is controlled by the narrow wordline pulsewidth in the figure. In the third cycle, a "0" written to the bitline since bitline voltage swings low while bitline bar voltage swings high.

Fig. 11 shows the operation of the read sense amplifier. V(ndse) is the data sense enable voltage. V(xreadsa149.ndum) and v(xreadsa149.nout) are the voltages on the cross- coupled latch of the read sense amplifier. During the read, the wordline is enabled, and since we are reading a “1”, bitline stays high while bitline bar swings low by about 100mv. The data sense enable is not asserted until after this bitline voltage swing. Prior to the read, the nodes stored on the data sense amplifier latch is precharged high. During the read, the precharge is disabled, so both nodes ndum and nout stored in the sense amp drop by a small voltage. Since we are reading a “1” on the bitline, the voltage on the dummy node drops faster than the voltage on nout. This difference is amplified by the latch and consequently, ndum drops low while nout pulls back up high, and consequently, the data out node goes high.

Fig. 12 shows the match sense amplifier operation in greater detail. V(nmatch) and v(nmatchb) represent the voltages on the nodes of the cross- coupled inverter in the match sense amplifier. During the match operation, first, a “0” is written to bitline and nmatch and nmatchb are precharged to vdd. In the second cycle of the match operation, the precharge is disable, so nmatch and nmatchb drop by a small voltage. Since a “0” is written on bitline and a “1” is written on bitline bar, we have a match, so wordline only drops by about 100mv. The match sense amplifier is then enabled after allowing time for the develop a small voltage swing in the case of a mismatch, and consequently, match goes high.
*Figures 9 – 12 illustrate CAM cell operation under TT corner

The first plot of Figure 9 is the clock and data input signal; the second plot is Write_Enable, which asserts during the first and third clock cycle, Read_Enable, which asserts during the second clock cycle, and Match_Enable, which asserts during the fourth and fifth clock cycles. In the first cycle, a 1 is written into the cell, and this datum is read out during the second cycle. Then a 0 is written into the cell. Two match operations ensue. One matches and the other mismatches.

Figure 10 shows a writing operation. Besides the bitline and complementary bitline signals, it also shows the flip of memory cell nodes s0 and s1.

Figure 11 shows a reading operation. The pulse width of wordline is fine tuned to result in a approximately 100mV different on bitline and complementary bitline. On the firing of sense enable signal, this difference is amplified to determine the data output.

Figure 12 shows the matching operation.

*Note: In worst case scenario of 1 mismatch as shown in fig. 8, wordline drops by approximately 400mV, therefore leaving a noise margin of ~300mV between match and mismatch.

Fig. 13 shows the same three read, write, and match functionality of the CAM cell under FS conditions, while fig. 14 shows the three operations under SF conditions. The functionality under all three conditions, TT, FS, and SF is maintained.

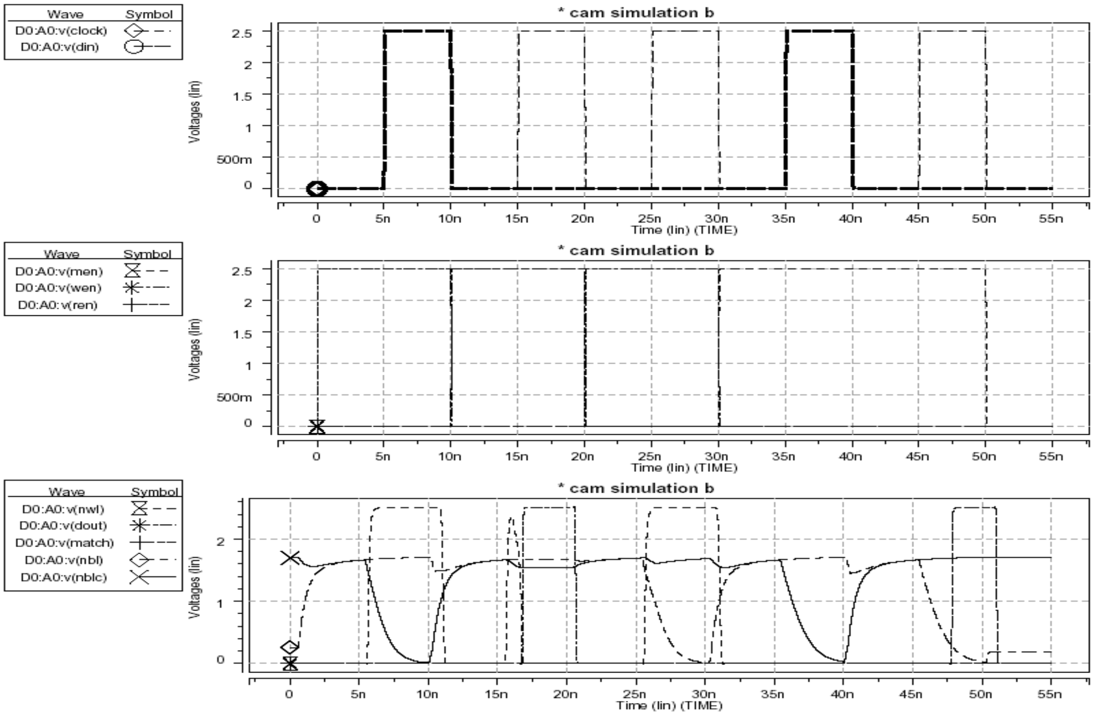

Figure 9. Read, Write, Match Operation Simulation of CAM Cell

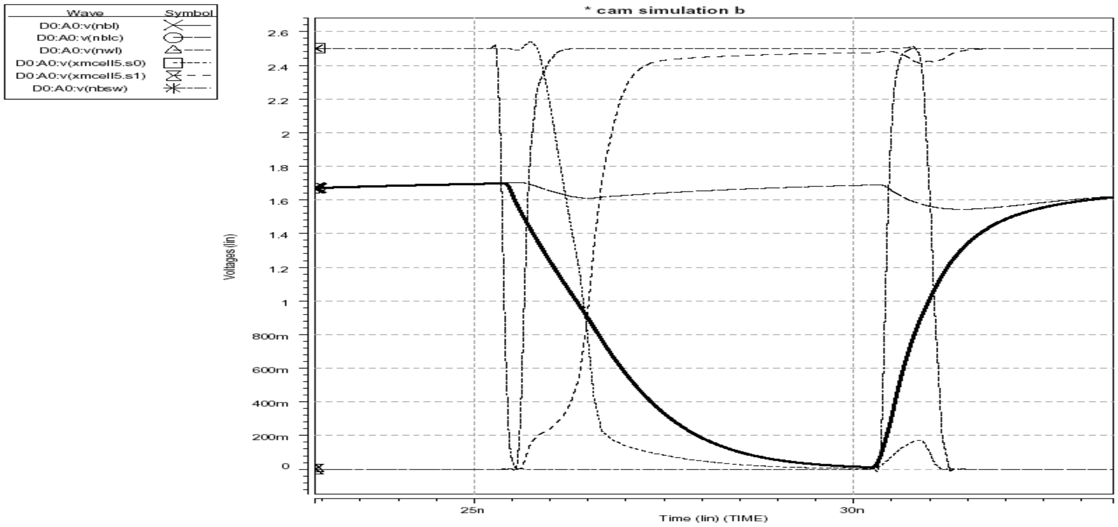

Figure 10. Write Operation of CAM Cell

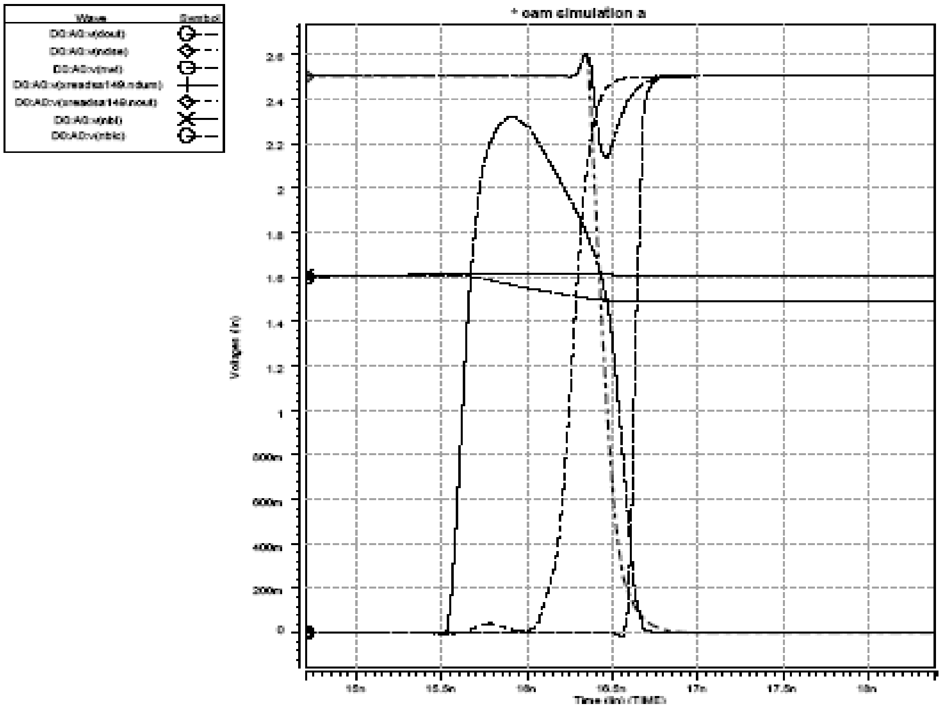

Figure 11. Read Sense Amplifier Operation

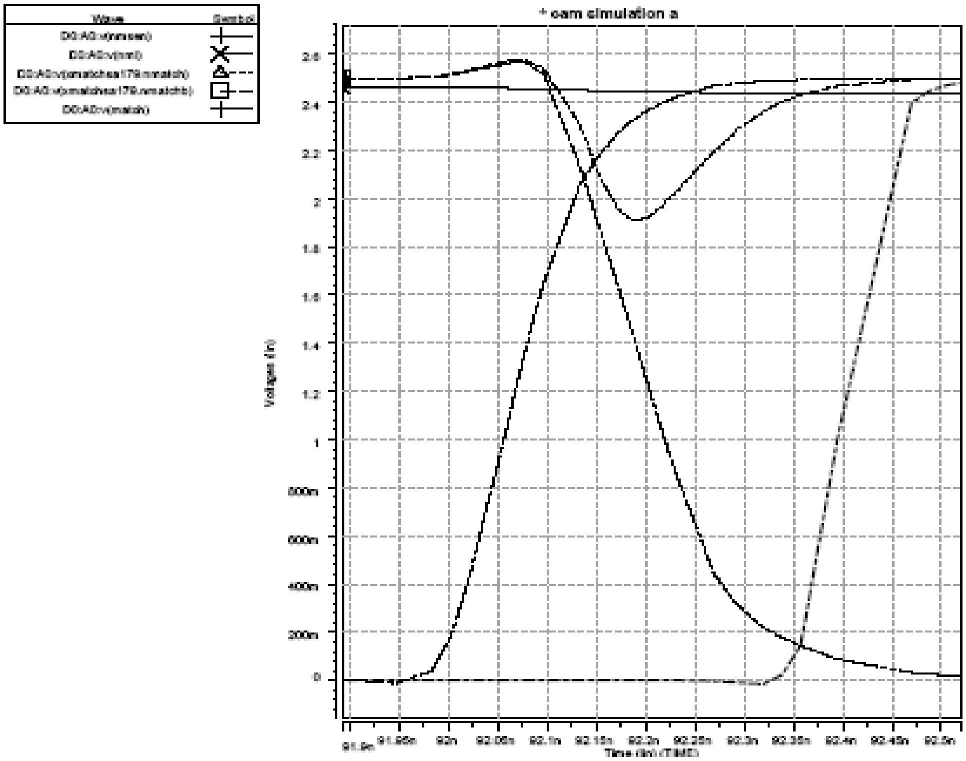

Figure 12. Match Sense Amplifier Operation

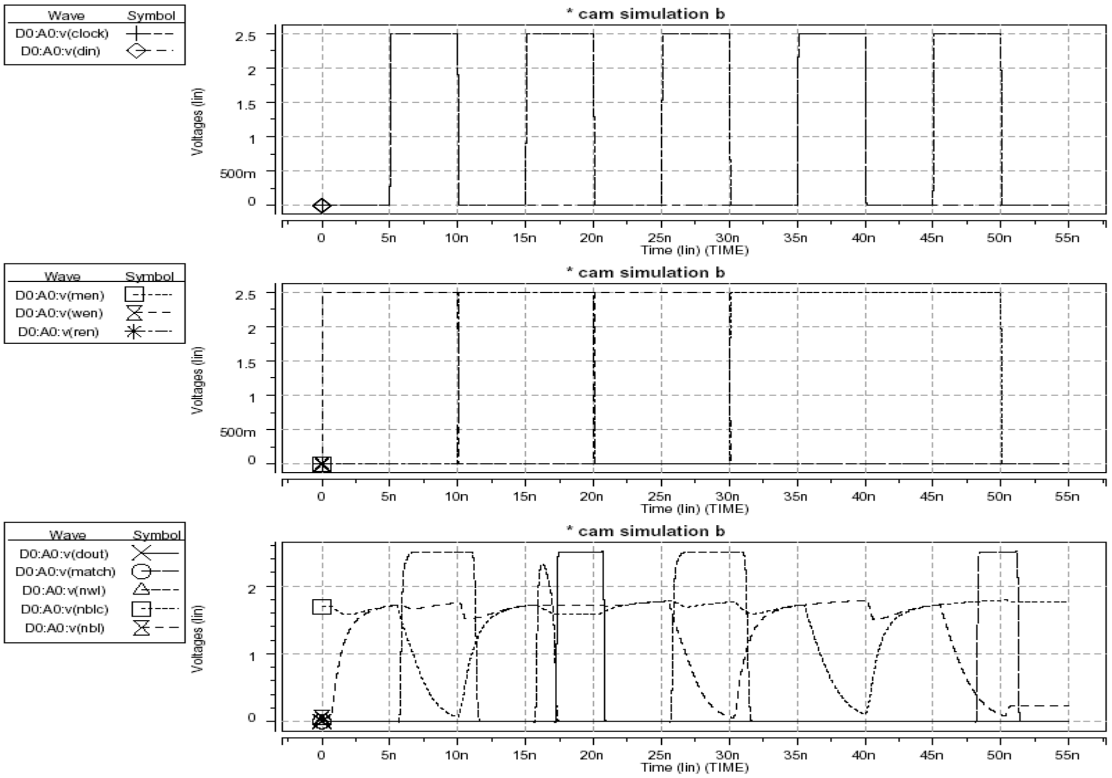

Figure 13. Read, Write Match Operation of CAM Cell under FS Conditions

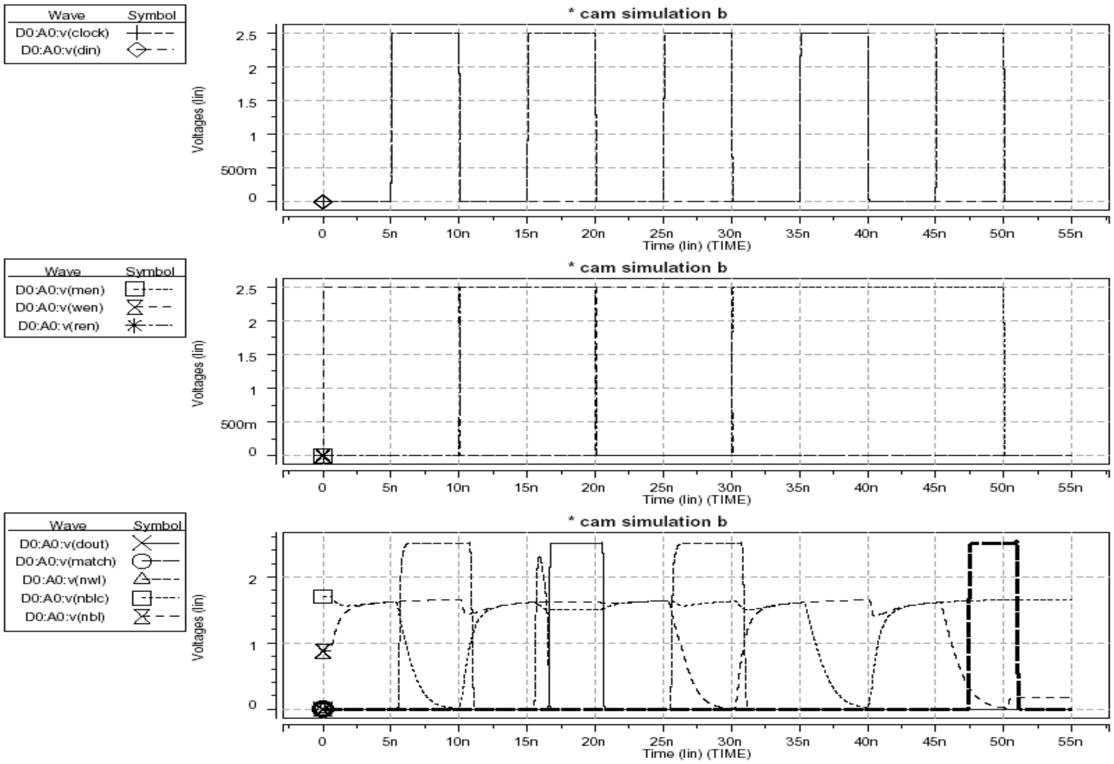

Figure 14. Read, Write, Match Operation of CAM Cell under SF Conditions

Delays

Bitline precharge delay
This includes the delay of generating bitline precharge signal DPC and delay of charging up the bitlines. The second part dominates. Using a pullup NMOS transistor of size 30 and equalizing PMOS transistor of size 40, the total precharge delay is 2.5ns to precharge bitline and bitlineb within 20mV of difference starting from (Vdd-Vt).

Matchline precharge delay
Matchline has a lot less parasitic capacitance than bitline. Using a pullup PMOS transistor of size 30, the precharge delay is 2.7ns to precharge the matchline higher than (Vdd-20mV).

Decoder delay
The delay of decoder starting from asserting the address line to selecting the wordline is 650ps.

Writing delay
The delay of writing starting from asserting input to switching memory cell nodes is 1.52 ns.

Reading delay
The delay of reading starting from asserting decoder input to the time when data output is available is 1.75ns. A replica bitline is used to control the pulsewidth of the wordline and the timing to fire the read sense amplifier. This approach proves to have the advantage of saving power and improving sensing robustness.

Matching delay
The delay of matching starts from asserting the data input to output matching signal. It is measured to be 2.60ns. The relative large value is attributed to a delayed matching sense enable signal that improves the robustness of matching sense amplifier.

Clock cycle
A clocked timing approach is used. With a clock of 50% duty cycle, the clock cycle can be set at 6ns (166.7 MHz).

Energy

Writing operation

The energy consumption during a writing operation includes the energy consumed in control circuitry, decoder and bitline precharge/discharge. Bitline activity accounts for by far the largest portion of it. This is alleviated by using NMOS transistors to precharge bitline and pass input data. As a result, the bitline swing is reduced to (Vdd-Vt). The measured energy during one writing cycle is 0.462nJ.

Reading operation

The energy consumption during a reading operation contains the energy consumed in control circuitry, decoder, bitline precharge/discharge, sense amplifier, and replica circuit. As the wordline pulse width is reduced by careful design, the energy spent on bitline switch is significantly less than that in a writing operation. The measured energy during one reading cycle is 0.109nJ.

Matching operation

Due to its NOR type operation, almost all matchlines will be discharged during a matching operation. This is very power consuming. The energy measured during one matching cycle is 5.60nJ.

VIII. References

[1] Miyatake, H., et. Al, "A Design for High- Speed Low- Power CMOS Fully Parallel Content- Addressable Memory Macros," JSSC, Vol. 36 No. 6, June 2001.
[2] Amruter, B. et Al, "A Replica Technique for Wordline and Sense Control in Low-Power SRAM's, JSSC, Vol 33. No. 8, August 1998.