EE215C: A RF Front End for 5GHz Wireless LAN

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***Abstract*—The front-end of a zero-IF receiver for 5GHz Wireless LAN (IEEE802.11a) applications consists of a low-noise amplifier (LNA), two mixers and a local oscillator with outputs in quadrature phases. The application band spans 5.15 to 5.35 GHz and the channels is 20MHz wide. In this project, our goal is to design a LNA, a single mixer and a single-phase oscillator using TSMC 0.18μm CMOS process with $1.8V$ supply voltage.**

I. LOW-NOISE AMPLIFIER

The main LNA circuit is shown in Fig. 1. It is a cascoded common source amplifier with inductance degeneration. Taking into account lossy resistances R_g and R_s, the input impedance of the circuit is given by:

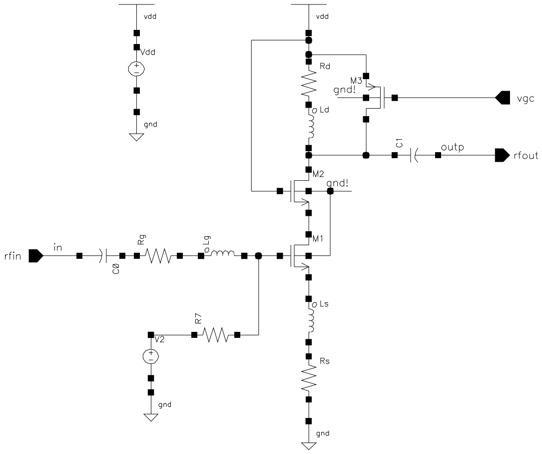

Fig. 1. Low noise amplifier schematics.

$$Z_{\text{in}} = \left(R_g + R_s + \frac{g_m L_s}{C_{gs}}\right) + j\left[\omega(L_g + L_s) - \frac{1 + g_m R_s}{\omega C_{gs}}\right]$$

When $Z_{\text{in}} = R_{\text{in}} = 50\Omega$ and L_d resonates with C_L, the gain and noise figure of the amplifier are:

$$A_v = \frac{\omega_T L_d Q}{R_{\text{in}} + \omega_T L_s}, \quad NF = 1 + \frac{\gamma g_m R_{\text{in}}}{(\omega_T/\omega)^2}$$

where $\omega_T = g_m/C_{gs}$.

L_d is designed to resonate with the total capacitance at the output for maximum amplification. To achieve a high A_v and low NF, it is desirable to have a large ω_T. Hence, the channel length of M1 is set to be the minimum (0.18μm). The width and bias of M1 is chosen to satisfy gain and noise figure requirement while consuming a small amount of power. Linearity also plays a role in determining these parameters since $V_{IIP3} = \sqrt{8V_{\text{eff}}/3\theta}$ demands a high V_{eff}. The values of L_s and L_g are subsequently adjusted based on impedance matching.

The amplifier gain is controlled by the voltage vgc at the gate of PMOS M3. When $vgc = V_{dd}$, M3 is off and the LNA has the highest gain. When $V_{g3} = 0$, M3 is in deep triode and lowers the gain to about 5dB.

Device parameters determined from above considerations are listed in Table.

The s_{11}, A_v, and NF are plotted in Fig.s 2,3, and 4.

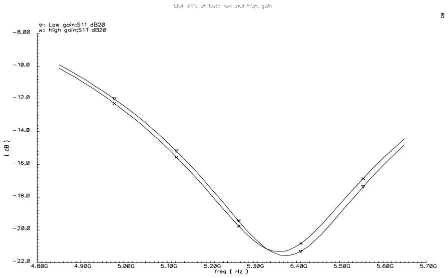

Fig. 2. The s11 of LNA at high and low gain.

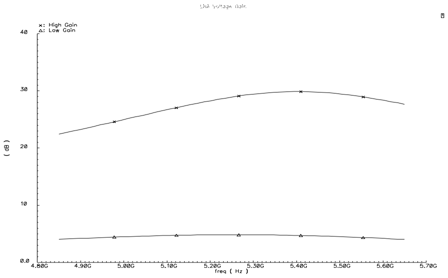

Fig. 3. LNA gain plot.

II. MIXER

We use the double balanced (Gilbert cell) mixer, which is shown in Fig 5. The mixers are resistively loaded with $R_d = 500\Omega$. When $V_{LO} >> V_{\text{eff}}$ of LO FETs, the conversion gain of the mixer is:

$$\frac{V_{\text{out}}}{V_{RF}} = \frac{2}{\pi} g_m R_d$$

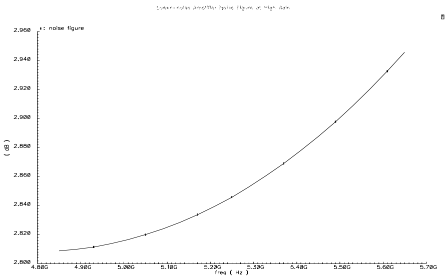

Fig. 4. Noise figure of LNA.

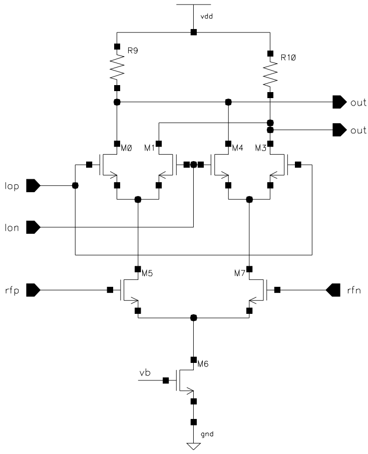

Fig. 5. Double balanced mixer schematics.

The FETs in the commuting differential pair contribute noise as they pass the balance point, which can be alleviated by sharp LO transitions. The transition time is proportional to the gate overdrive and inversely proportional to LO amplitude. The former is lowered using a large W/L ratio, and the LO amplitude is set to 700mV. Further increasing LO amplitude will drive the devices into deep triode and worsen the overall performance. The FETs connecting RF inputs use slightly longer channels to improve the linearity. Their size and bias are properly set to achieve the required conversion gain of 5dB.

Device parameters are listed in Table. The mixer differential output when $f_{LO} = 5$GHz, and $f_{RF} = 5.25$MHz is shown in Fig. 6. The mixer conversion gain when $f_{LO} = 5$GHz and $f_{RF} = 5.25$GHz is plotted in Fig. 7. The gain at 250MHz is 8.167dB.

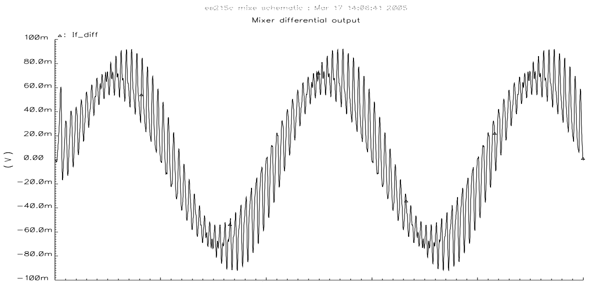

Fig. 6. Mixer differential output.

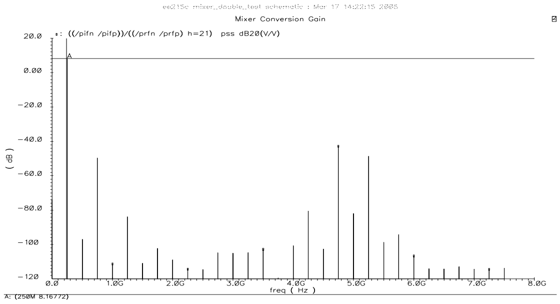

Fig. 7. Mixer differential output.

III. OSCILLATOR

The oscillator is realized using a differential LC configuration as depicted in Fig 8. The different pair provides the negative impedance to compensate the inductor loss. To sustain the oscillation, it is required that $g_m R > 2$. The oscillation frequency is set by the LC tank, which filters out higher harmonics.

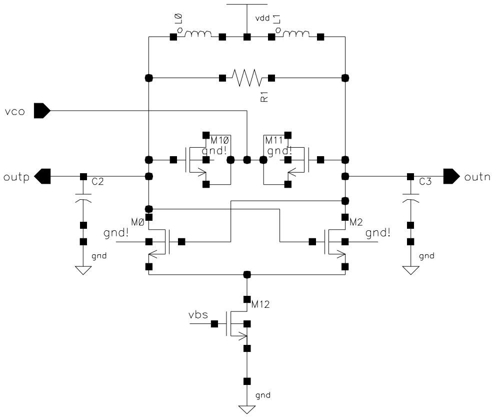

Fig. 8. Tunable differential LC oscillator.

$$\omega_0 = 1/\sqrt{LC}$$

To allow for PVT variations, ω_0 must be tunable across twice the application bandwidth. Using MOS varactor to vary the frequency, we have the following relation:

$$\Delta\omega = -\left(\frac{\Delta C}{2C}\right)\omega_0$$

Therefore, $\Delta C \approx 0.16C$ is required to achieve a tuning range of 400MHz.

The amplitude of oscillation is determined by the bias current and lossy resistor $A = 2IR/\pi$. The phase noise of the oscillator at offset frequency ω_m can be estimated by the following equation.

$$PN(\omega_m) = \frac{kTR}{A^2}\left[1 + \gamma\left(1 + \frac{\pi A}{4V_{\text{eff}}}\right)\right]\left(\frac{\omega_0}{Q\omega_m}\right)^2$$

First of all, the oscillation amplitude must be maximized to achieve a small phase noise. Nearly $2V_{dd}$ swing is achieved by appropriately setting the bias current and inductor value. Second, V_{eff} at the tail source should be increased. This can be done by decreasing W/L ratio of the FET.

The device parameters are given in Table. The oscillator outputs and the phase noise at $f_{LO} = 5.238$GHz are plotted in Fig. 9.

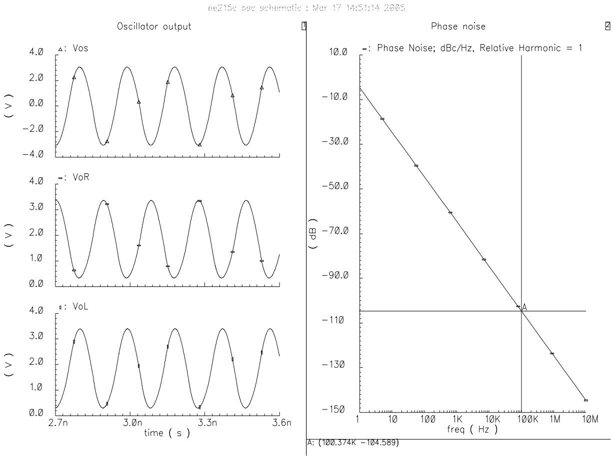

Fig. 9. Tunable differential LC oscillator.

IV. OVERALL SYSTEM

The cascaded system diagram is shown in Fig. 10. The waveforms at different points of the cascaded system is plotted in Fig. 11

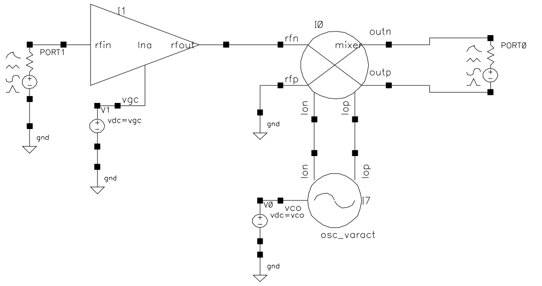

Fig. 10. Overall sytem.

During tuning of the front end system, we realized that if the oscillator is directly connected to the mixer, significant distortion was introduced to the oscillator, which causes degradation of the system. This is partially due to the gate capacitance at the mixer. In order to maintain high quality and large driving strength of the oscillator, we used two buffers at the output of oscillator. The buffer has the same structure as the oscillator except the feedback part. The total current consumption of the overall system is 19.83mA. We were not able to get the IIP3 of the overall system. Whenever we simulated it using PSS, the program reported internal error. The IIP3 of the LNA at low gain side and the mixer is plotted in Fig. 12. We observed that the IIP3 is heavily dependent on the extrapolation point, which needs experience to be determined. It is not clear to us whether the plot shown in Fig. 12 is completely right, which might suggest our circuit needs more tuning to get more than zero dB IIP3.

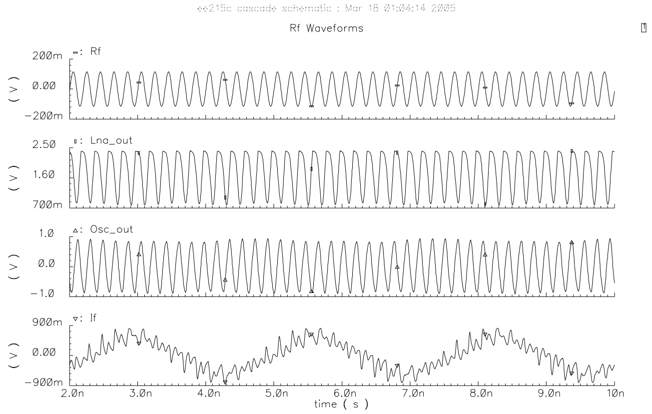

Fig. 11. Waveform outputs of the overall system.

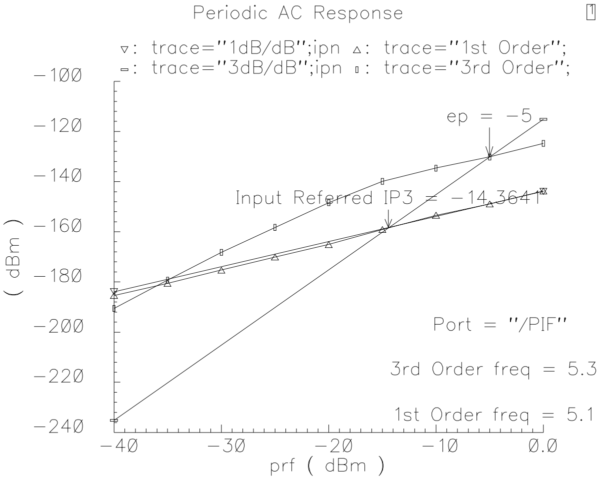

Fig. 12. IIP3 of LNA and Mixer.

V. CONCLUSION

In this project, a front end of a wireless LAN RF receiver is designed and simulated using Spectre-RF. We gain the hands-on experience of RF circuit design. Although we are still confused about different ways to compute the noise figure, the IIP3 and all the P-methods in Cadence, one thing is for sure. RF circuit is more of arts than engineering. It demands knowledge, patience and diligence.