

C. SHA

Although the 1.5-bit-per-stage pipelined topology greatly relaxes the offset requirements of the op-amp and comparator, the gain error of the SHA is still of great concern. We analyze the origin of SHA's gain error and its effect on ADC's linearity. The SHA in sampling and amplification modes are shown in Fig. 3. Neglecting capacitor and charge injection

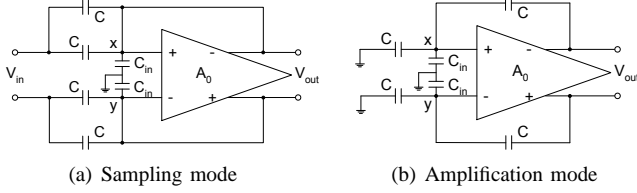


Fig. 3. Sample and hold amplifier.

mismatches, the gain error is caused mainly by the input capacitor C_{in} and the finite gain A_0 of the op-amp. Neglecting the offset of op-amp, during sampling mode $v_x = v_y = 0$. The charge resides on the top plates of capacitors C is

$$Q_x = Q_y = \frac{v_{in}}{2} \times 2C = v_{in}C$$

During amplification, the input switches to zero. We have

$$Q_x = \left(\frac{v_{out}}{2} - \frac{v_{xy}}{2} \right) C - \frac{v_{xy}}{2} (C_{in} + C)$$

due to charge conservation, and

$$-v_{xy}A_0 = v_{out}$$

from op-amp. Therefore, the gain of the SHA is

$$G = \frac{v_{out}}{v_{in}} = 2 - \frac{2(2C + C_{in})}{(A_0 + 2)C + C_{in}} = 2 + \alpha \quad (4)$$

where the gain error

$$\alpha \approx \begin{cases} -6/A_0 & \text{when } C_{in} \approx C \\ -4/A_0 & \text{when } C_{in} \ll C \end{cases}$$

The effect of this gain error on the residue is illustrated in Fig. 4. The INL reaches its maximum at the last reference

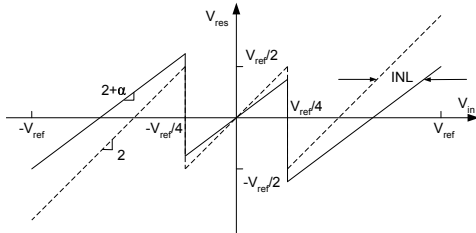


Fig. 4. Dashed line is the ideal residue, and solid line is due to gain error.

voltage $v_r = V_{ref} - 1LSB$. To determine the INL at v_r , we find the actual v_{in} that causes the comparator to trip zero.

$$(2 + \alpha)^n v_{in} - (2 + \alpha)^{n-1} V_{ref} - \dots - (2 + \alpha)^0 V_{ref} = 0$$

which gives rise to

$$v_{in} = \frac{V_{ref}}{1 + \alpha} - \frac{V_{ref}}{(1 + \alpha)(2 + \alpha)^n}$$

Thus

$$INL_{max} = v_r - v_{in} \approx \alpha V_{ref} < 1LSB$$

For a 7-stage ADC, this demands $\alpha < 0.8\%$. From Eq. (4), this can be achieved by using an op-amp with $A_0 \approx 1000$. The effect of gain error on DNL is generally less severe.

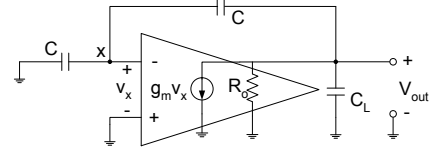


Fig. 5. SHA settling.

Besides accuracy, the speed of SHA is also tied to the op-amp. The time constant of the SHA during hold mode, shown in Fig. 5, can be shown to be

$$\tau_{hold} = \frac{R_o(2C_L + C)}{1 + g_m R_o} \approx \frac{2}{G_{DC} f_{3dB}}$$

The approximation is true when $C_L \gg C$. The requirement of a high-gain and fast op-amp poses one of the most challenging tasks in pipelined ADC design.

In our design, since inputs and outputs of SHA are connected to their respective common mode levels instead of configured as a unity gain sampler during sampling mode, the SHA offset remains uncanceled. However, this error can be pushed all the way to the input of the first stage by inserting opposite offsets to comparators [2]. The net effect becomes a input-referred offset that does not affect ADC linearity after the comparator offset is eliminated by digital correction.

D. Op-amp

Given the medium gain and high speed requirement, we use a single stage telescopic topology for the op-amp design. The difficulty in shorting the inputs and outputs to form a unity gain buffer is avoid by connecting inputs and outputs to separate common mode voltages during sampling. The main part of the op-amp is shown in Fig. 6. To boost the gain, the channel length of transistors M2~M7 are set to be larger than the minimum channel length 0.18 μm .

The bias circuitry is depicted in Fig. 7. Outputs vg2, vg4, vg6, and vb connect to the corresponding wires in Fig. 6. All transistors in the bias circuitry operate in saturation except for M1, which is in triode. The V_{ds} of M1 defines that of M2,3 in the cascode.

The common mode feedback network, which is shown in Fig. 8, uses a capacitor sensing scheme discussed in [3]. When the SHA is in sampling mode, vout1 and vout2 are connected to the common mode level. Meanwhile, ck asserts high, and the voltages across C0 and C1 are refreshed.

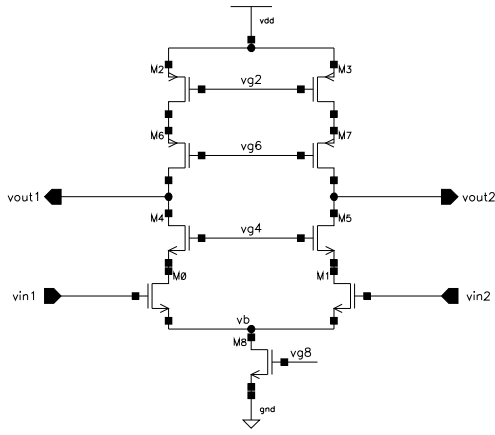


Fig. 6. Telescopic op-amp.

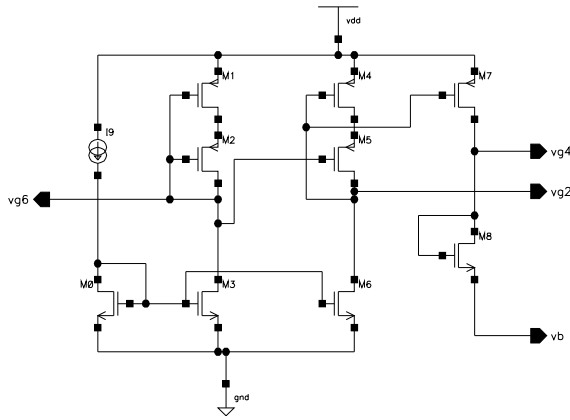


Fig. 7. Bias circuitry of the telescopic op-amp.

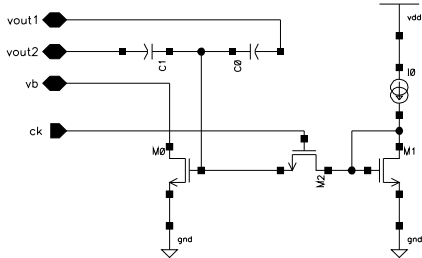


Fig. 8. The common mode feedback network.

E. Comparator

The comparator design is shown in Fig. 9. It compares the differential voltages $\Delta v_{in} = v_{in} - v_{inb}$ with $\Delta v_{ref} = v_{ref} - v_{refb}$, and outputs $\Delta v_{out} = v_{out} - v_{outb}$. The speed of the comparator is limited by preamplifier overdrive recovery and latch regeneration.

The outputs of comparators at each stage is used to drive a simple logic whose output switches the input of SHA to $\pm V_{ref}$ or common ground. The detailed view of this switch is shown in Fig. 10. The control signals X , Y , and Z are functions of comparators' outputs (A , B), and clock signal.

$$X = \bar{B}\phi_2, \quad Y = A\phi_2, \quad Z = \bar{A}B\phi_2 \quad (5)$$

These functions are implemented as simple digital gates.

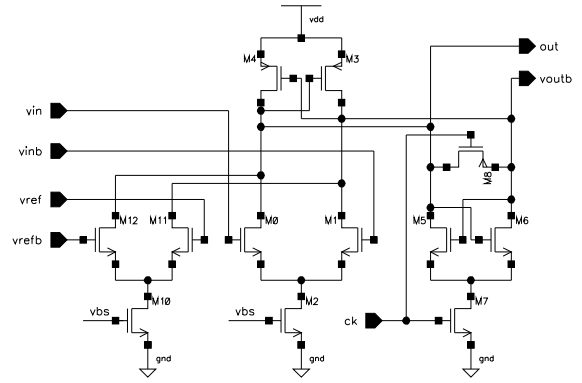


Fig. 9. The CMOS differential comparator.

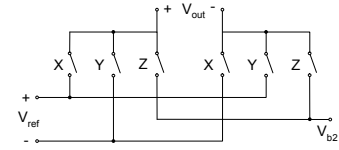


Fig. 10. The switch s in Fig. 2.

F. Timing diagram

The clock sequences ϕ_1 , ϕ'_1 , and ϕ_2 at i th stage are shown in Fig. 11. The sampling instance is defined by ϕ'_1 which

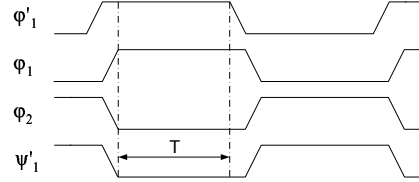


Fig. 11. The timing diagram.

falls ΔT seconds before ϕ_1 to avoid input dependent charge injection. ψ'_1 is the counterpart of ϕ'_1 at $(i-1)$ st stage. ψ'_1 is also ΔT seconds behind ϕ'_1 to avoid disturbing the input at i th stage before it is sampled. The slightly displaced clock edges are generated using cascaded inverters. The following table summaries the activities of SHAs and comparators at stages $(i-1)$ and i during different clock period.

	ϕ_1 high (ψ_1 low)	ϕ_1 low (ψ_1 high)
SHA _{i}	Sample	Hold
Op-amp _{i}	CMFB	Amplify
Comp _{i}	Amplify	Latch
SHA _{$i-1$}	Hold	Sample
Comp _{$i-1$}	Latch	Amplify

The sequence of events that takes place during T (between the falling edges of ψ'_1 and ϕ'_1 in Fig. 11) are: Comp _{$i-1$}

regenerates; Outputs of Comp_{i-1} propagate through digital logic; SHA_{i-1} settles; Comp_i finishes pre-amplification. This is the critical signal path of the pipelined ADC. The minimum clock period is hence given by:

$$T_{ck} = 2(T + \Delta T + T_{tran}) \quad (6)$$

where T_{tran} is the clock transition time.

III. SIMULATION RESULTS

A. Op-amp

We summarize some parameters of our op-amp in the following table when it operates as a stand-alone system.

Parameters	Values
DC gain (G_{DC})	1172
C_{in}	99.4 fF
3dB bandwidth	1.47 MHz
Phase margin	50.9°
I_{ss}	788.8 μA
P_D	1.55 mW
Output swing	0.8 Vp-p
Input offset	4.5 mV

When driving capacitive load, f_{3dB} will drop and PM will improve. Besides boosting g_m , a large I_{ss} helps reduce the slewing time. P_D includes the power consumption in bias and CMFB circuitry. The overall system employs one op-amp in each of first six stages. Hence, the total power consumed by op-amps is 9.3 mW, which is approximately one half of the power budget. The effective voltages of transistors in cascode are set to be less than 0.2 V, which gives approximately a 0.8 V p-p output swing. As discussed previously, the input offset is tolerable as long as it does not exceed the capacity of digital correction.

B. SHA

Complementary switches are used. $C = 0.4$ pF for sampling capacitors. In the first simulation, a constant input of 100 mV is used. A 0.9 pF capacitor, which approximates the next stage SHA, loads each of SHA differential outputs. The result is shown in Fig. 12. The gain error α is less than 0.8%. It takes the SHA about 5.5 ns to settle to 199.2 mV, which is within 0.1% (0.25 LSB) of its final value (199.34 mV). Although op-amp provide a output swing up to 0.8 Vp-p, gain error prevents V_{ref} to be as high. To find out the maximum V_{ref} can be used. The input is progressively increased while monitoring the gain error. It is found that α remains less than 0.8% when $V_{out} \leq 640$ mV, which is shown in Fig. 13. Therefore, we choose $V_{ref} = 640$ mV. This leads to $1LSB = 5$ mV. A large value of LSB is desirable in that the system is less susceptible to distortion and noise. Even higher V_{ref} can be achieved by boosting op-amp gain or choosing a different topology. However, both will likely lead to sacrifice in SHA speed. Fig. 14 depicts the settling of SHA when input is a sinusoid.

In all cases, the sampling instance is defined by the falling edge of the clock ϕ_1' .

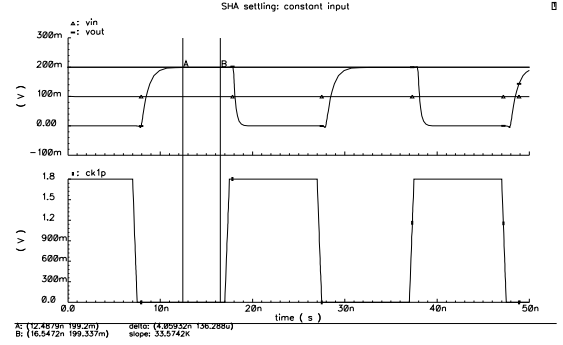


Fig. 12. The output settles to 199.34 mV when $v_{in} = 100$ mV.

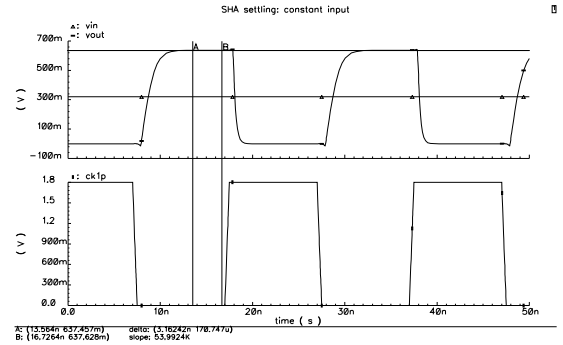


Fig. 13. The output settles to 637.63 mV when $v_{in} = 320$ mV.

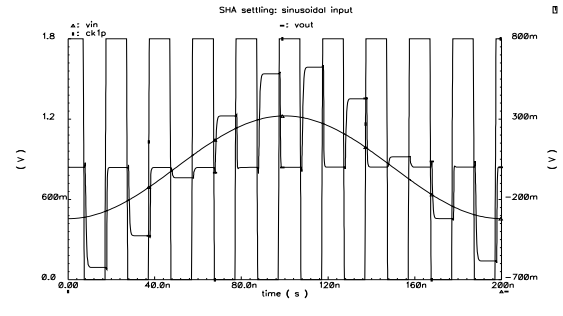


Fig. 14. Output $v_{out} = 2v_{in}$, where v_{in} is a sinusoid.

C. Comparator

The following table lists some metrics of the comparator.

Parameters	Values
Preamplifier gain (G_{pre})	2
Input offset	32 mV
I_D during amplification	185.8 μA
I_D during latching	351.6 μA
Average power dissipation	0.4837 mW
Regeneration time	1.5 ns
Overdrive recovery time	2 ns

The gain of the pre-amplifier is given by

$$G_{pre} = \frac{g_{m0}R_{on,8}}{2 - g_{m3}R_{on,8}}$$

(Refer to Fig. 9 for corresponding transistors.) $g_{m3}R_{on,8}$ is set to be approximately 1.2, which yields $G_{pre} \approx 2$.

Although we use a 1.5-bit-per-stage topology, the offset of comparator has to be carefully monitored to ensure that it doesn't exceed the capability of digital correction. To reduce the input offset M0, M1, M11, and M12 are sized relatively large. Large g_m for input transistors also helps to neutralize the offset contribution from the latch. The total input offset, which takes into account four pairs of transistors (M0-M1, M3-M4, M5-M6, and M11-M12), is well within the range of digital correction ($V_{ref}/4 = 160$ mV).

The preamplifier consumes a current of $185.8 \mu\text{A}$. When the latch is switched on, an additional $165.8 \mu\text{A}$ is burned. This gives rise to the average power dissipation of 0.4837 mW. There are 15 comparators in the system. Taking into account also 6 op-amps, the total power is about 16.56 mW. This leaves some room for digital logic and switching circuits.

Fig. 15 shows the result of a regenerative test. It takes the latch less than 1.5 ns to regenerate from 1 LSB to near rail-to-rail voltage. Shown in Fig. 16 are the overdriving tests for preamplifier recovery. The comparator recovers from full-scale voltage difference to 1 LSB in less than 2 ns.

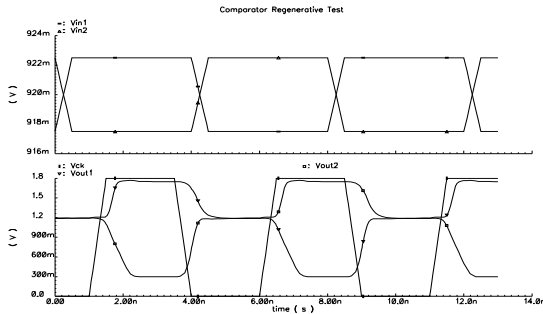


Fig. 15. Comparator regenerative test, v_{in} 's common level is 0.92 V.

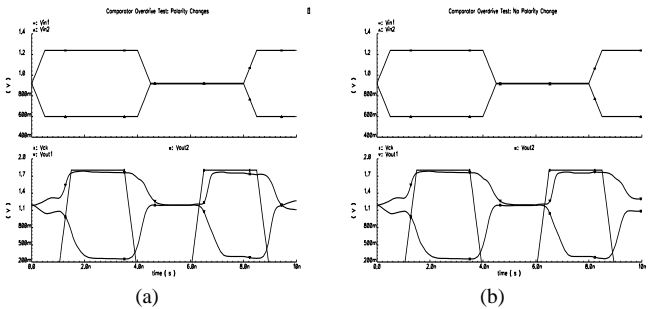


Fig. 16. Comparator overdriving tests (a) v_{in} 's polarity changes; (b) v_{in} 's polarity does not change. Comparator recovers correctly in both cases.

Fig. 17 shows a test of the digital circuitry $X, Y,$ and Z in Eq. (5). A full-scale sinusoid is used as the input. Its value is compared to $\pm V_{ref}/4$ by two comparators each time $ck2$

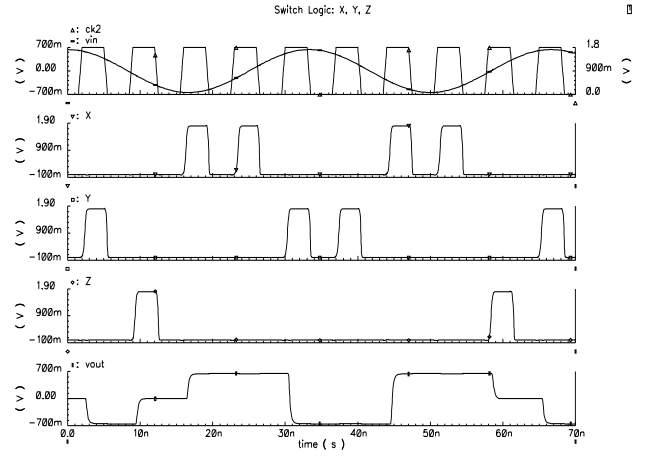


Fig. 17. X, Y, Z switch V_{out} to $\pm V_{ref}$ or common ground.

asserts high. Results of comparison are converted to switch controlling signals $X, Y,$ and Z . Accordingly, v_{out} in Fig. 10 is switched to $\pm V_{ref}$ or common mode level. Starting from the rising edge of $ck2$, digital signals $X, Y,$ and Z are fully generated in less than 1.5 ns, which is consistent with our comparator regenerative test. Since v_{out} is connected to 1 pF capacitor loads in this test, its value remains at previous level even after $ck2$ falls.

D. Single stage test

A set of simulation results are run to test the performance of a single ADC stage described in Fig. 2. First, two constant inputs 5 mV and 150 mV are used. The output reaches $1.992v_{in}$ about 5 ns and 7 ns after ϕ_1 's falling edge respectively, and it remains within 0.25 LSB of the final value. Fig. 18 shows their waveforms. In Fig. 19, we use $v_{in} = 300$ mV and 170 mV.

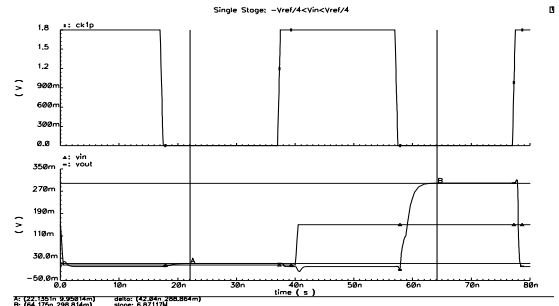


Fig. 18. Single stage test: $-V_{ref}/4 < v_{in} < V_{ref}/4$, $v_{out} = 2v_{in}$.

v_{out} settles within 0.25 LSB of the nominal output $2v_{in} - V_{ref}$ in about 6 ns and 7 ns respectively. Fig. 20 shown the result when $v_{in} = -630$ mV and -400 mV. Both outputs settle in less than 6 ns. In all the simulations, the SHA output satisfies our gain error requirement set out in section II-C.

The last simulation is to determine the worst case T in Eq. (6), and deduce the minimum clock period. In Fig. 21, the input is switched from -640 mV to 640 mV and back to -640 mV. The worst case settling time in this sequence is

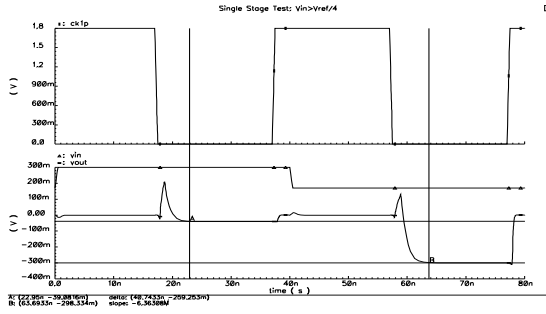


Fig. 19. Single stage test: $v_{in} > V_{ref}/4$, $v_{out} = 2v_{in} - V_{ref}$.

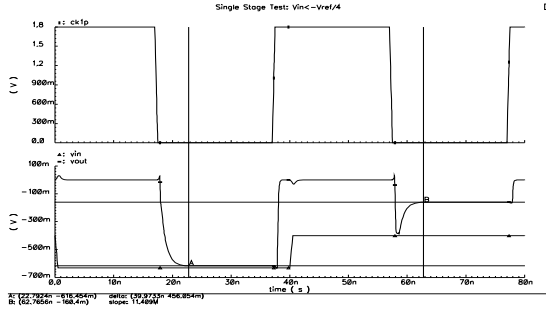


Fig. 20. Single stage test: $v_{in} < -V_{ref}/4$, $v_{out} = 2v_{in} + V_{ref}$.

found to be $T = 5.74$ ns. Note that T defined in Fig. 11 is relative to the end of ϕ_2 's falling edge, which is 1 ns behind the reference we used in Fig. 18~20. For this reason, ck2 instead of ck1p is plotted in Fig. 21. If we choose $T = 6$ ns and

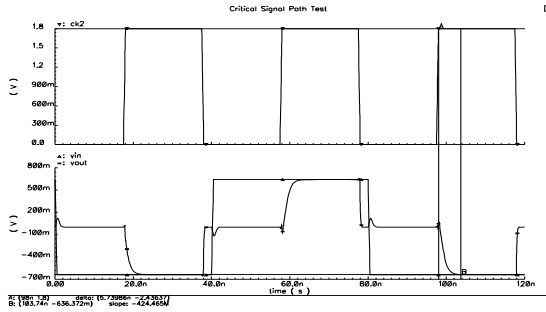


Fig. 21. Critical signal path test: $v_{in} = -640$ mV, 640 mV, -640 mV.

$\Delta T = T_{tran} = 0.5$ ns, the minimum clock period is $T_{ck} = 14$ ns, which yields a sampling frequency of 71.4 MHz. To leave some safety margin our clock frequency is set at 50 MHz.

E. Complete ADC system

The overall pipelined ADC is set up as described in Fig. 1. Since there are many devices in the system, the simulation takes a long time. Insufficient time prevents us from running a full set of simulations to gauge ADC's linearity. Instead, as an indication of the full system's functionality, a trivial simulation is showcased here. For simplicity, op-amp and comparator offsets are disabled. We feed a 1 LSB (5 mV) input to the system, and observe the signal ripples through pipelined ADC and produces meaningful digital output levels. The outputs of

stage 1 through stage 6 are shown in Fig. 22 and 23. They settle to the values in the following table as the input signal propagates through the pipeline.

stage	1	2	3
v_{out} (mV)	-9.96	-19.84	-39.52
stage	4	5	6
v_{out} (mV)	-78.80	-157.2	-313.5

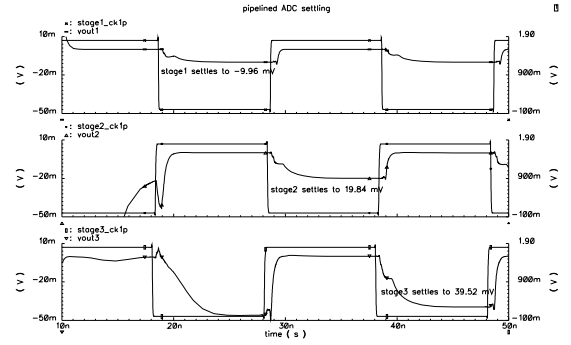


Fig. 22. Outputs at stage 1 through 3 when $v_{in} = 5$ mV.

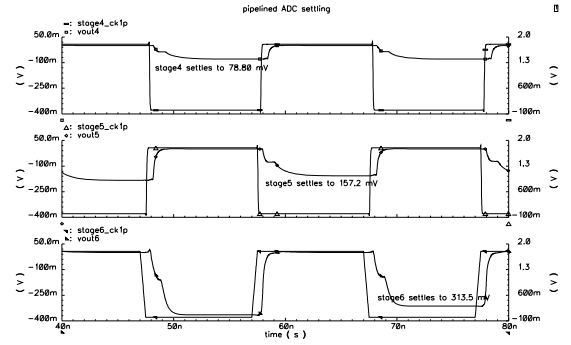


Fig. 23. Outputs at stage 4 through 6 when $v_{in} = 5$ mV.

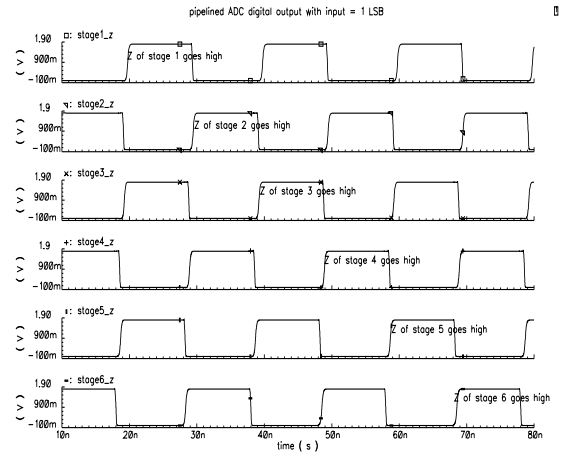


Fig. 24. Digital signal Z at stage 1 through 6.

Instead of comparator output levels, we plotted the digital level Z of Eq. (5) in Fig. 24. They produce all ones, which are correct decisions.

IV. CONCLUSION

Experience belies the claim that the complexity of pipelined ADC grows linearly with number of bits. Although pipelined ADC offers a more streamlined structure than flash ADC, it demands high performance op-amps, which directly affects the gain error and SHA settling speed. Moreover, at high precision, capacitor and charge injection mismatches come into the picture, and eventually, the complexity of the overall system becomes comparable to that of a flash ADC.

This project also offers valuable hands-on experience on analog integrated circuit design. The need to balance multiple design objectives such as power consumption, speed, accuracy, linearity, output swing, makes the process challenging and often intriguing.

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