

Programmable Gigabit Ethernet Packet processor

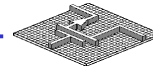
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Acknowledgement to



MICRO
University of California

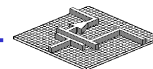
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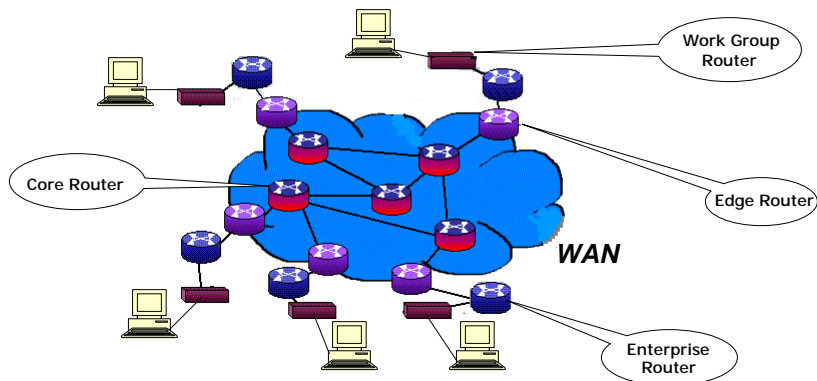
Outline

- Introduction
- Problem description
- Available Solutions
- Proposed solution (fully integrated programmable processor)
- Design Methodology
- OCAPI , Parsec, NS, Standard C++ ????
- Results
- Preliminary architecture
- Work in Progress
- Conclusion

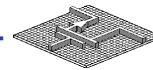
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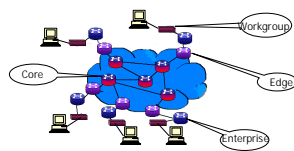
Introduction



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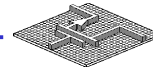


Introduction

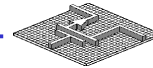
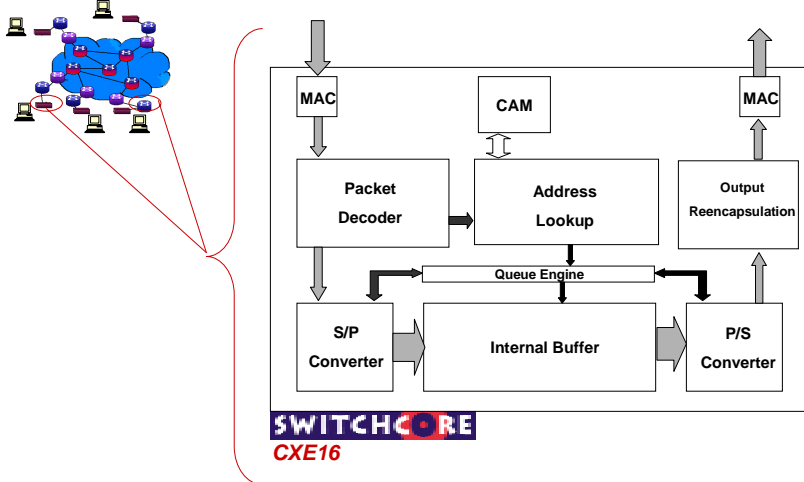


	Workgroup Router	Enterprise Router	Edge Router	Core Router
Data Rate (Packet/sec)	6 – 10 Millions	10+ Millions	2 – 4 Millions	30+ Millions
Physical Size	"Pizza box" size	Rack sized Modular box	Small Size	Room Size
Environment	Only Homogeneous	Primarily homogeneous	Heterogeneous	Heterogeneous
Protocols	All ATM (or) All Ethernet	All ATM (&) All Ethernet	Ether, ATM, DSL, T1,.....	DSL T1
Implementation	Integrated Switch	Integrated Switch	Network Processor	Dedicated Switch

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Introduction



Problem Description

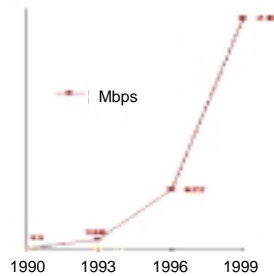
- The Gigabit Ethernet Router is a very fast switch

Single port:

1Gbit port = 1.5 Million packet/sec

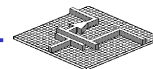
10 ports:

15 Million packet/sec



- New protocols are emerging for different application and to improve the QoS. (Video, Audio .. Etc)

➔ **Fast & Flexible**



Available Solutions



- Processor based General Purpose CPU) 

- *Very flexible*
- *Very slow*

⇒ { Router cannot support 1Gbit port }

- On board programmable router 

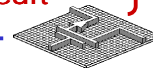
- *Flexible*
- *Board level problems (Speed, power, etc..)*

- Fully integrated ASIC Solution 

- *Very fast*
- *Not Flexible*

⇒ { Upgrading is difficult }

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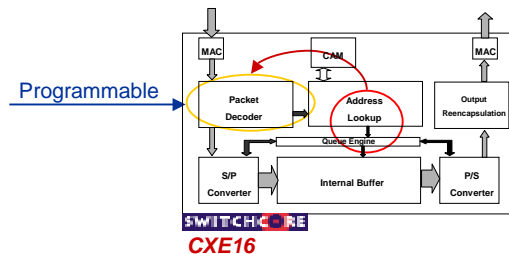


Proposed Solution

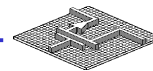


- Fully Integrated Programmable Router

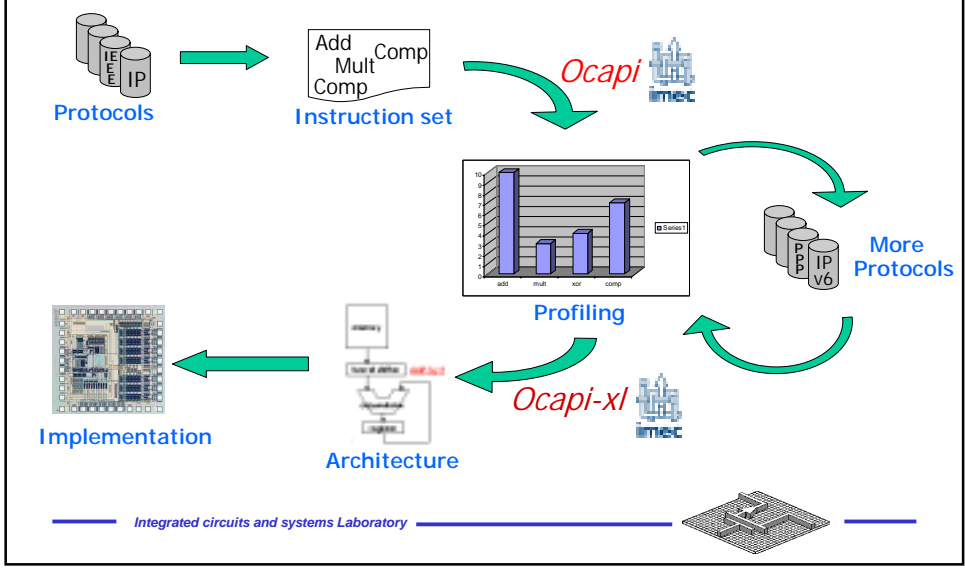
- *Very flexible*
- *Very fast*



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Design Methodology UCLA



OCAPI, Parsec, NS, Standard C++ UCLA

PARSEC vs. *NS*

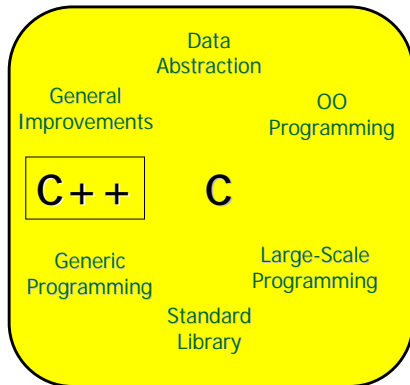
- | | |
|--|---|
| <ul style="list-style-type: none"> • C based parallel Simulator • More suitable for wireless networks (GloMoSim) • Don't describe hardware. (high level description only) • No Profiling | <ul style="list-style-type: none"> • C++ based Network Simulator • Frontend : Tcl
<i>Wired network</i> • Backend : C++
<i>Wireless network</i> • Don't describe hardware. (high level description only) • No profiling |
|--|---|

OCAPI , Parsec, NS, Standard C++

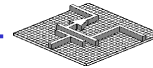
C++

vs.

OCAPI



- C++ class library
- Contains support for:
 - * Values (floating , fixed)
 - * Algorithm and Architecture modeling.
 - * Dataflow and cycle-true simulation
- Code generation to VHDL and Verilog.
- Test-bench generation to VHDL and Verilog



Results

L2 Protocols

IEEE 802.3/802.2 SNAP Encapsulation (RFC 1042)

DA	SA	Length	AA AA 03	Org. code	EType	Data	CRC
6	6	2	3	3	2		4

Ethernet II Encapsulation (RFC 894)

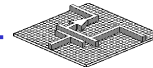
DA	SA	Etype	Data	CRC
6	6	2		4

NetWare 802.3 RAW Encapsulation (IPX only)

DA	SA	Length	IPX-Checksum	Data	CRC
6	6	2	2		4

IEEE 802.3/802.2 Encapsulation

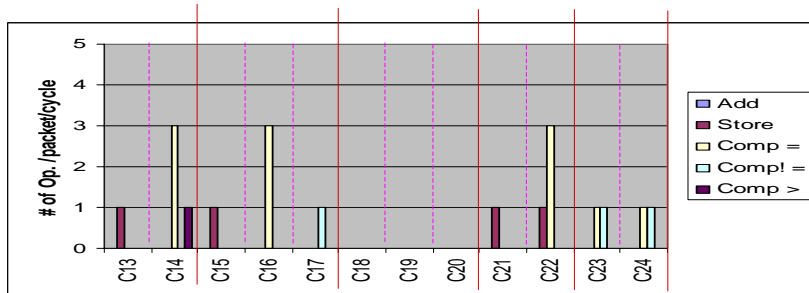
DA	SA	Length	LLC	Data	CRC
6	6	2	3 or 4		4



Results



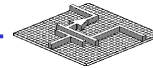
L2 Parser



DS	SA	Length	AA AA 03	Org. Code	Etype	Data	CR C
6	6	2	3	3	2		4

IEEE 802.3/802.2 SNAP Encapsulation (RFC 1042)

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Preliminary Results



L3 Protocols

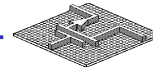
IP Datagram

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Version				IHL				TOS								Total length															
Identification										Flags		Fragment offset																			
Time to live					Protocol					Source IP address					Header checksum																
Destination IP address										Options																					
Data																															

IPX Datagram

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
IPX Checksum																Total length															
Hop Count				Packet type				Destination Network Address (part I)																							
Destination Network Address (part II)										Destination Node Address (part I)																					
Destination Node Address (part II)																															
Destination Socket Number																Source Network Address (part I)															
Source Network Address (part II)										Source Node Address (part I)																					
Source Node Address (part II)																															
Source Socket Number																															

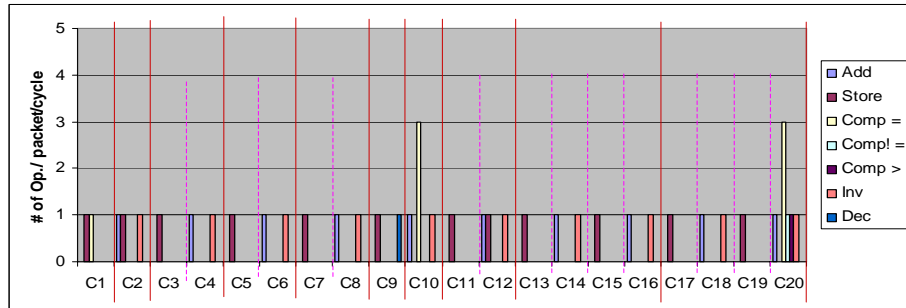
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Results



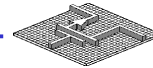
L3 -IP Parser



Ver	TOS	Length	Identify	Fragmet	TTL	Pro	CheckS	IP SA	IP DA	Data
1	1	2	2	2	1	1	2	4	4	

IP

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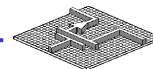
Results Summary

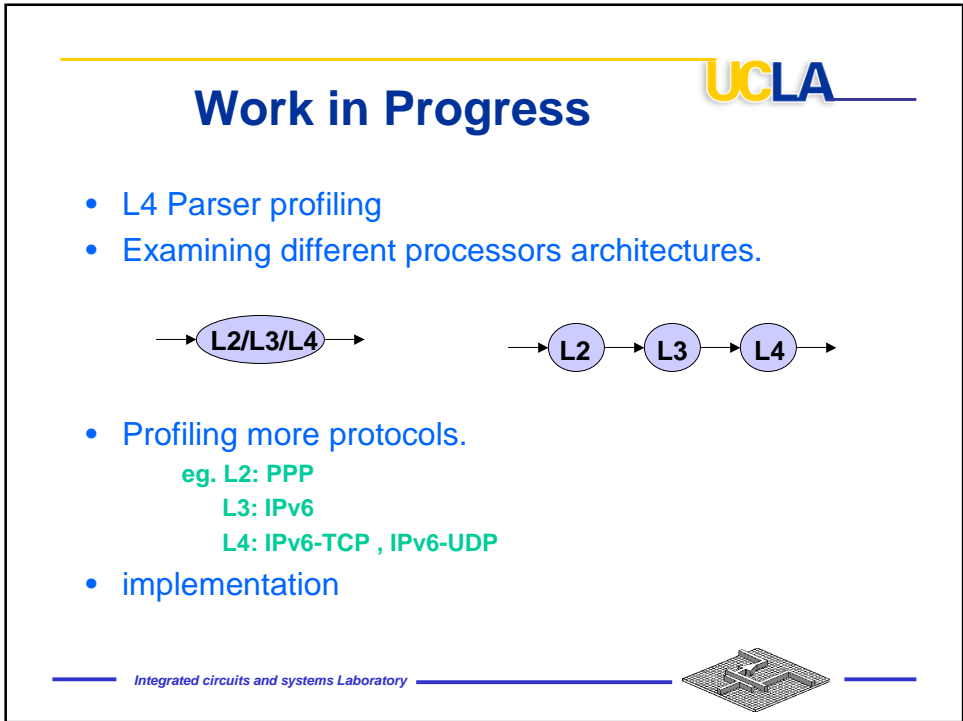
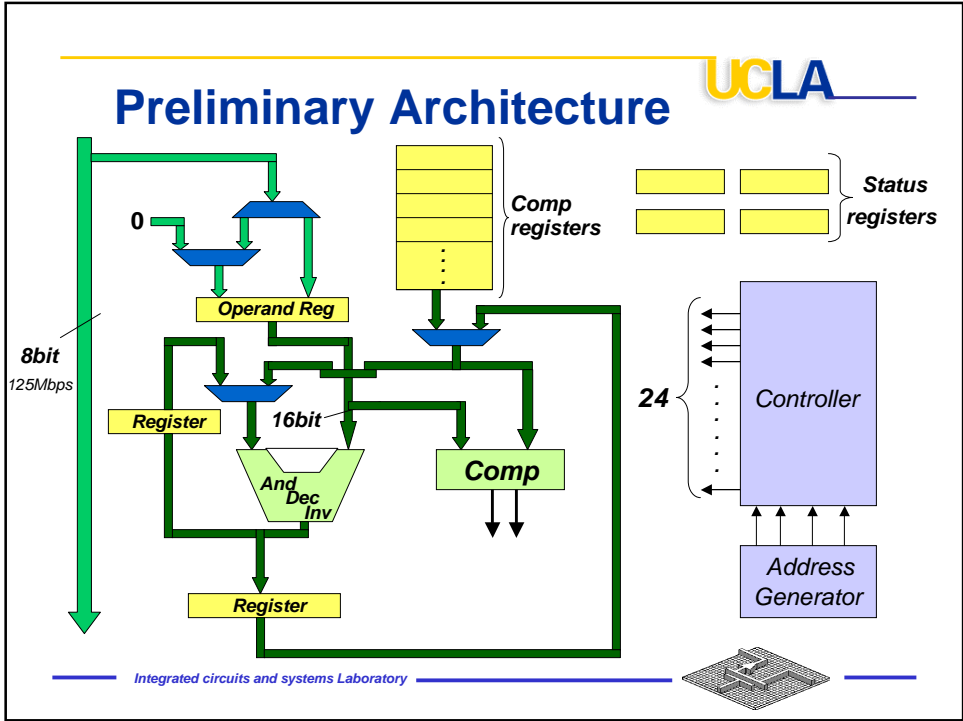


- 16 bit datapath
- Maximum number of operations per packet per cycle:

	L2	L3
Add	0	2
Store	1	1
Comp =	3	3
Comp !=	1	1
Comp >	1	1
Inv	0	1
Dec	0	1

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Conclusion

UCLA

- Workgroup and Enterprise routers:
 - * Require **high speed** processing.
 - * Will be **obsolete** soon.
- Current solutions are either too general (slow) or too specific (rigid).
- Using the proposed design methodology, a **flexible domain specific** architecture is obtained.
- The same design methodology could be applied to 10Gbit and 100Gbit routers.

