

EE213A
Spring, 2000
Professor Ingrid Verbauwhede

HW2 Solution

Problem1 (15 points)

1) Horner expansion rule (3 points)

$$\mathbf{0.375 = 0.011 = 2^{-2}(1+2^{-1}) \text{ or } 0.1-0.001 = 2^{-1}(1-2^{-2})}$$

In this case CSD notation has the same amount of bits. Please note that for accuracy reasons the Horner expansion rule is used.

0.175 can not be represented with a small number of bits. So, we need to investigate what can be represented by 8 bits. With 2 pipelined adders in the loop, there is room for bit repeaters up to 2^{-6} and two non-zero bits. With 3 pipelined adders in the loop, there can be 3 non-zero bits, but only up to 2^{-5} . This leaves the following solution:

$$\mathbf{0.175 = 0.0011 = 2^{-3}(1+2^{-1})}$$

This solution assumes that the adders have a unit pipeline delay and the bit repeaters have no pipeline delay (as is the case in the chapter13 of “VLSI Digital Signal Processing”). In case a pipelined bit repeater is used, even less numbers are possible.

2) The two implementations are equivalent? (4 points)

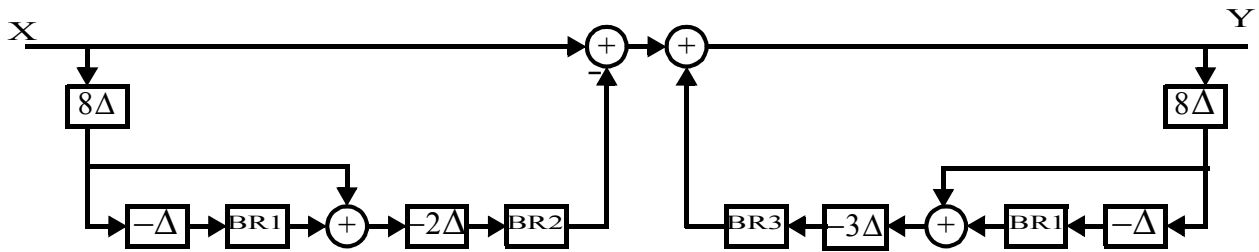
Coefficient quantization error only occurs in the pole section. Therefore, the direct form I will have less quantization noise propagation. In the canonic form, the quantization noise will propagate through the pole and zero section.

Roundoff noise is present in both sections. But following the guidelines of the lecture on fixed point effects, one should put the section with the largest coefficients up front (least amount of shifting and thus truncation error.)

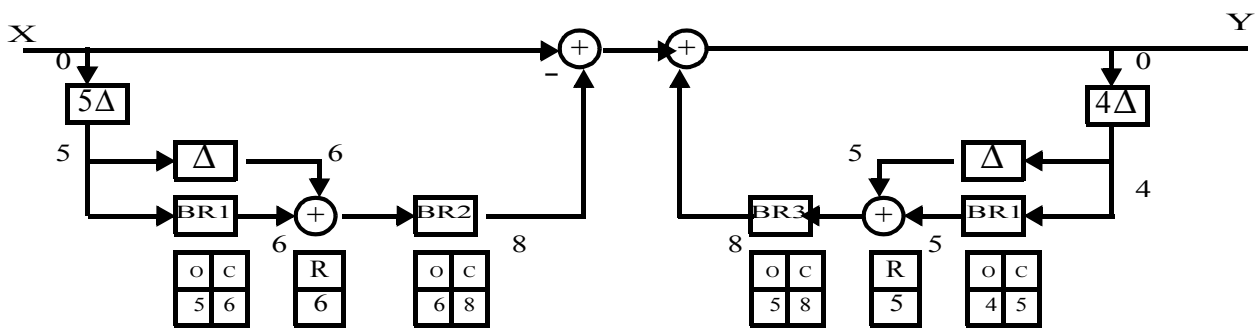
Thus, for this design, the direct form I will introduce least amount of digital noise.

3) Implementation (8 points)

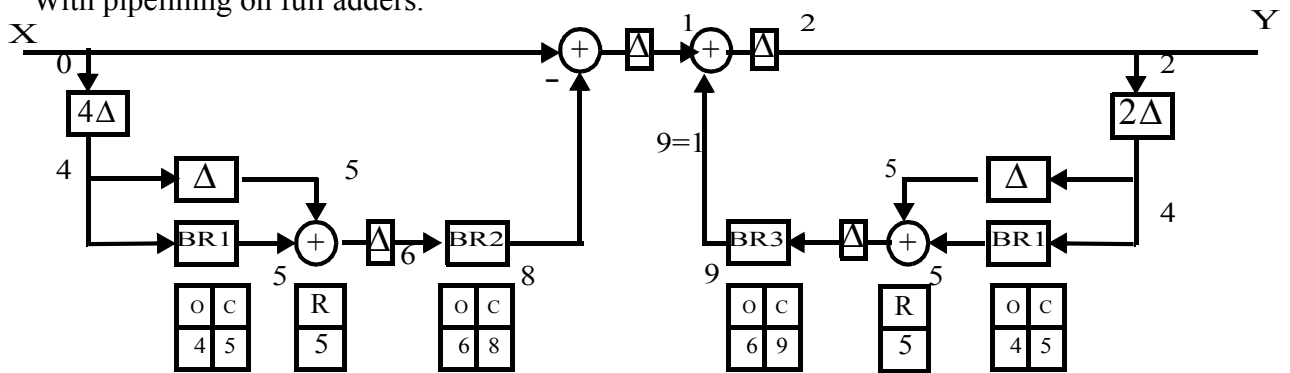
(a) Direct form I



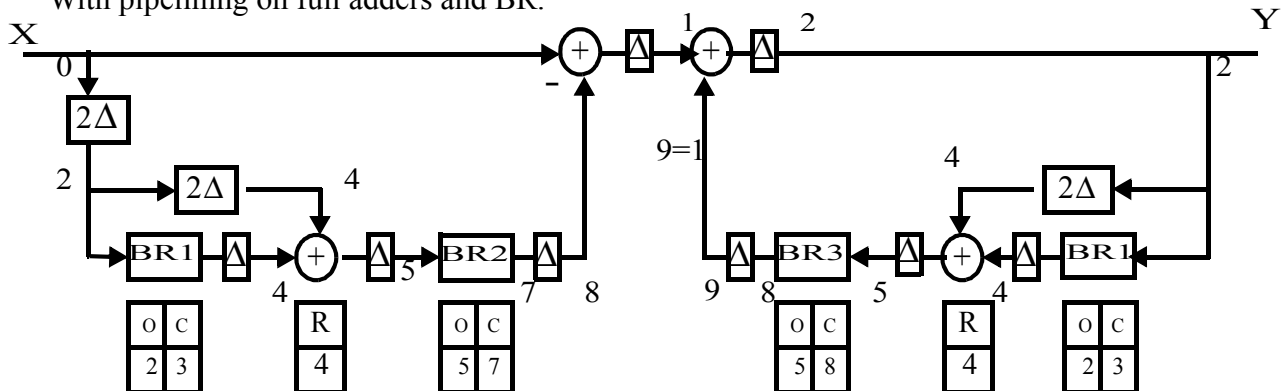
Without pipelining.



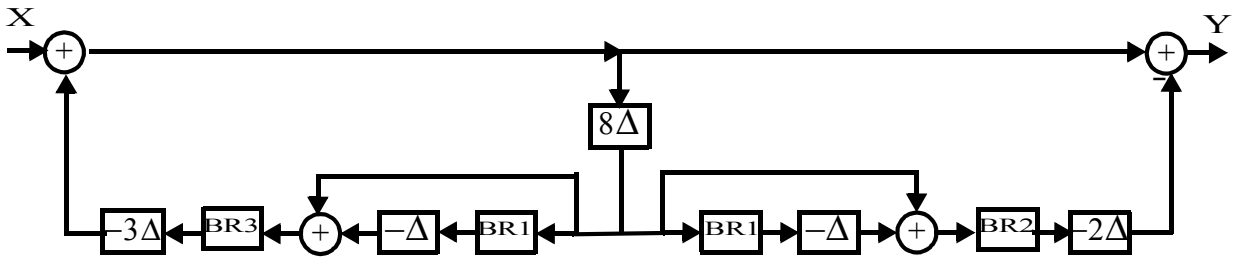
With pipelining on full adders.



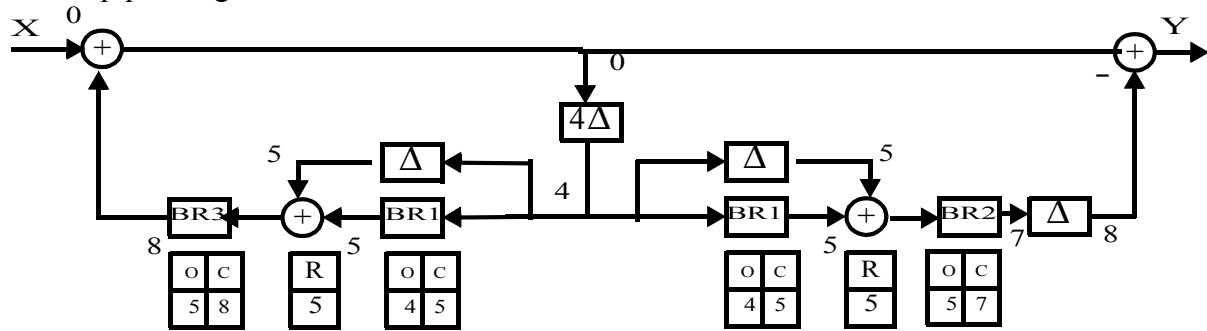
With pipelining on full adders and BR.



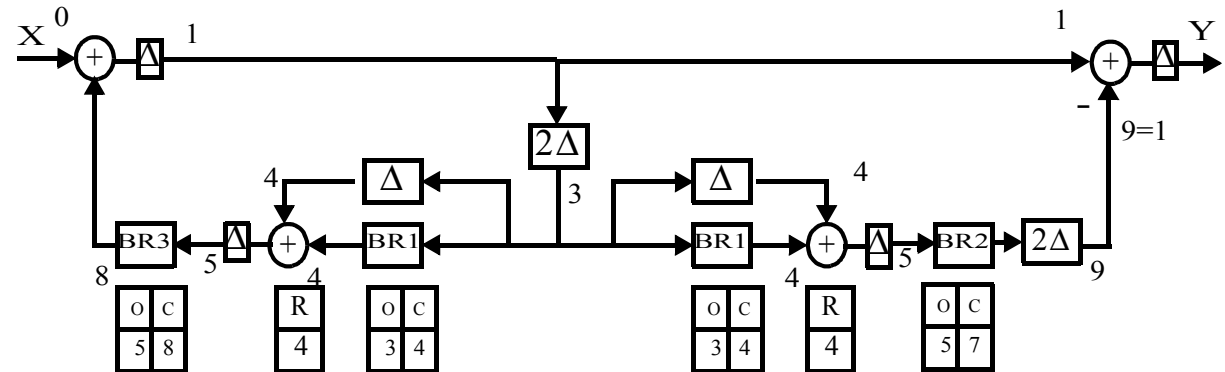
(b) Canonic form



Without pipelining.



With pipelining on full adders.



With pipelining on full adders and BR.

