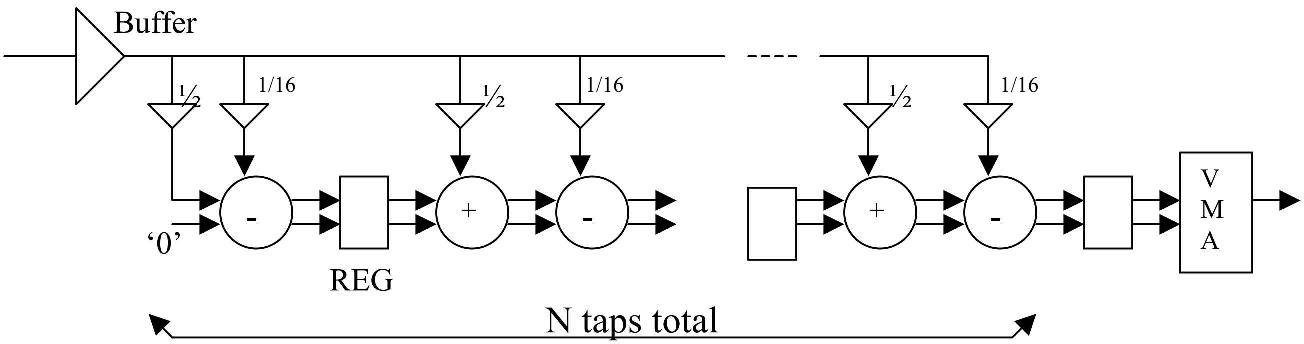
Problem 1:

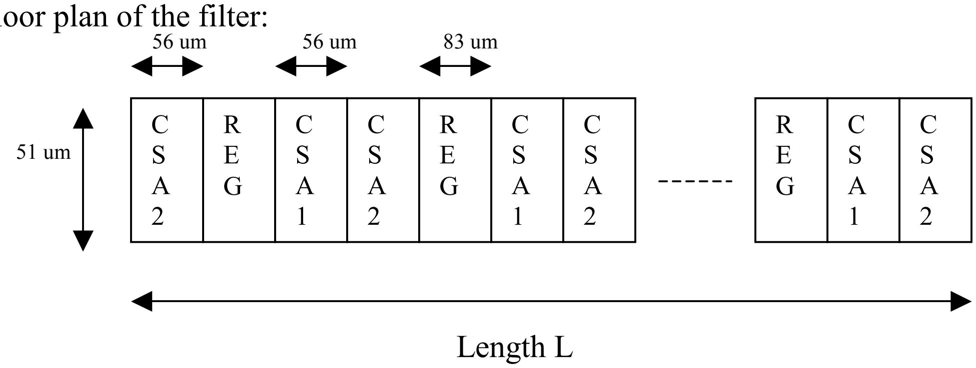
Every tap has the same CDS coefficient 0.4375 (= 1/2 – 1/16) or $(2^{-1} - 2^{-4})$ or 0.100(-1).

Non-folded FIR presented in "FIRGEN: A Computer-Aided Design System for High Performance FIR Filter Integrated Circuits."
Input X: n-bit word
Output Y: n-bit word.



Let denote CSA1: Adder.
CSA2: Subtractor.

The critical path will be $T_{critical} = \max \{ T_{buf} + T_{reg} + T_{csa1} + T_{csa2} , T_{VMA} \}$
We need to draw the floor plan to calculate the buffer delay time.
Floor plan of the filter:



$L = N*L_{csa2} + (N-1)*(L_{csa1} + L_{reg}) = N*56\ um + (N-1)*(56+83)\ um = (N*195 - 139)\ um.$

For each data bit line:
Capacitance load $C_{load} = N*C_{csa2} + (N-1)*C_{csa1} + C_{routing}$ (here, C_{reg} is ignored).

Due to MSB extension in 2's compliment, sign-bit is loaded by input capacitance of more adders than other bits. In this problem, sign-bit will be extended one position for coefficient ½ (or loaded by **2** CSA1s), and four positions for the coefficient 1/16 (or loaded by **5** CSA2s). And the sign-bit line delay is used to calculate critical path delay.

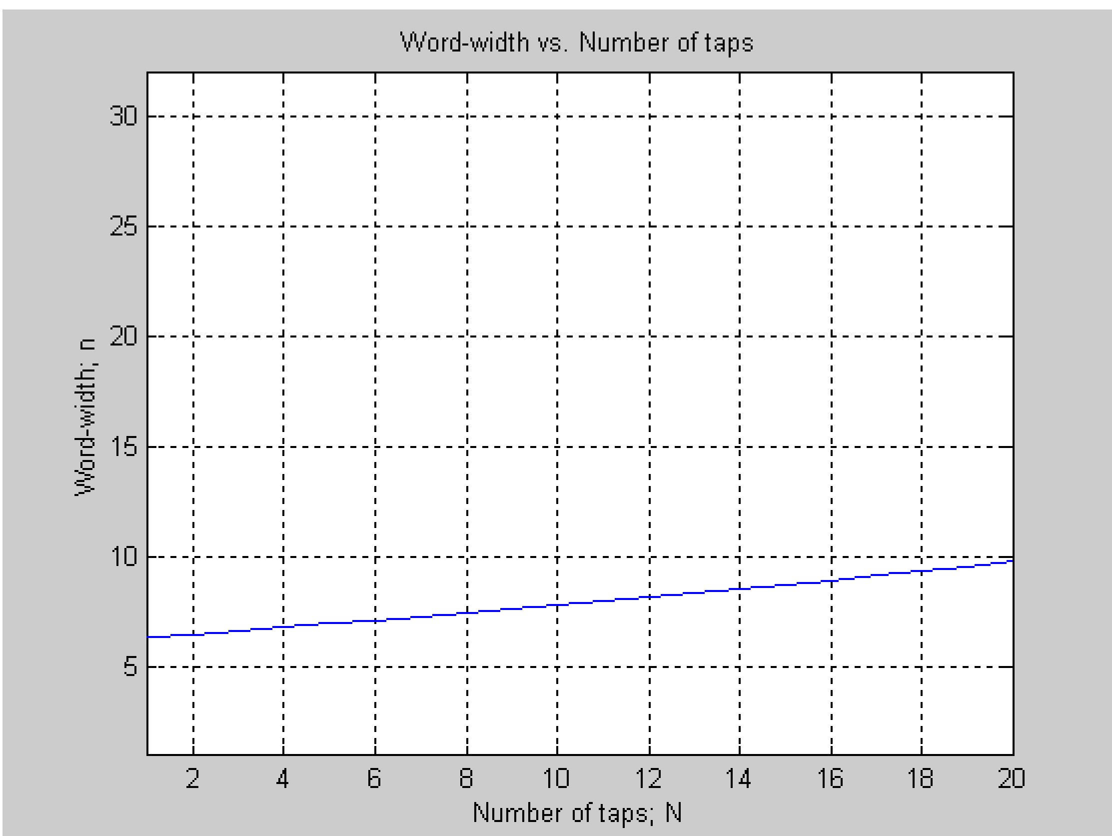
Capacitance load $C_{load} = N*(5*0.10)\ fF + (N-1)*(2*0.10)\ fF + L*0.25\ fF/um.$
$= N*(5*0.10)\ fF + (N-1)*(2*0.10)\ fF + (N*195 - 139)*0.25\ fF$
$= 0.5N + 0.2N - 0.2 + 48.75N - 34.75 = (49.45N - 49.47)\ fF.$

$T_{critical}$ = max { $T_{buf} + T_{reg} + T_{csa1} + T_{csa2}$, T_{VMA}}
= max {$(2 + 2*C_{load}) + T_{reg} + T_{csa1}$ + Tcsa2, T_{VMA}}
= max { $(2 + 2*(49.45N - 49.47)\ 10^{-3}) + 2 + 2 + 2$, $3.0*\log_2 n$}
= max {$7.90106 + 0.0989N$, $3.0*\log_2 n$}

Therefore, $3.0*\log_2 n = 7.90106 + 0.0989N$
$\log_2 n = (7.90106 + 0.0989N)/3$
$n = 2^{(7.90106 + 0.0989N)/3}$

Using MATLAB to plot the critical path:

```
n=[0:32];
N=[1:20];
n=(2.^((.0989*N+7.90106)/3)),
plot(N,n),
grid,
axis([1,20,1,32]),
xlabel('Number of taps; N'),
ylabel('Word width; n'),
title('Word width vs. Number of taps')
```



At the curve, $T_{critical} = T_{VMA}(n) = T_{RC}(N)$
Above the curve, $T_{critical} = T_{VMA}(n)$ (a function of word width n).
Under the curve, $T_{critical} = T_{RC}(N)$ (a function of RC line, or number of taps N).

Problem 2:

In the handouts, the number of adders in the critical path of the carry tree is approximately $\log_2 N$ because carry-ripple adders are used here. For each carry-ripple adder, CRA_i, the carry-out signal $C_{out\ i}$ is rippled across the horizontal direction. Therefore, for two inputs A_i and B_i , only one output S_i is broadcasted down the tree. The ratio of "down tree" is 2:1. The critical path will contain $\log_2 N$ carry-ripple adders.

In contrast, in the paper "FIRGEN: A Computer-Aided Design System for High Performance FIR Filter Integrated Circuits", carry-save adders, CSAs, are used in the tree. At each CSA_i, for three inputs C_i , A_i , B_i there are two outputs C_{outi} , S_i are broadcasted down the tree. The ratio is 3:2 or 1.5. Therefore, the number of CSAs in the critical path will be $\log_{1.5} N$ approximately.

Problem 3:

COMPANY	ARCHITECTURE	TARGET APPLICATION	PRODUCT
3DSP Corp. http://www.3dsp.com	Fixed-point DSP	Digital Still Camera, PC camera	Software: Assembler and linker, C simulator, compiler, Analysis tools. Hardware: SP5 DSP.
ARC Cores Ltd. http://www.arccores.com	32-bit RISC	High-perform processing engine. High-Bandwidth protocol engine. System controller	Software: MetaWare High C tool. Soft solution: VHDL for synthesis.
BOPS, Inc. http://bopsnet.com	ManArray: (iVLIW, SIMD, Multi-processing and Cluster Switch)	Multimedia: Digital video, camera. Wireless: Handset, base station. Internet: VOIP, DSL	Software: Software Dev Kit. Soft solution: BOPS (2010, 2020 2040) IP cores.
Chameleon Systems http://www.chameleonsystems.com	ARC synthesizable 32-bit RISC-based engine.	Data Streaming Telecom.	Software: C and HDL Dev. tool. Hardware: SOC platform.
Improv Systems Inc http://www.improvsys.com	VLIW programmable.	Multi-channel Communication. Media Processing	Hardware: SOC platform.
Lexra Inc. http://www.lexra.com	RISC-DSP core based on MIPS achitecture.	Embedded Processor.	Soft solution: RISC-DSP cores.
Massana Ltd. http://www.massana.com	Hardwired DSP.	Internet: Ethernet, DSL Multimedia: Digital TV	Software: DSP design tools Soft solution: DSP coprocessor Cores
Morphics Technology Inc. http://www.morphics.com	Reconfigurable baseband processor	Wireless communications systems	Soft solution: reconfigurable DSP Cores for wireless
Mysticom Ltd. http://www.mysticom.com	Gigabit Ethernet	Internet: High-speed modem. Ethernet. LAN.	Soft solution: DSP-based 10/100BASE-TX Fast Ethernet PHY Core
SandCraft Inc. http://www.sandcraft.com	Montage architecture.	Multimedia: Digital TV, set-top boxes. Internet: appliances, routers, switches.	Hardware: SOC platform. Soft solution: advanced microprocessor cores.
SSL Design, Ltd. http://www.ssldesign.com	ARM7TDMI RISC processor.	Wireless Communication. Consumer Multimedia.	Hardware: Smart phone IC Platform. Soft solution: Link Controller IP.
Systolix Ltd. http://www.systolix.co.uk	PulseDSL.	Communications. General Signal Filtering and Conditioning. Industrial Instrumentation and Control Systems. Automotive & Aviation Electronic Systems.	Software: Systolix Design System. PulseDSP compiler. Soft solution: Standard PulseDSP Core.