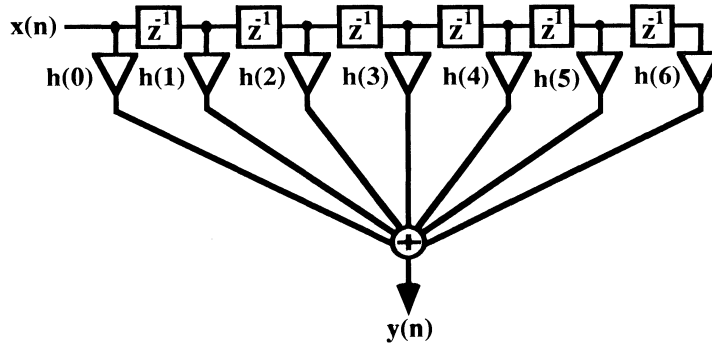
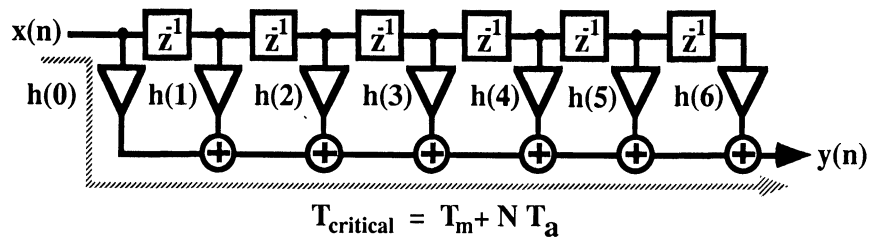


High Speed FIR Filter Implementation

Generic FIR Filter Structure



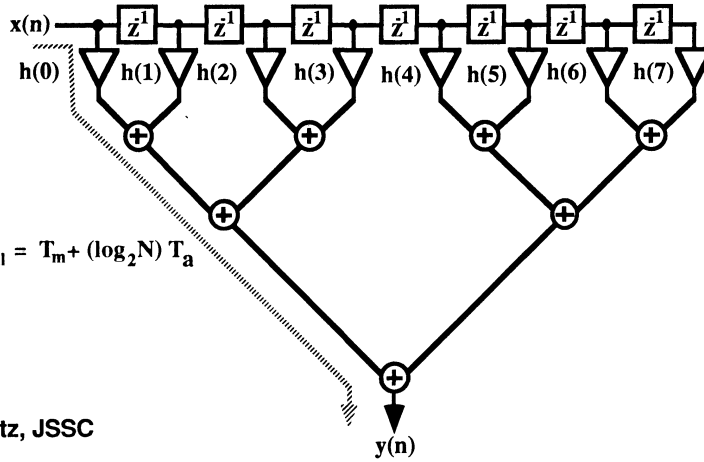
Direct Form FIR Filter Structure



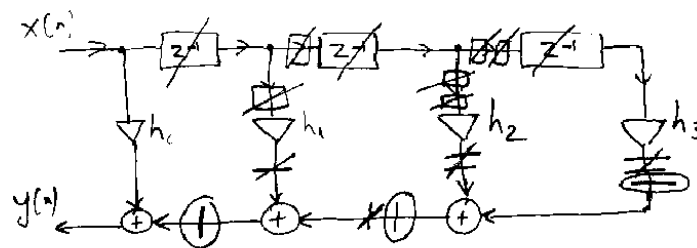
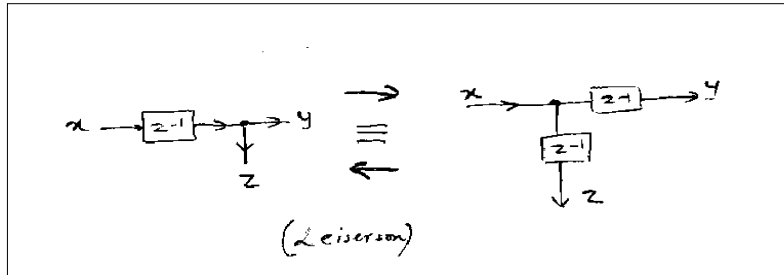
T_m = multiplier delay
 T_a = adder delay
 N = filter order

Associative Transformation

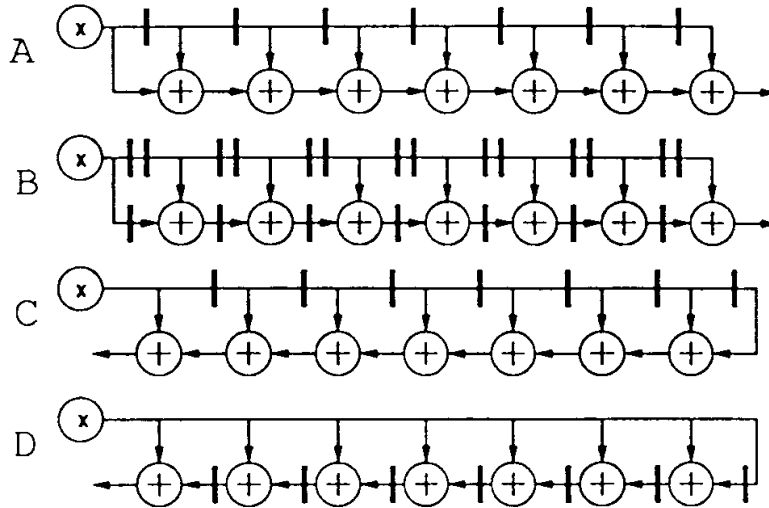
Direct Form Structure with Adder Tree



Associative Transformation and Retiming

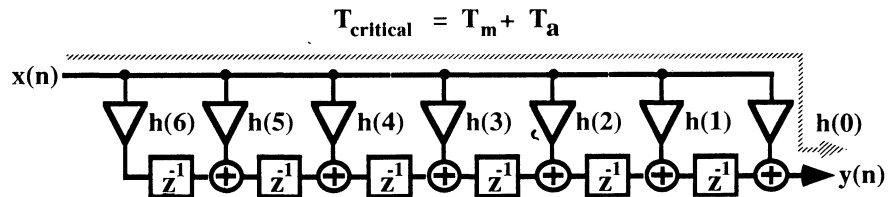


Associative Transform and Retiming

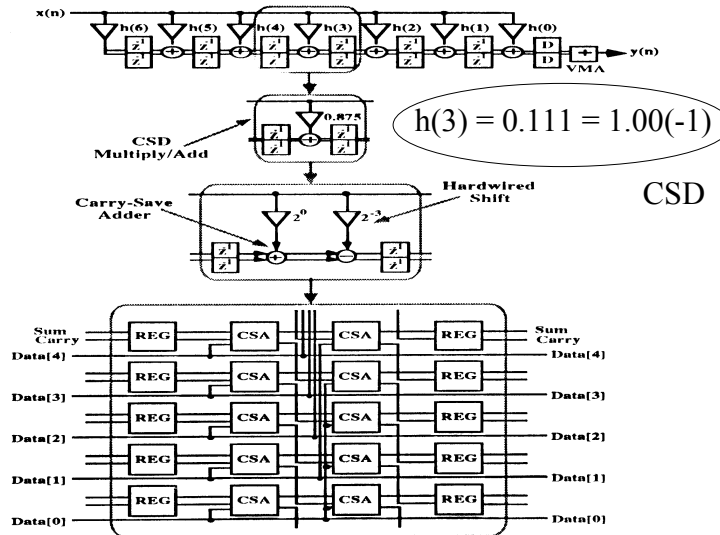


Associative Transform and Retiming

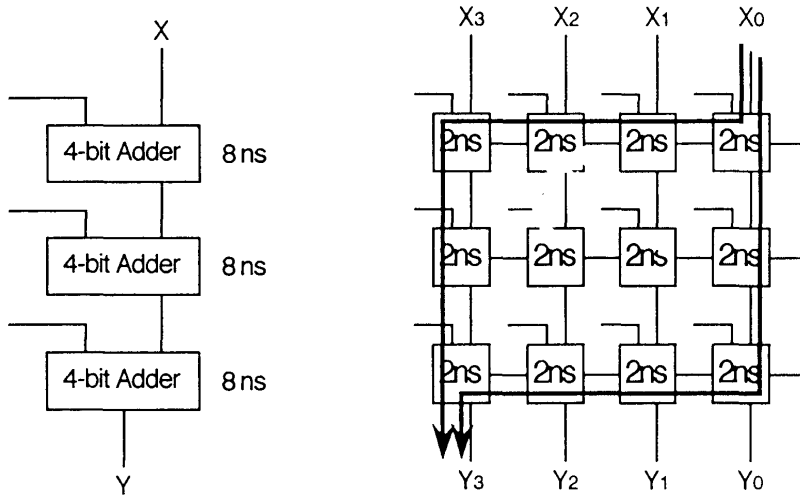
Transpose Form Structure



Architecture Detail



Accurate Timing Calculation

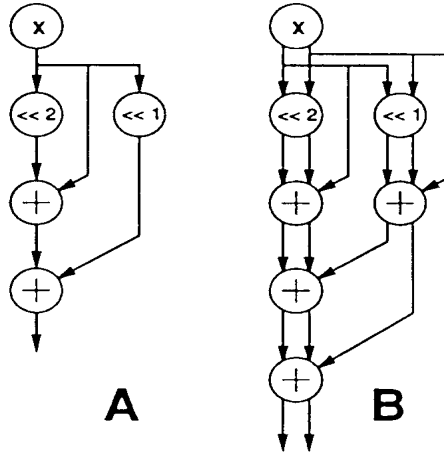


Word-level model:
delay of 24ns is incorrect

Bit-level model:
correct delay of 12ns

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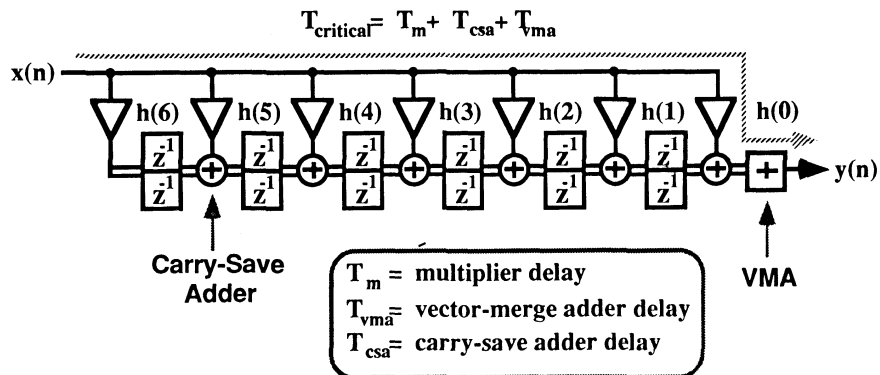
Carry-save addition vs. carry-ripple



Carry-save with fanout

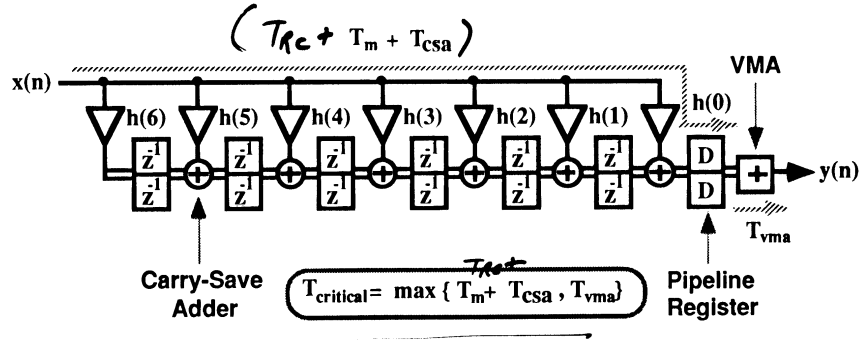
UCLA

Transpose Form with CSA & VMA



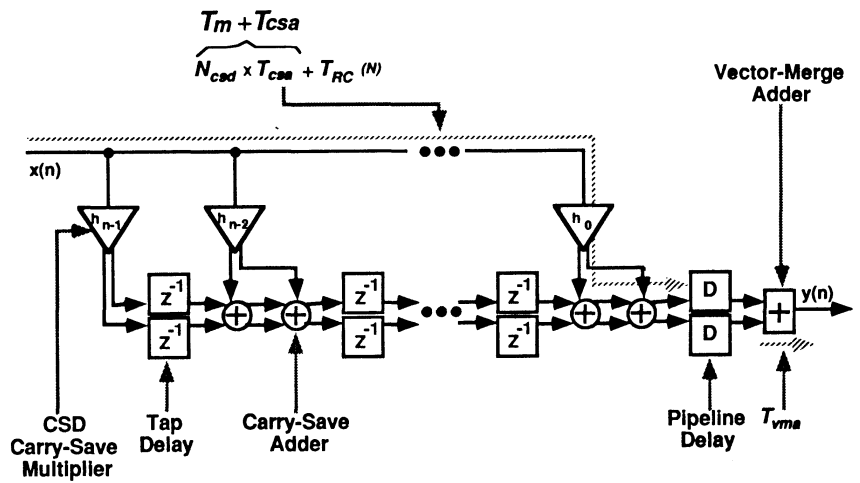
● Ulbrich & Noll, ISCAS

One-Stage Pipelined Transpose Form with CSA & VMA

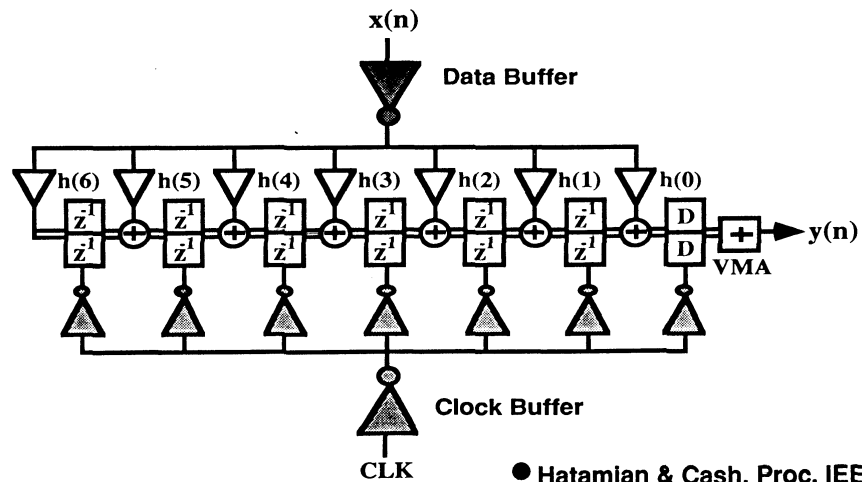


- Ulbrich & Noll, ISCAS
- Lin & Samueli, ISCAS

FIRGEN Filter Architecture



Data & Clock Distribution Network



Sign-bit Loading

- Due to MSB extension in 2's complement, sign-bit is loaded by input capacitance of more adders than other bits
- Layout level solution: bigger buffer for sign-bit
- Algorithm level solution: do not sign extend, add compensation signal

Sign-bit Loading

- Given $x(n) = 1.11$ (i.e. -0.25) consider $2^{-1}x(n) = 1.111$ i.e. (-0.125)
↑
(extension)

- Instead of extending sign-bit, add "0" in all sign-bit locations except right-most, add sign-bit inverse in right most position:

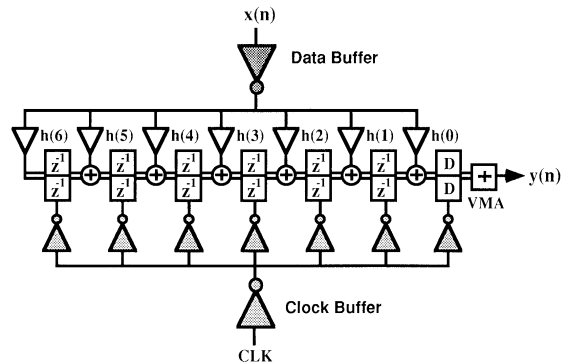
i.e. modify $2^{-1}x(n)$ to: 0.011
↑
(sign-bit inverse)

- After the shift and add operation, add a compensating signal with "1" s in all the sign-bit extension positions:

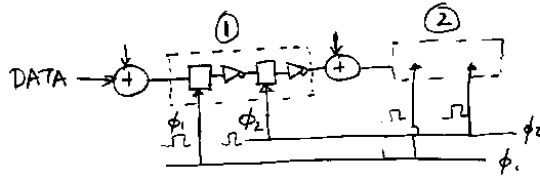
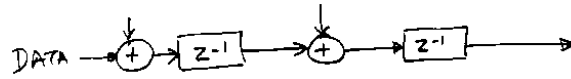
$$\begin{array}{r} 0.011 \\ +1.100 \\ \hline \underline{1.111} \end{array}$$

Floorplan Generation for High-Performance Layout

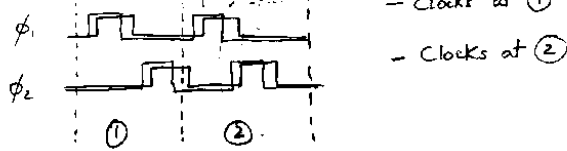
- Floorplan essential to ensure proper data and clock distribution network for minimized clock and data skew
- Example: Steiner tree distribution network for FIR filter



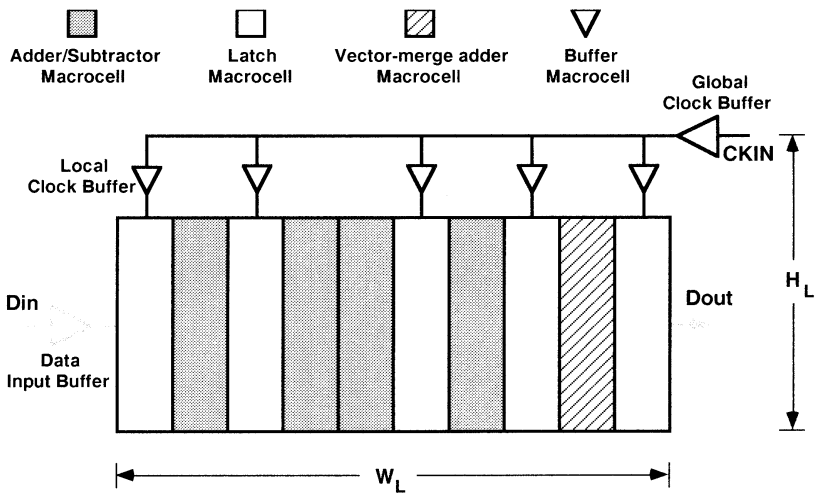
Clock/Data Routing vs. Clock Skew



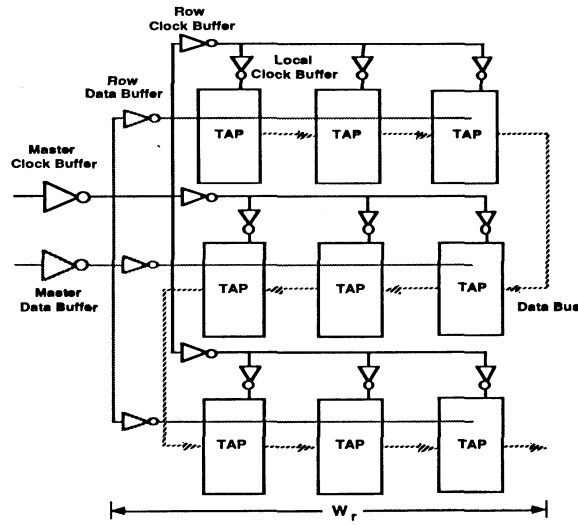
Case I. Clock generator at left (same side as data src).



Linear Floorplan

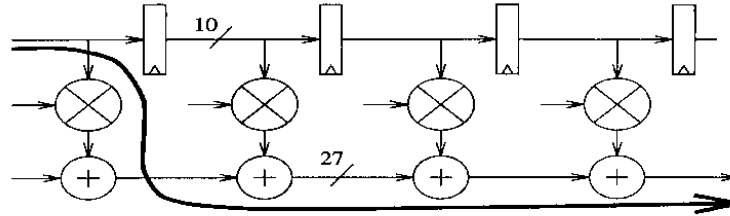


Folded Floorplan

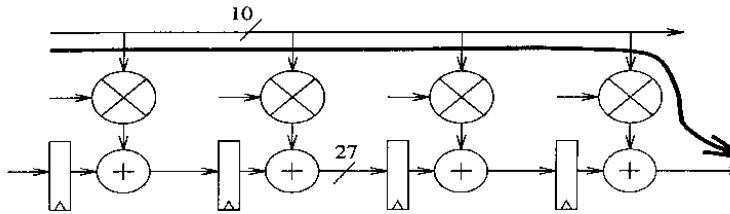


Low Power FIR Implementation

Direct Form: Low Power (10b flip-flops), Long Critical Path (series adders)



Transposed Form: High Power (27b flip flops), Short Critical Path (1 MAC)



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- Since critical path is smaller, for the same sample rate we can drop voltage for transpose form to reduce power consumption
- As voltage reduces towards threshold voltage, V_{dd} has hard lower bound
- If additional register power is too large voltage reduction may not compensate
- Hybrid architecture: direct form for m-taps, transpose in between

UCLA

Reference:

R. Jain, P. Yang, T. Yoshino, "FIRGEN: A Computer-Aided Design System for High Performance FIR Filter Integrated Circuits," IEEE Transactions on Signal Processing, Vol. 39, No. 7, July 1991, pg. 1655-1668.