Electrical and structural properties of shallow p^+ junctions formed by dual (Ga/B) ion implantation

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Ultrashallow p^+ junctions formed by dual implanation of Ga and B with low-temperature rapid thermal anneal (RTA) are reported. The electrical and structural properties of the shallow junction were studied by sheet resistance and diode reverse recovery measurements, Rutherford backscattering channeling, and secondary-ion mass spectrometry. A junction of 400 Å depth (full width at half maximum) and an average carrier concentration of 3×10^{19} cm^{-3} were realized with RTA at 600 °C. It is shown that there is excess damage in the dual-implanted junctions which affects the minority-carrier lifetime.

The formation of shallow junctions is essential in fabrication of scaled silicon devices that will be implemented in very large scale integrated circuits. The ability to improve speed, lower power dissipation, and increase integration level is the motivation for lateral and vertical scaling of device dimensions. The obstacle against formation of shallow junction is the diffusion of implanted atoms during the high-temperature step which is required for activation of dopants. Rapid thermal annealing (RTA) has proven useful in reducing impurity diffusion while achieving a high activation ratio. However, a serious problem that remains is the presence of tails in the dopant profile associated with ion channeling, especially for light ions such as boron.

Dual implantation has been shown to be useful in reducing channeling tails.[1–4] Recent works have shown that shallow p^+ junctions with sub 100 nm depth and low sheet resistance can be achieved by Ga (Ref. 3) and Sb (Ref. 4) preimplantation. In this work we have studied electrical and structural properties of B-doped p^+ shallow junctions formed with Ga preimplantation. Here, we demonstrate ultrashallow p^+ junctions, 400 Å full width at half maximum (FWHM), using this technique and study its majority- and minority-carrier properties using sheet resistance and diode reverse recovery, respectively. We have employed Rutherford backscattering (RBS) channeling measurements to study the effect of residual ion damage after RTA. The results are consistent with the diode reverse recovery measurements and indicate that the presence of additional damage due to Ga preimplantation degrades the minority-carrier lifetime of these junctions.

The junctions were formed by dual implantation of Ga and B in ⟨100⟩ silicon wafers. The implantation consisted of 10^{15} cm^{-2} of Ga ions at 100 keV followed by 10^{16} cm^{-2} of B ions at 5 keV. The implantation ranges of Ga and B were 693 and 198 Å calculated by the TRIM program.[5] A thermal oxide mask was used as implantation mask. Sheet resistance was measured using van de Pauw structures on n-type 4–6 Ω cm silicon wafers. Diode reverse recovery measurements were made on p/n^+ wafers where the contact to the p region was formed by either dual (Ga/B) or single (B) implantation followed by RTA in a H_2/N_2 ambient.

The formation of shallow p^+-n junctions with a low-temperature process was investigated using secondary-ion mass spectrometry (SIMS) and sheet resistance measurements. Figure 1 shows the SIMS depth profile of B for a sample preimplanted by Ga followed by B implantation with a subsequent rapid thermal anneal at 600 °C for 30 s. For comparison, the boron depth profile for a sample with single boron implantation and the same annealing condition is also shown. The Ga preimplantation impedes the B diffusion and completely eliminates the channeling tail. Therefore the junction depth is distinctly less than by single implantation. Figure 2 shows the sheet resistance measured on samples annealed at various temperatures. For the 600 °C case, the sheet resistance is 1300 Ω/□. This value can be used to obtain the average carrier concentration of the junction. Taking the hole mobility to be 50 $cm^2/V\,s$ (Ref. 6) and the junction depth to be 400 Å (FWHM), the estimated carrier

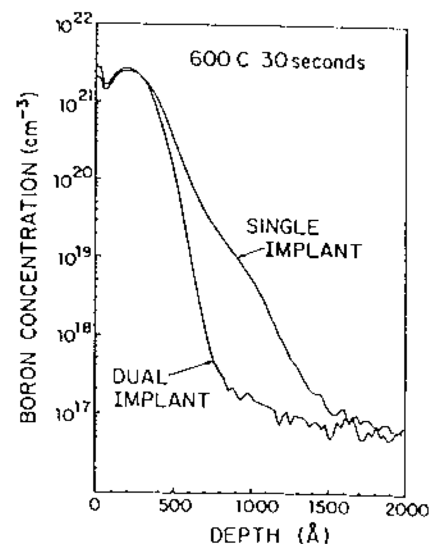

FIG. 1. SIMS depth profiles of B in B-implanted samples (10^{16} cm^{-2} at 5 keV) with and without Ga preimplantation (10^{15} cm^{-2} at 100 keV). Both samples were annealed at 600 °C for 30 s.

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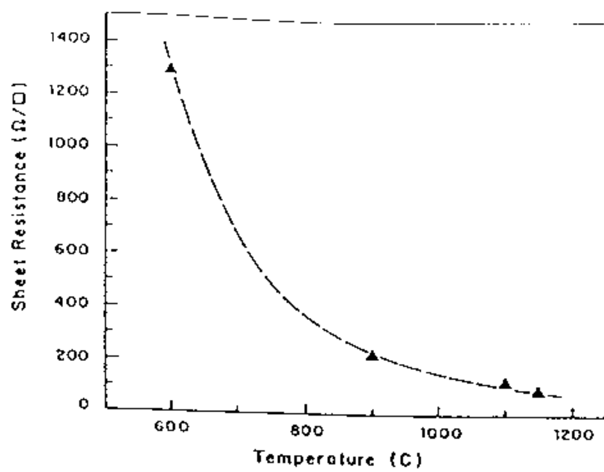

FIG. 2. Sheet resistance measurements on dual-implanted samples with RTA (30 s) at various temperatures.

concentration is 3×10^{19} cm^{-3}. Since the implanation dose of B is an order of magnitude greater than that of Ga, the carrier concentration is dominated by B acceptors. It is thus shown that a very low-temperature process can be employed to obtain a heavily shallow junction.

Figure 3 shows SIMS depth profiles of B and Ga with RTA at various temperatures. The depth of B peak in the as-implanted sample is about 200 Å which correlates well with a calculated value predicted by the TRIM simulation program. In the sample annealed at 600 °C, B diffusion is negligible. An active carrier concentration of 3×10^{19} cm^{-3} is realized with a junction depth determined by the as-implanted profile. The B diffusion depth for the 1100 °C sample is about 900 Å where an average carrier concentration of $\sim1\times10^{20}$ cm^{-3} is estimated from the sheet resistance of 150 Ω/□ (Fig. 2). For samples annealed at a higher temperature, an interesting feature of diffusion process can be seen. The abnormal diffusion behavior is a manifestation of the high B concentration. This is attributed to B atoms which are at a concentration above the solubility limit.[7] Thus from Fig. 3 solubility limit is of the order of 2×10^{20} cm^{-3} at 1100-1200 °C. For the case of a 600 °C anneal, although the abnormal diffusion profile is not seen, we speculate that the maximum active concentration is still limited by the solubility limits. It is also observed that Ga preimplantation is ineffective in reducing the B diffusion at high temperatures.

The minority-carrier characters of p^+ shallow junctions, when used as contacts are studied by diode reverse recovery measurements.[8] In this experiment p^+ junctions are used as contacts to p/n^+ diodes. Since the thickness of the p layers is much less than the electron diffusion length, the reverse storage time of the diode is determined by electron-hole recombination within the contact region. Thus the measurement of storage time can be used to study the recombination velocity of the p^+ junction region.

Figure 4 shows the storage time of diodes with and without Ga preimplantation. In general, the recombination velocity of the contact depends on the gradient of the junction profile, minority-carrier lifetime in the junction, and metal-semiconductor interface which is assumed to be the same with and without Ga preimplantation. From Fig. 1, since the preimplanted junction has a higher concentration gradient, we would expect it to have a larger storage time and thus lower recombination velocity. However, in Fig. 4 we observe the opposite which indicates that the dual-implanted junctions must have a lower minority-carrier lifetime compared to single implanted junctions. Therefore additional damage due to Ga preimplant must remain even after RTA. This is confirmed by RBS channeling measurements. Figure 5 shows channeling spectra for samples implanted with B and without Ga preimplantation. It can be seen that for 600 °C RTA, the dechanneling yield (χ_{min}) of a dual-implanted sample is ~1 compared with 0.82 for simple implanted one. For 1100 °C RTA, the dechanneling yield is much smaller which is also consistent with the storage time measurement (Fig. 4). In addition, we observe that after a high-temperature (1100 °C, 30 s) anneal, about 80% of Ga atoms have diffused out of the sample. As a result there is a higher substi-

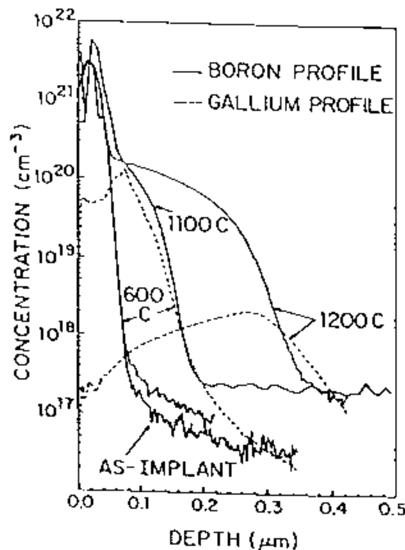

FIG. 3. SIMS depth profiles of B (solid lines) and Ga (dashed lines) for samples preimplanted with 10^{15} cm^{-2} Ga at 100 keV (30 s RTA).

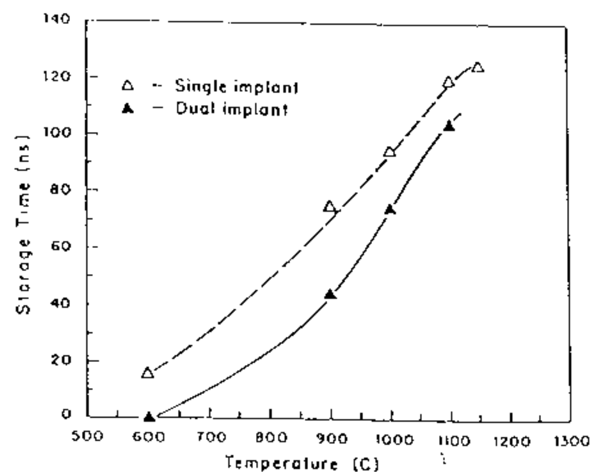

FIG. 4. Storage time for devices with (▲) and without (Δ) Ga preimplantation.

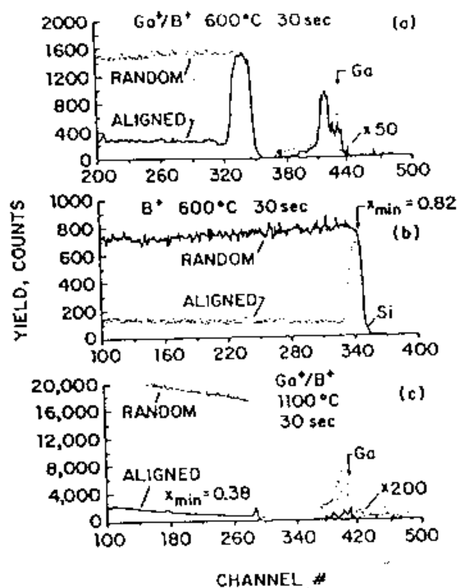

FIG. 5. RBS channeling spectra for samples (a) with and (b) without Ga preimplantation and annealed at 600 °C for 30 s, and (c) dual implanted and annealed at 1000 °C for 30 s.

tutional to interstitial ratio at 1100 °C compared to a 600 °C anneal. This is possible since interstitial atoms are more mobile than those in substitutional sites. This is contrary to the observation of single Ga implantation in silicon.[9,10]

In summary, we have studied the formation of ultrashallow junction by dual (Ga/B) implantation. A 400 Å (FWHM) shallow junction with a carrier concentration of 3×10^{19} cm^{-3} was obtained with a 600 °C rapid thermal anneal for 30 s. The maximum active concentration is limited by B solubility in silicon. Although the dual implantation technique can be used to form shallow junctions for majority devices, it has been shown here that the minority-carrier lifetime of these junctions can be shorter due to excess ion damage. This aspect should be taken into account in the fabrication of minority-carrier devices.

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