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Estimation of Electromigration-Aggravating Narrow Interconnects Using a Layout Sensitivity Model

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Abstract

During semiconductor manufacturing, particles undesirably depose on the surface of the wafer causing "open" and "short" defects to interconnects. In this paper, a third type of defects called "interconnect narrowing" defect is defined. Interconnect narrowing occurs when a defect intervenes the lithographic printing of interconnects causing the formation of a narrow interconnect. The narrow sites of defective interconnects favor electromigration that makes narrow interconnects more likely to induce a chip failure than regular interconnects. In this paper, a layout sensitivity model accounting for narrowing defects is derived. A methodology for predicting the probability of narrow interconnects using the sensitivity model is then proposed. The layout sensitivity model for narrow interconnects is tested and compared to actual and simulated data. Our layout sensitivity model for narrow interconnects predicts the probability of narrowing with 3.1% error, on average. The model is then combined with electromigration constraints to predict mean-time-to-failure of chips manufactured in future technology down to 32nm node. The paper concludes with some other possible applications of the narrow interconnect predictive model.

1. Introduction

Integrated circuits are very susceptible to particle deposition on the surface of the wafer during the manufacturing process. The deposition of a single particle with 0.5 to 0.33 of the minimum feature size can result in a defective die [1]. This fact and the abundance of particles in the air make the probability of producing defective dies considerably high. Moreover, tiny defects in the lithographic mask can also induce chip's failure. Consequently, the manufacturing yield, defined as the ratio of devices performing properly to the total number of devices, is significantly affected.

Semiconductor manufacturers have employed cleanliness techniques in order to reduce the probability of particle deposition, and consequently increase the fabrication yield. In particular, the manufacturing process is performed in clean rooms equipped with high efficiency particle air (HEPA) and ultra low penetration air (ULPA) filters. The filters are capable of eliminating almost every particle in the air larger than a few hundredth of a micron [2]. However particles of smaller size still float abundantly in the fabrication environment, and with the ever scaling down of the smallest IC feature size, such tiny particles can cause the production of faulty dies.

We define interconnect narrowing defect as a new type of defects that occurs when a defect intervenes the lithographic printing of interconnects causing the formation of a narrow interconnect as shown in Figure 1. Semiconductor yield enhancement faces non-stopping challenges as the number of transistors per die is exponentially growing and the minimum feature size in semiconductor fabrication is exponentially scaling down [3]. Formation of open and short defects caused by the intrusion of particles into the die surface during the fabrication

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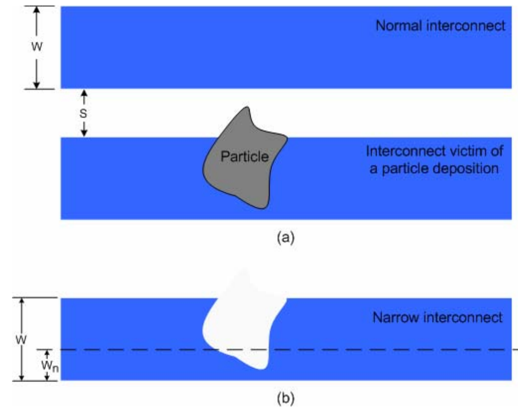

Figure 1. Example of particle deposition on wafer. (a) Particle deposition interfering with the formation of an interconnect. (b) A narrow interconnect

process represent the major challenge to yield enhancement. Thus, the yield can be directly determined from the layout sensitivity to defects. Layout sensitivity refers to the ratio of parts of the layout, where the intrusion of particles leads to short or open circuit defects, also known as "critical areas", to the overall layout area.

Semiconductor manufacturing yield is one of the most important factors affecting the fabrication cost. Therefore, yield forecasting is necessary in studying the economical feasibility since it gives a close approximation of the cost of new products.

Different layout sensitivity models were developed. In 1976, Stapper pioneered a model for critical area model [4]. Then, Christie and de Gyvez developed a model in [5] that predicts manufacturing defects using interconnect length distribution, defect size, and wire width. However, this model didn't show a good accuracy. More recently, Zarkesh-Ha and Doniger offered in [6] an accurate layout sensitivity model that makes use of basic layout information i.e. interconnect width and spacing, defect size, and interconnect density.

2. Effects of narrow interconnect on electromigration

Narrow interconnects represent a risk of chip failure in the field. Such interconnects are almost impossible to detect during IC testing by the manufacturer. This makes the effect of narrow interconnects even more severe. In this section, electromigration induced chip failure in narrow interconnects is analyzed.

2.1. Electromigration Aggravation

Electromigration (EM) is an interconnect failure mechanism that is considered as a foremost challenge for semiconductor manufacturing [7], [8]. EM is the mass movement of metal caused by the flow of electrons in conducting wires at high temperature [9], [10]. In particular, it is the transfer of momentum from electrons to thermally active metal atoms causing the transport of metal, away of its original site, in the direction of the electron flow [11].

Possible failures induced by EM are the formation of open circuit as a result of metal migration, and the formation of a short circuit in consequence of metal atoms exerting a pressure at a site and breaking the passivation layer [11].

Copper (Cu), instead of aluminum (Al), has been employed in semiconductor manufacturing for the interconnect material because Cu has a smaller resistivity and better opposition to

electromigration than Al [17], [18]. In Cu interconnect fabrication process, a barrier layer is deposited on the bottom and sidewalls of the interconnect while a dielectric film is added on top [7], [19]. The barrier layer is used to prevent Cu diffusion in the interconnect layer dielectric (ILD). Studies have shown that Cu interconnect are still vulnerable to EM [17], [20]. In particular, EM occurs at the interconnect top surface since it is not covered by the barrier layer [7]. However, as reported in [19], EM can also occur at the interface of Cu and barrier layer. It has been even reported in [21] that Cu interconnects, in some particular cases, demonstrate less lifetime than Al interconnects. Therefore, EM is expected to continue to be the primary reliability concern for interconnects and a leading challenge for IC reliability.

A typical metric used in the analysis of EM is the interconnect mean time to failure (MTTF). An empirical model describing MTTF caused by EM is derived by Black in [14] and, for MTTF of a single interconnect, Black's law is stated as follows [15]:

$$MTTF = A\frac{wt}{J_e^2}e^{E_a/kT} \tag{1}$$

where w and t are the interconnect width and thickness respectively, k is the Boltzmann's constant, T is the interconnect temperature, A is a constant embodying physical properties of the metal in use, J_e is the electron current density, E_a is the activation energy for EM failure. Replacing the current density J_e by $I/(w \times t)$, where I is the average current flowing in the interconnect and the term ($w \times t$) represents the area of the interconnect cross section, Black's law can be written as:

$$MTTF = A\frac{wt}{I^2/w^2t^2}e^{E_a/kT} = A\frac{t^3w^3}{I^2}e^{E_a/kT} \tag{2}$$

Equation (2) shows that for a narrow interconnect having width of w/K at its weakest point (narrowed region), where w is the width of the normal interconnect and K is defined as the narrowing factor, the MTTF is reduced by a factor of K^3. Figure 2 plots, for three different technology nodes, the MTTF of narrow interconnect as a function of the width of its narrow site. The plot shows that the impact of interconnect narrowing on MTTF becomes more severe as technology node scales down.

Another factor that aggravates EM in narrow interconnects is the rise of temperature at the narrowed region. Specifically, the narrowed site represents a region of high resistance compared to other parts of the structure, consequently, more energy dissipation is generated and

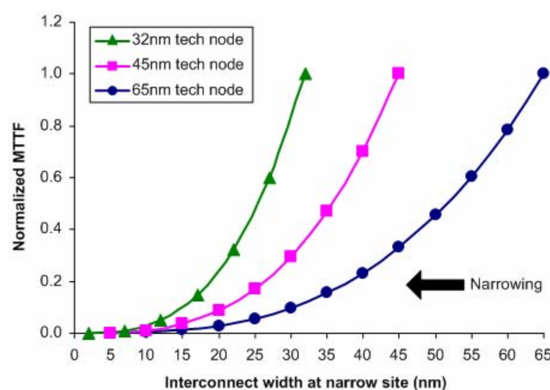

Figure 2. Plot of normalized MTTF vs. interconnect width at narrow site for 65nm, 45nm, and 32nm technology nodes.

higher temperature is observed at the narrow site. As shown in (2) the MTTF decreases exponentially by increasing temperature. Thus, the increase of temperature in the narrow region dramatically reduces the MTTF of the interconnect.

3. Predictive model for narrow interconnects

In this section, a stochastic model that predicts the number of narrow interconnects is derived. The new model is based on the layout sensitivity for open defects that accounts for narrow interconnects. The section starts by deriving the model for layout sensitivity and then a methodology for inferring the probability of narrow interconnects is proposed.

3.1. Layout sensitivity model accounting for narrows

Spot defects represent the main challenge for enhancement of manufacturing yield. Thus, researchers have developed layout sensitivity models for such defects in order to estimate the manufacturing yield. Moreover, pre-layout yield estimation is believed to be necessary for determining whether or not new products can meet their cost objectives [24].

Maly offered in [25] a model for predicting the critical area and consequently the manufacturing yield by considering narrow interconnects that have a width less than a predefined minimal width as open defects. However, he did not extended his model to predict narrow interconnects and his model lacks accuracy in predicting the probability of failure caused by spot defects. An attempt to estimate the probability for a single interconnect to become narrowed as a result of spot defects is offered in [26]. Yet, the suggested analysis is extremely complicated even when applied to a very simple structure [26] and becomes nearly impossible to apply to actual layout. The rareness of the models that accounts for narrowing defects in predicting the yield and the inefficiency of the ones that do account for this type of defect represented the primary motivation for developing a layout sensitivity model that considers narrowing defects in predicting the yield.

The layout sensitivity model for opens that involves narrow defects is given by (3) (shown at the bottom of the page), where w and s are the interconnect width and spacing respectively, and d is the channel density, r is the defect size, m is the minimum number of channels covered by a defect of size r, and w_n is the "critical width" i.e. a parameter that we define as the minimum acceptable width of interconnect at narrow sites, below which narrow interconnects are considered a failure.

The new model is based on layout sensitivity model developed in [6]. The main difference between the two models is that the new model uses a probabilistic approach in determining the number of channels covered by a defect; whereas in the old model a deterministic approach is used and a defect of specific size r is assumed to cover a fixed number of channels. The probabilistic approach of the new model allows us to include the narrowing defects in calculating the probability of failure for opens.

The critical width w_n specifies the smallest acceptable interconnect width in the layout. Any

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$$S_{open} = 1 - \left(\frac{2w + s + m(w+s) - r - 2w_n}{w+s} \times (1-d)^m + \frac{r - w - m(w+s) + 2w_n}{w+s} \times (1-d)^{m+1} \right) \quad (3)$$

$$m = m_1 + \left[\left\lfloor \frac{r - (w - w_n) - m_1(w+s)}{w + s - w_n} \right\rfloor > 0 \right], where\ m_1 = \left\lfloor \frac{r - (w - w_n)}{w+s} \right\rfloor \quad (4)$$

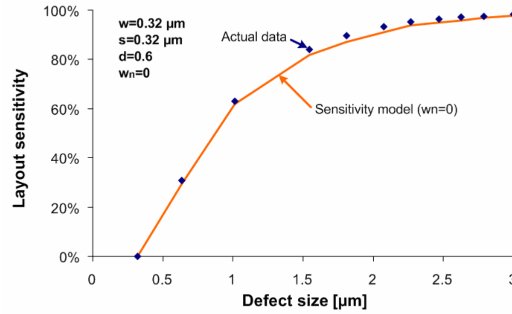

Figure 3. Comparison of model with actual extracted layout sensitivity for opens.

narrow interconnect that has a width smaller than w_n is considered as an open defect. This is needed to consider in the model only the narrowing defects that are likely to induce a failure.

3.2. Methodology for predicting narrows

The choice of the critical width in the model determines how much narrowing is acceptable before a failure occurs. For instance, a critical width of zero means that narrows are not considered as open defects and are excluded from the model. Therefore, the probability of narrow interconnect having the width between w_{n1} and w_{n2} can be obtained by subtracting the outcomes of the model when critical width is set to w_{n1} and w_{n2}, respectively.

4. Results and comparison with measured data

The sensitivity model was tested for 0.32µm technology node with an interconnect density of 0.6 and a critical width of 0 (i.e. without considering narrow interconnects). Figure 3 shows the result of testing and a comparison with the sensitivity extracted from an actual layout in [5]. The average percent error of the model's outcomes when compared to actual data was found to be 1.7%, which is an indication of the high fidelity of the model.

Because of the absence of layout analysis data for narrow interconnects in real design, the model is compared with results extracted from simulations. Testing of this model is performed using PRS, a placement and routing software previously developed in [27]. PRS is used to create the layout of a small circuit that computes the absolute value of the difference between two 2-bit numbers with a 45nm technology node. The generated layout is exhibited in Figure 4.

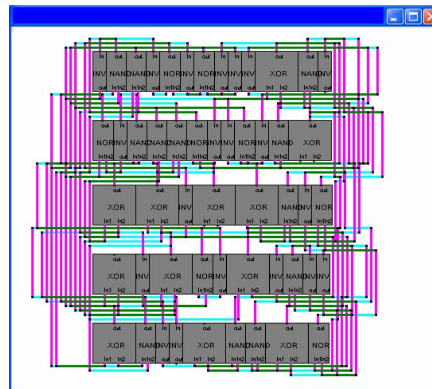

Figure 4. PRS displaying the layout of an actual circuit

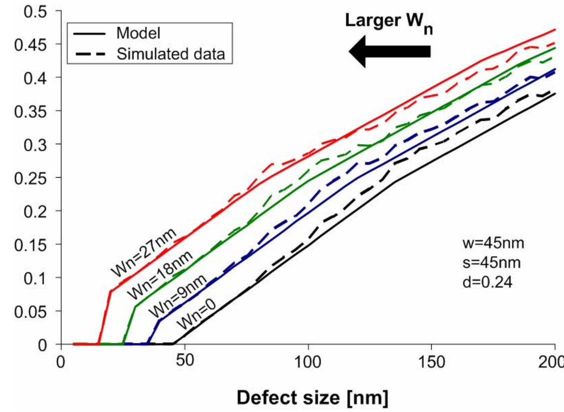

Figure 5. Comparison of modeled and simulated probabilities of failure due to open and narrow defects for different critical widths w_n.

We expanded PRS tool to generate defects and check for the resulting narrows and opens. A large number of defects with different sizes (20,000 defects per defect size) are placed randomly on the layout and the number of resulting narrows and opens for a single metal layer is determined for different critical widths w_n. The probability of failure associated with each defect size is then obtained by the ratio of the total number of resulting narrows or opens to the total number of generated defects for each defect size.

The channel densities and total area are then extracted from the layout and provided to the predictive model. Figure 5 presents a comparison between the simulated and predicted probabilities of failure for different defect sizes and different critical widths w_n. Results shows the accuracy of the model in predicting narrow and open defects and are summarized in Table I.

5. Application

5.1. Prediction of probability of failure caused by narrows

Studies have indicated that the size of spot defects follow a specific distribution. A well established defect size distribution is of the form [4]:

$$D(r) = \begin{cases} \dfrac{2(n-1)r}{(n+1)r_0^2} & 0 \le r \le r_0 \\ \dfrac{2(n-1)r_0^{n-1}}{(n+1)r^n} & r_0 \le r \le r_{\max} \end{cases} \tag{5}$$

Table I. Summary of percent errors of narrows predictive model when compared to simulated data for different values of critical width

critical widths w_n [nm]	Average percent error of model when compared to simulated data (%)
0	5.6
4.5	4.7
9	3.9
13.5	3.0
18	2.3
22.5	2.4
27	2.6

where r is the defect size, r_0 is the defect size with the peak density, r_{max} is the maximum possible defect size that is allowed by the cleanliness technique employed in the manufacturing process, and n is a parameter that depends on the cleanliness of typical fabrication line and is approximated to 3 [24], [4]. It is believed that r_0 is less than the minimum feature size [24].

The probability for a defect of specific size r to cause the formation of an open or narrow interconnect with a width less than some width w_n is determined using the sensitivity model described in the previous section. Consequently, the probability P_n for a defect of an unknown size to induce a narrow interconnect with a width less then w_n can be calculated as follows:

$$P_n(w < w_n) = \int_0^{r_{\max}} D(r) \cdot \left(S_n(w_n, r)\right) \cdot dr \qquad (6)$$

where $S_n(w_n , r)$ is the probability of the formation of an open or narrow interconnect having width less than w_n due to a spot defect.

$S_n(w_n , r)$ is a function of interconnect width w, spacing s, and density d as well as the critical width w_n and defect size r (See Equation (3)). Since w and s are predetermined by the manufacturing process and d is preset by the design of the layout, then $S_n(w_n , r)$ is only a function of w_n and r variables. According to (6), the probability of interconnect narrowing, P_n, is therefore only a function of w_n. Figure 6 illustrates the probability of narrowing, P_n, versus critical width, w_n, for different technology nodes. In this plot, interconnect width w and spacing s were chosen in accordance with International Technology Roadmap for Semiconductor (ITRS) [28], the defect size r_0, for which the defect size distribution peaks, is assumed to be 80% of the minimum feature size for each technology, manufacturing is assumed to be performed in a typical fabrication line with n=3, and the channel density d is assumed to be 0.675 considering a constant Rent's parameters for all technology nodes [29].

The narrow site represents the weakest point of a defective interconnect. Consequently, failure of a narrow interconnect will most probably occur at its narrow site. In this case, the interconnect time to failure is the time for the narrow site to fail, which can be calculated using Black's law by replacing w with w_n. If an interconnect MTTF less than a predefined threshold is considered as a failure, then the plots of Figure 6 can be transformed into plots of the probability of failure P_f versus the mean time to failure of a narrow site having a width of w_n, MTTF(w_n). Figure 7 shows plots of P_f as a function of MTTF(w_n) where a realistic current density exponent of 1.1 was used in Black's equation to find the MTTF associated with w_n.

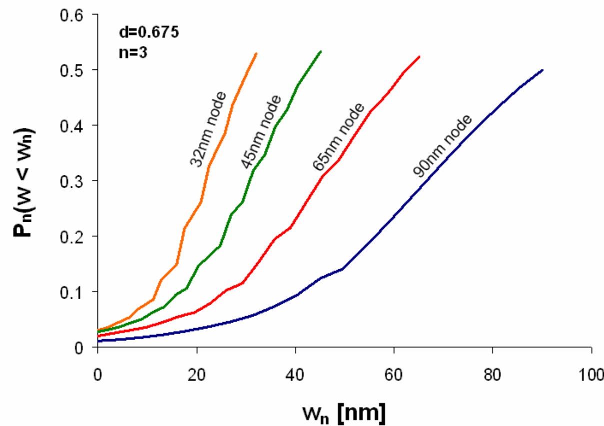

Figure 6. Plots of probability P_n of formation of an open or narrow as a function of the critical width w_n for 90nm, 65nm, 45nm, and 32nm technology nodes.

The plots of Figure 7 reveal the dramatic increase of the probability of failure due to narrowing defects as technology advances toward smaller lithographic nodes. For instance, the plots show that, for a MTTF threshold of 1 year, the probability of failure due to narrowing defect (which can be an open defect also) is 1.8%, 3.5%, 7%, and 22% for 90nm, 65nm, 45nm, and 32nm technology nodes, respectively.

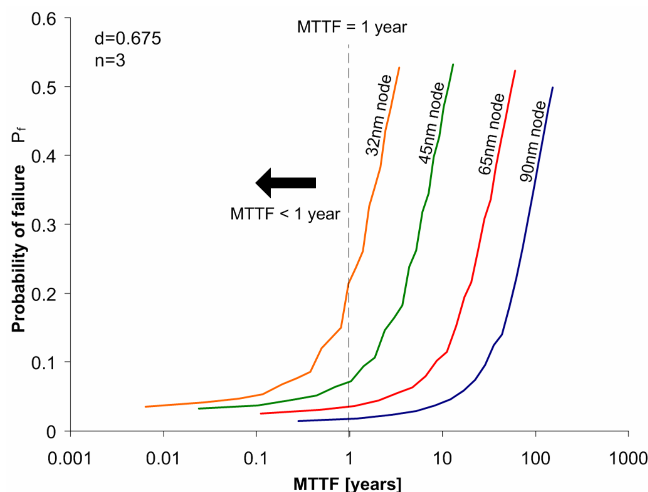

Figure 7. Plots of probabilities of failure P_f due to a narrowing defect versus interconnect MTTF for 90nm, 65nm, 45nm, and 32 nm technology nodes.

5.2. Enhancement of cost and reliability analyses

The predictive model of narrow interconnects can be employed in cost and reliability analyses of newly developed products. In particular, narrow interconnects can induce early chip's failure affecting the reliability as well as the cost of a product. Hence, accounting for narrows in the analyses of a product's reliability and determination of its cost results in more precise estimations. Moreover, a more trusted reliability analysis allows manufacturers to better approximate the warranty period to be offered for a particular product.

6. Conclusion

Narrow interconnects favor electromigration that may lead to interconnect open or short defects and consequently a chip failure. We expect narrowing defects to present a serious challenge for IC reliability with the ever decreasing feature size. Models that accounts for narrow interconnects in predicting the manufacturing yield are very rare and existing ones are ineffective. In this work, we proposed a very simple yet efficient methodology to predict the probability of narrow interconnects in any layout given some basic information such as interconnect width, spacing, and density. Subsequently, the probability of chip's failure due to narrowing defects can be inferred.

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