J Electron Test
DOI 10.1007/s10836-008-5079-x

A Layout Sensitivity Model for Estimating Electromigration-vulnerable Narrow Interconnects

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Received: 27 November 2007 / Accepted: 11 June 2008
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Abstract During back-end manufacturing process of IC, intervention of spot defects induces extra and missing material of interconnects causing circuit failures. Interconnect narrowing occurs when spot defects induce interconnects missing material without resulting in a complete cut. The narrow sites of defective interconnects favor electromigration that makes narrow interconnects more likely to induce a chip failure than regular interconnects. In this paper, an innovative layout sensitivity model accounting for "narrow" defects is derived. The paper also pioneers estimation of the probability of narrow interconnects in the die. The layout sensitivity model for narrow interconnects is tested and compared to actual and simulated data. Our layout sensitivity model predicts the probability of narrowing with 3.1% error, on average. The model is then combined with electromigration constraints to predict mean-time-to-failure of chips manufactured in future technologies down to 32 nm node. The paper concludes with some other possible applications of the narrow interconnect predictive model.

Keywords Yield modeling · Yield prediction · Electromigration · Layout sensitivity · Critical area · Spot defects · Narrow defects

Responsible Editors: C. Bolchini and Y.-B. Kim

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1 Introduction

Random particles are either particles floating in the air or particles originating from etching of material involved in many steps of the fabrication process. Failure to eliminate such particles from the surface of the wafer during the processing of each layer can generate circuit failure. Even the presence of a tiny random particle as small as 0.5 to 0.33 of the size of the minimum feature can be risky and result in a defective die [1]. As a result, manufacturing yield, which is the ratio of devices performing properly to the total number of devices, is significantly degraded.

Semiconductor manufacturers have employed cleanliness techniques in order to reduce the presence of random particles, and consequently, increase the manufacturing yield. Specifically, the manufacturing process is performed in clean rooms equipped with high efficiency particle air (HEPA) and ultra low penetration air (ULPA) filters. The filters are capable of eliminating almost every particle in the air larger than a few hundredth of a micron [2]. However airborne particles of smaller size and particles originating from the etching process are still abundant, and with the ever scaling down of the smallest IC feature size, such tiny particles can cause chip failure.

We define interconnect narrowing defect as a new type of spot defects that occurs when a defect intervenes the lithographic printing of interconnects causing missing material of interconnects without causing a complete cut of the interconnect. Also, we define the critical width, w_n, as the minimum acceptable width of interconnect at the narrow site. Therefore, only defects resulting in the formation of narrow sites having widths less than the critical width at their narrow sites will be considered as narrow defects. Interconnects victim of defect intervention are shown in Fig. 1. In Fig. 1b, the defect results in the formation of a

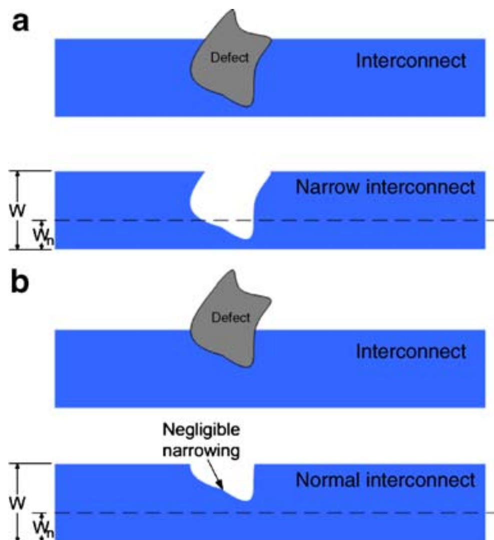


Fig. 1 Examples of a random defect causing: **a** Formation of a narrow interconnect, **b** formation of a negligible narrow site

narrow site with a width larger than the critical width, and consequently, the defect can be neglected. In Fig. 1a, a narrow site with a width smaller than the critical width is formed by the defect, and consequently, the defect is considered as a narrow defect and the victim interconnect is called a *narrow interconnect*. These narrow interconnects are vulnerable to electromigration (EM) failure mechanism and can cause a chip failure in the field.

Semiconductor yield enhancement faces non-stopping challenges as the number of transistors per die is exponentially growing and the minimum feature size of the manufacturing process is exponentially scaling down [3]. Yield loss caused by random particles, referred to as random yield loss, is significant. Random yield modeling is traditionally based on the analysis of the "critical areas" i.e. portions of the layout where a defect would cause a functional failure of the device [4]. In this paper, we focus on the stochastic method of critical area analysis that consists of the modeling of the layout sensitivity to defects defined as the ratio of critical areas to the overall layout area. The paper proposes a layout sensitivity model that includes the effects of the narrowing defect in the analysis and prediction of the manufacturing yield.

Section 2 explains different types of interconnect manufacturing defects and the concept of critical area. Section 3 gives an overview of the existing contributions to the stochastic method of yield modeling. Section 4 emphasizes on the effects of narrow defect on aggravating electromigration. The model predicting the layout sensitivity to narrow defects is derived in Section 5. In Section 6, the model is validated through testing and comparisons with simulated and actual data extracted from real layouts. Applications of the layout sensitivity model accounting for narrows are proposed in Section 7. Section 8 draws some conclusions.

2 Spot Defects and Critical Area

Device failure during the manufacturing process is the result of the formation of an open or a short circuit caused by a spot defect. An open defect occurs when a non-conducting defect disconnects a signal path as in Fig. 2c. This type of defect is typically difficult to diagnose during test procedures [5, 6] and is becoming more frequent in modern damascene processes [7]. A short defect occurs when a conducting defect connects two paths of different signals as in Fig. 2b. This type of defect occurs more often than the open defect [6].

The term, "critical area," was first introduced by Stapper in 1976 [4]. Since then, critical area has become a widely accepted measure of the sensitivity of VLSI design to random defects occurring during the manufacturing process.

Critical area consists of regions of the layout where the occurrence of a defect would cause functional failure. Examples of critical area for open and short defects are highlighted in Fig. 3. The highlighted regions in Fig. 3a show the area at which the placement of the center of a defect would cause a short failure. Similarly, the highlighted regions in Fig. 3b show the area at which the placement of the center of a defect would cause an open failure. The area of these highlighted regions is the critical area.

Critical area depends on the defect size. Larger defect size creates a larger critical area. For instance, the critical area of a very large defect can be the entire layout area if the placement of such defect anywhere on the layout causes a failure. Obviously, the larger the critical area (highlighted regions in Fig. 3), the more sensitive the layout becomes to defects.

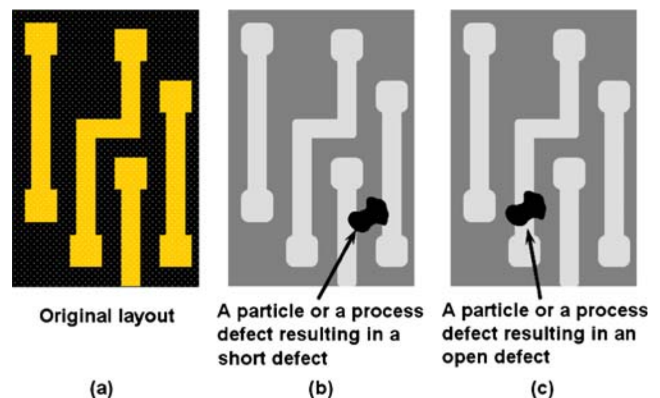


Fig. 2 Examples of **b** a short defect and **c** an open defect in **a** a sample layout

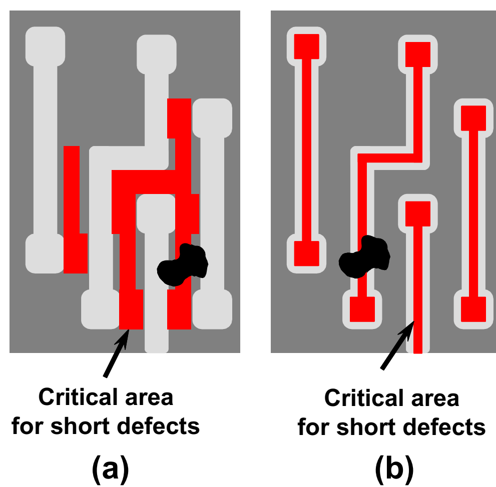


Fig. 3 Critical area for **a** short defects and **b** open defects

3 Stochastic Method of Yield Modeling

Semiconductor manufacturing yield is a major factor affecting the fabrication cost. Most models rely on extraction or analysis of the critical area. The application of critical area analysis on yield modeling is explained in [8–12]. On the other hand, the *stochastic method* of yield modeling is performed by modeling and prediction of critical area.

The stochastic method is not as accurate as other yield modeling approaches involving critical area analysis; however, it has very important advantages. In particular, the simplicity of this method in determination of the yield is one important advantage that expedites the yield computation process. An even more important advantage of this method is that the manufacturing yield can be forecasted at a very early stage of the design phase (Ghaida et al., Yield prediction based on a stochastic layout sensitivity model, unpublished). Yield forecasting is necessary in studying the economical feasibility of new products, and therefore, it can be used to determine whether or not a design would meet its cost objectives.

Not many contributions to the stochastic approach of yield modeling exist. In 1983–1984, Stapper pioneered a model for estimating the critical area [13, 14]. Then, Christie and de Gyvez developed a model in [15] that predicts manufacturing defects using interconnect length distribution, defect size, and wire width. However, these two models have poor accuracy when compared to actual data. A layout sensitivity model with a better accuracy was developed recently by Zarkesh-Ha and Doniger in [16]. It uses basic layout information i.e. interconnect width and spacing, defect size, and interconnect density. Figure 4 shows a comparison between the new and previous models.

4 Effects of Narrow Interconnect on Electromigration

Narrow interconnects represent a risk of chip failure in the field. Such interconnects are almost impossible to detect during IC testing by the manufacturer. This makes the effect of narrow interconnects even more severe. In this section, electromigration-induced chip failure in narrow interconnects is analyzed.

4.1 Electromigration Aggravation

Electromigration (EM) is an interconnect failure mechanism that is considered as a foremost challenge for semiconductor manufacturing [17, 18]. EM is the mass movement of metal caused by the flow of electrons in conducting wires at high temperature [19, 20]. In particular, it is the transfer of momentum from electrons to thermally active metal atoms causing the transport of metal, away of its original site, in the direction of the electron flow [6].

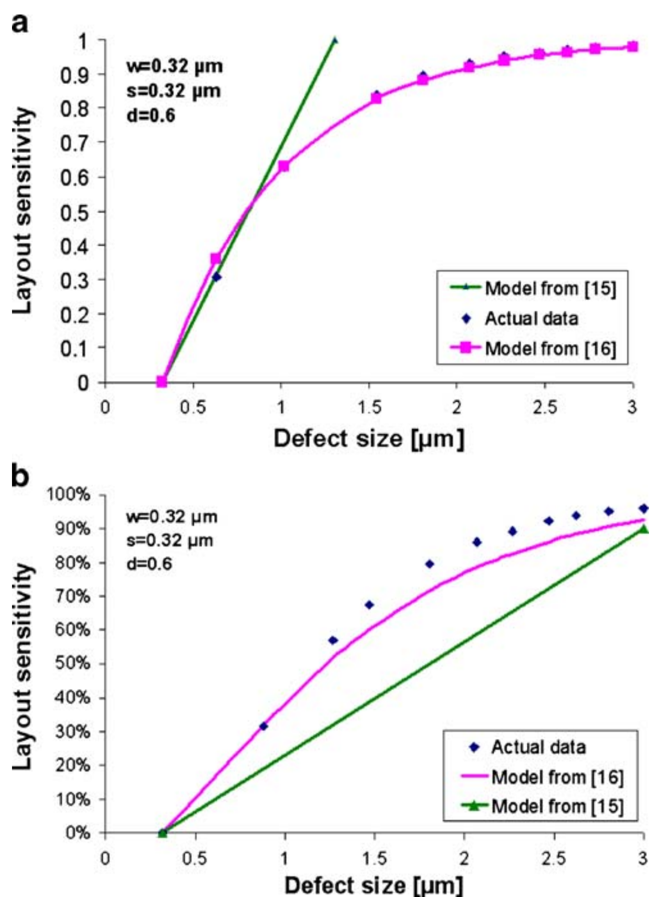
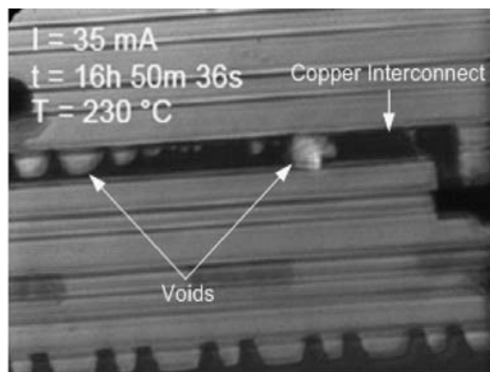


Fig. 4 Comparison between layout sensitivity using Zarkesh-Ha's model [16] and Christie's model [15], where w and s are the interconnect width and spacing, respectively, and d is the channel density. **a** For open defects. **b** For short defects

Possible failures induced by EM are the formation of open circuit as a result of metal migration as in Fig. 5a, and the formation of a short circuit in consequence of metal atoms exerting a pressure at a site and breaking the passivation layer [6] as shown in Fig. 5b.

Copper (Cu), instead of aluminum (Al), has been employed in semiconductor manufacturing for the interconnect material because Cu has a smaller resistivity and better opposition to electromigration than Al [21, 22]. In Cu interconnect fabrication process, a barrier layer is deposited on the bottom and sidewalls of the interconnect while a dielectric film is added on top [18, 23]. The barrier layer is used to prevent Cu diffusion in the interconnect layer dielectric (ILD). Studies have shown that Cu interconnect are still vulnerable to EM [21, 24]. In particular, EM occurs at the interconnect top surface since it is not covered by the barrier layer [18]. However, as reported in [23], EM can also occur at the interface of Cu and barrier layer. It has been even reported in [25] that Cu interconnects, in some particular cases, demonstrate less lifetime than Al interconnects. Therefore, EM is expected to continue to be the primary reliability concern for interconnects and a leading challenge for IC reliability.



(a)

(b)

Fig. 5 Examples of EM induced failure. **a** Open circuit resulting from formation of voids due to EM in a line interconnect [34]. **b** Extrusion of metal through the passivation layer [35]

A typical metric used in the analysis of EM is the interconnect mean time to failure (MTTF). An empirical model describing MTTF caused by EM is derived by Black in [26], and for MTTF of a single interconnect, Black's law is stated as follows [27]:

$$\mathrm{MTTF} = A\frac{wt}{J_{\mathrm{e}}^{2}}e^{E_{\mathrm{a}}/kT} \tag{1}$$

where w and t are the interconnect width and thickness, respectively, k is the Boltzmann's constant, T is the interconnect temperature, A is a constant embodying physical properties of the metal in use, J_{e} is the electron current density, E_{a} is the activation energy for EM failure. Replacing the current density J_{e} by $I/w \times t$, where I is the average current flowing in the interconnect and the term $(w{\times}t)$ represents the area of the interconnect cross section, Black's law can be written as:

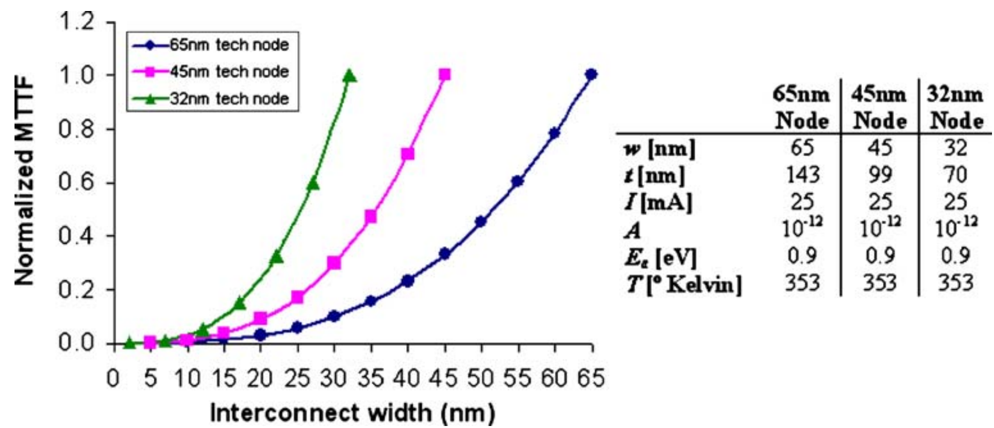
$$\mathrm{MTTF} = A\frac{wt}{I^{2}/w^{2}t^{2}}e^{E_{\mathrm{a}}/kT} = A\frac{t^{3}w^{3}}{I^{2}}e^{E_{\mathrm{a}}/kT} \tag{2}$$

Equation 2 shows that for a narrow interconnect having width of w/K at its weakest point (narrowed region), where w is the width of the normal interconnect and K is defined as the narrowing factor, the MTTF is reduced by a factor of K^{3}. In practical, the coefficient of J_{e} is not exactly 2 as in Black's original equation, but, it varies between 1 and 2 [18, 28]. Therefore, the MTTF in this case is reduced by a factor between K^{2} and K^{3}. Using Eq. 2, the MTTF of narrow interconnect as a function of the width of its narrow site is depicted in Fig. 6 for three different technology nodes. Technology parameters used for these plots are summarized in the table of Fig. 6. The plot shows that the impact of interconnect narrowing on MTTF becomes more severe as technology node scales down.

Another factor that aggravates EM in narrow interconnects is the rise of temperature at the narrowed region. Specifically, the narrowed site represents a region of high resistance compared to other parts of the structure; consequently, more energy dissipation is generated and higher temperature is observed at the narrow site. As shown in Eq. 2 the MTTF decreases exponentially by increasing temperature. Thus, the increase of temperature in the narrow region dramatically reduces the MTTF of the interconnect.

5 Predictive Model for Narrow Interconnects

In this section, a stochastic layout sensitivity model for narrow defects is derived. The model is based on the layout sensitivity to open defects offered in [16]. The section starts by deriving the model for layout sensitivity and then a



	65nm Node	45nm Node	32nm Node
w [nm]	65	45	32
t [nm]	143	99	70
I [mA]	25	25	25
A	10^{-12}	10^{-12}	10^{-12}
E_a [eV]	0.9	0.9	0.9
T [° Kelvin]	353	353	353

Fig. 6 Plot of normalized MTTF vs. interconnect width at narrow site for 65, 45, and 32 nm technology nodes and table summarizing technology parameters

methodology for inferring the probability of narrow interconnects is proposed.

5.1 Layout Sensitivity Model Accounting for Narrows

Spot defects represent the main challenge for enhancement of manufacturing yield. Thus, researchers have developed layout sensitivity models for such defects in order to estimate the manufacturing yield. Moreover, pre-layout yield estimation is believed to be necessary for determining whether or not new products can meet their cost objectives [29].

Maly offered in [30] a model for predicting the critical area and consequently the manufacturing yield by considering narrow interconnects that have a width less than a predefined minimal width as open defects. However, his model is not extended to predict narrow interconnects and lacks accuracy in predicting the probability of failure caused by spot defects. An attempt to estimate the probability for a single interconnect to become narrowed as a result of spot defects is offered in [31]. Yet, the suggested analysis is extremely complicated even when applied to a very simple structure [31] and becomes nearly impossible to apply to actual layouts. The rareness of the models that accounts for narrowing defects in predicting the yield and the inefficiency of the ones that do account for this type of defect represented the primary motivation for developing a layout sensitivity model that considers narrowing defects in predicting the yield.

The layout sensitivity model for opens that involves narrow defects is given by Eq. 3 (shown at the bottom of the page), where w and s are the interconnect width and spacing, respectively, and d

$$S_n = 1 - \left(\frac{2w + s + m(w+s) - r - 2w_n}{w+s} \times (1-d)^m + \frac{r - w - m(w+s) + 2w_n}{w+s} \times (1-d)^{m+1} \right) \tag{3}$$

$$m = m_1 + \left[\left\lfloor \frac{r-(w-w_n)-m_1(w+s)}{w-w_n+s} \right\rfloor > 0 \right], \text{ where } m_1 = \left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor \tag{4}$$

is the channel density, r is the defect size, m is the minimum number of channels covered by a defect of size r, and w_n is the "critical width," which is the minimum acceptable width of interconnect at narrow sites, below which the narrow site is considered as a narrow defect. The complete derivation of layout sensitivity model 3 for narrow defects is presented in Appendix A.

The new model is based on layout sensitivity model developed in [16]. The main difference between the two models is that the new one uses a probabilistic approach in determining the number of channels covered by a defect; whereas in the old model a deterministic approach is used and a defect of specific size r is assumed to cover a fixed number of channels. The probabilistic approach of the new model allows us to include the narrowing defects in calculating the probability of failure for opens.

The critical width, w_n, specifies the smallest acceptable interconnect width in the layout. Any narrow site that has a width smaller than w_n is considered as a narrow defect. This parameter is needed to limit the narrowing defects considered in the model to narrows that most likely have a short time to failure.

5.2 Methodology for Predicting Narrows

The sensitivity model determines the probability of having an interconnect with a width less than the critical width. In other words, the model includes open as well as narrow

defects. The value of the critical area specified by the manufacturer determines the narrows to include in the model. For instance, setting of the critical width to zero leads to the exclusion of narrow defect from the model and reduce its outcome to the layout sensitivity to opens. Therefore, the probability of having a narrow interconnect with width less than a specific critical width w_n^* is equal to the outcome of the model when the critical width is set to w_n^* minus the outcome of the model when the critical width is set to zero. In the general case, the probability of narrow interconnect having the width between w_{n1} and w_{n2} can be obtained by subtracting the outcomes of the model when critical width is set to w_{n2} and when critical width is set to w_{n1}.

6 Results and Comparison with Measured Data

The sensitivity model was tested for 0.32 μm technology node with an interconnect density of 0.6 and a critical width of 0 (i.e. excluding narrow defects). Figure 7 shows the result of testing and a comparison with the sensitivity extracted from an actual layout in [15].

The percent error of the model's outcomes when compared to actual data was calculated. The average percent error was found to be 1.7%, which is an indication of the high fidelity of the model.

Because of the absence of layout analysis data for narrow interconnects in real design, the model was compared with results extracted from simulations. The testing of the model is performed using PRS, a placement and routing software previously developed in [32]. PRS is used to create the layout of a small circuit that computes the absolute value of the difference between two 2-bit numbers using a 45 nm technology node. The generated layout is exhibited in Fig. 8. We expanded PRS tool to generate defects and check for the resulting narrows and opens.

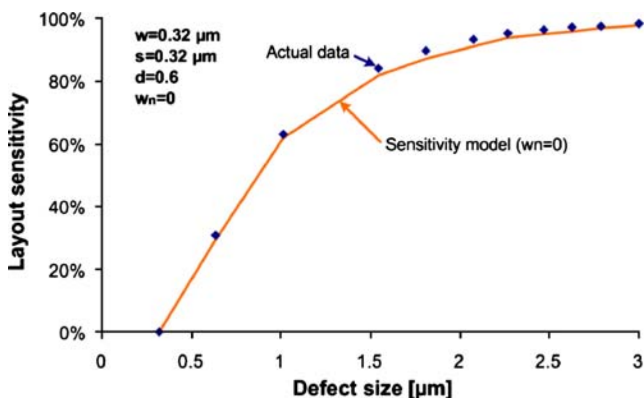


Fig. 7 Comparison of sensitivity model with actual extracted layout sensitivity for open defects

Fig. 8 PRS displaying the layout of a circuit that computes the absolute value of the difference between two 2-bit numbers

A large number of defects with different sizes (20,000 defects per defect size) are placed randomly on the layout. The number of defects is made large enough to avoid any dependence of the results on the number of samples. The number of resulting narrows and opens for a single metal layer is then computed for different critical widths w_n. The probability of failure associated with each defect size is obtained by the ratio of the total number of defects resulting in narrows or opens to the total number of generated defects for each defect size.

The channel densities and total area are then extracted from the layout and provided to the model. Figure 9 presents a comparison between the simulated and predicted probabilities of failure for different defect sizes and different critical widths, w_n. Results show the accuracy of

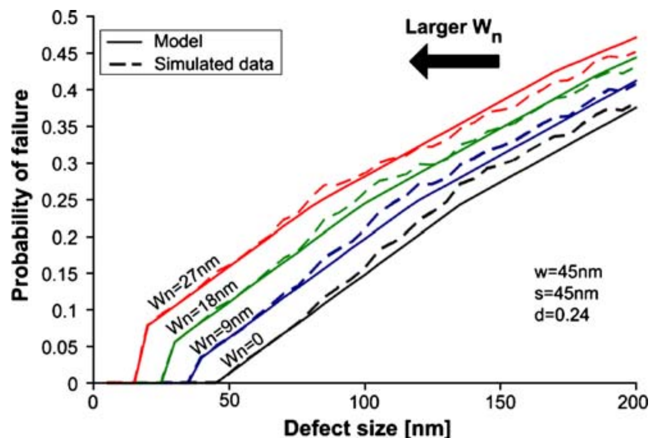


Fig. 9 Comparison of modeled and simulated probabilities of failure due to open and narrow defects for different critical widths w_n

the model in predicting narrow and open defects and are summarized in Table 1.

Figure 9 shows that there is a steep increase of the probability of failure from 0, for a defect size equal to $(w-w_n)$, to a non-zero value for a defect size slightly larger than $(w-w_n)$. This is because there is no possibility for the defect to create a failure if its size is less than or equal to $(w-w_n)$. This steep increase of the probability of failure becomes more noticeable for larger values of w_n. This is illustrated in Fig. 10. In this figure, the shaded regions represent the locations where the center of the defect must fall to create a narrow interconnect. In the case of a large w_n, as in Fig. 10b, there are more possible locations for the defect to occupy in order to create a narrow than in the case of a small w_n, as in Fig. 10a. Another observation in Fig. 10 is that the minimum defect size that can create a narrow is larger for a smaller w_n. This is in accordance with the plots of Fig. 9.

7 Application

In this section, some applications of the predictive model of narrowing defects are examined.

7.1 Prediction of Probability of Failure Caused by Narrows for Future Technologies

Studies have indicated that the size of spot defects follow a specific distribution. A well established defect size distribution is of the form [13]:

$$f_s(r) = \begin{cases} \frac{2(n-1)r}{(n+1)r_0^2} & 0 \leq r \leq r_0 \\ \frac{2(n-1)r_0^{n-1}}{(n+1)r^n} & r \geq r_0 \end{cases} \tag{5}$$

where r is the defect size, r_0 is the defect size with the peak density, and n is a parameter that depends on the cleanliness of the fabrication line. n is approximated to 3 in typical fabrication lines [13, 29]. It is believed that r_0 is less than the minimum feature size [29]. Figure 11 is a plot of Eq. 5

Table 1 Summary of percent errors of narrows predictive model when compared to simulated data for different values of critical width

critical widths w_n (nm)	Average percent error of model when compared to simulated data (%)
0	5.6
4.5	4.7
9	3.9
13.5	3.0
18	2.3
22.5	2.4
27	2.6

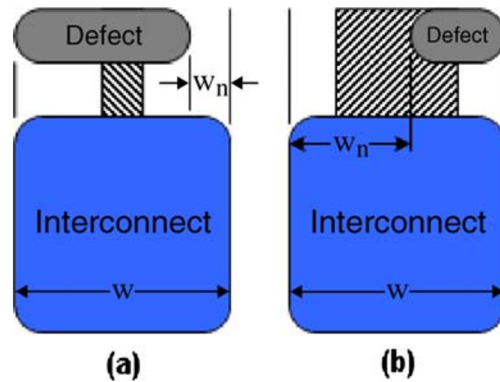


Fig. 10 Possible locations (shaded regions) the defect can occupy to create a narrow for **a** small w_n, and **b** large w_n

for 90, 68, 45, 32, and 22 nm technology nodes in a typical fabrication line, i.e. $n=3$, and where r_0 are chosen in accordance with the International Technology Roadmap for Semiconductor (ITRS) [3].

The probability for a defect of specific size r to cause the formation of an open or narrow interconnect with a width less than some width w_n is determined using the sensitivity model described in the previous section. Consequently, the average probability P_n for a defect of any size to induce a narrow interconnect with a width less then w_n can be calculated as follows:

$$P_n(w < w_n) = \int_0^\infty f_s(r) \times (S_n(w_n, r) - S_n(w_n = 0, r))dr \tag{6}$$

where $S_n(w_n, r)$ is the probability of the formation of an open or narrow interconnect having width less than w_n and is given by Eq. 3.

$S_n(w_n, r)$ is a function of interconnect width w, spacing s, and density d as well as the critical width w_n and defect size r (See Eq. 3). Since w and s are predetermined by the manufacturing process and d is preset by the design of the

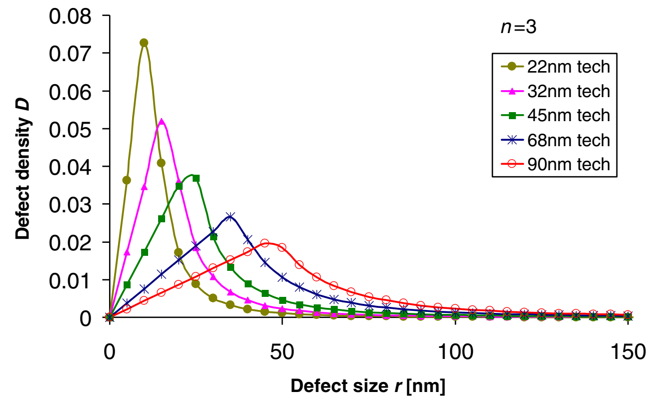


Fig. 11 Defect size distribution for 90, 68, 45, 32, and 22 nm technology nodes in a typical fabrication line

layout, then $S_n(w_n, r)$ is only a function of w_n and r variables. According to Eq. 6, the probability of interconnect narrowing, P_n, is therefore only a function of w_n.

Figure 12 illustrates the probability of narrowing, P_n, versus critical width, w_n, for different technology nodes. In this plot, the interconnect width w and spacing s as well as the critical defect size r_0, for which the defect size distribution peaks, were chosen in accordance with ITRS [3]. Manufacturing is assumed to be performed in a typical fabrication line with n=3, and the channel density d is assumed to be 0.675 considering constant Rent's parameters for all technology nodes [33].

The narrow site represents the weakest points of a defective interconnect. Consequently, failure of a narrow interconnect will most probably occurs at its narrow site. In this case, the interconnect time to failure is the time for the narrow site to fail, which can be calculated using Black's law by replacing w with w_n. If an interconnect MTTF less than a predefined threshold is considered as a failure, then the plots of Fig. 12 can be transformed into plots of the probability of failure P_f as a function of the mean time to failure of a narrow site having a width of w_n, MTTF(w_n). Figure 13 shows the plots of P_f as a function of MTTF where a realistic current density exponent of 1.1 was used in Black's equation to find the MTTF associated with w_n.

The plots of Fig. 13 reveal the dramatic increase of the probability of failure due to narrowing defects as technology advances toward smaller lithographic nodes. For instance, the plots show that, for a MTTF threshold of 1 year, the probability of failure due to narrow defects (excluding open defect) is 0.9%, 1.5%, 4.5%, and 18.5% for 90, 65, 45, and 32 nm technology nodes, respectively. Note the exponential increase of the probability of failure due to narrows as technology scales down. This is an indication that the considering narrow defects in yield analysis would be a must for future technology nodes.

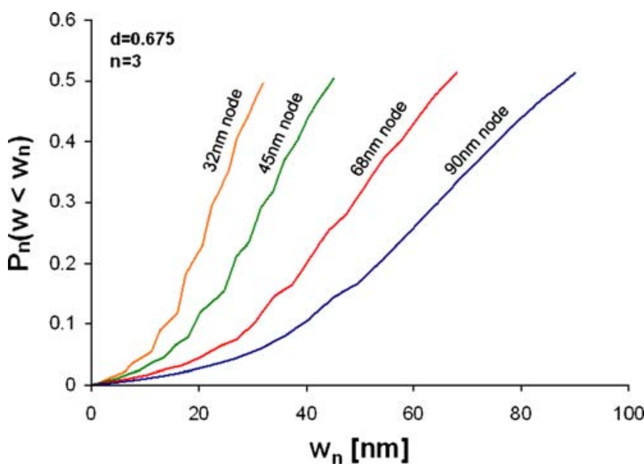


Fig. 12 Plots of probability P_n of formation of an open or narrow as a function of the critical width w_n for 90, 68, 45, and 32 nm technology nodes

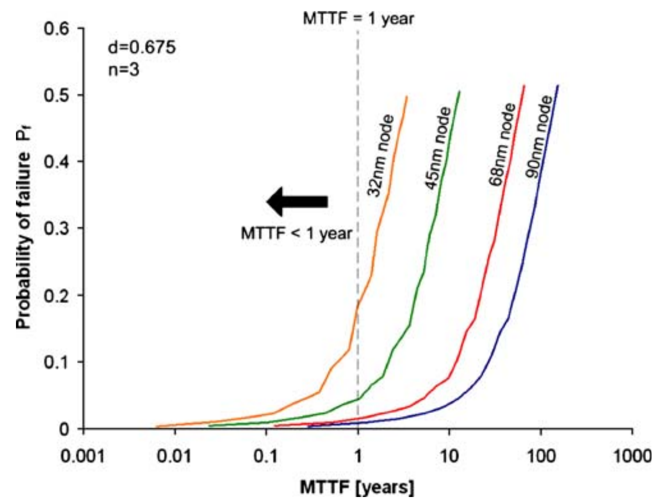


Fig. 13 Plots of probabilities of failure P_f due to a narrowing defect versus interconnect MTTF for 90, 68, 45, and 32 nm technology nodes

7.2 Enhancement of Cost and Reliability Analyses

The predictive model of narrow interconnects can be employed in cost and reliability analyses of newly developed products. In particular, narrow interconnects can induce early chip failure affecting the reliability as well as the cost of a product. Hence, more precise reliability and cost estimations can be obtained by including the effects of narrows in the analyses of these measures. Moreover, a more trusted reliability analysis allows manufacturers to better approximate the warranty period to be offered for a particular product.

8 Conclusion

This paper presents a model for "narrow defects", which is a new type of failure mechanism in advanced semiconductor manufacturing. We define "narrow defects" as non-catastrophic missing material spot defects causing the formation of a narrow site at the victim interconnects. Narrow interconnects victim of such a defect favor electromigration that may lead to interconnect open and short defects, and consequently, a chip failure. The induced failure may occur during the different stages of manufacturing and affect the yield, but also, the failure may occur in the field and affect the product's reliability. We expect narrowing defects to present a serious challenge for IC reliability with the ever decreasing feature size. Models that

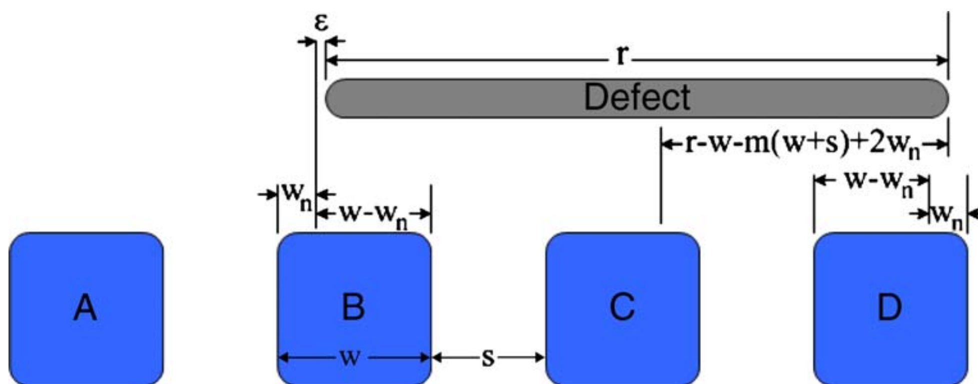


Fig. 14 Example of a defect at a location covering the minimum number of channel m. In this case, the defect covers channels C and D, and therefore, m is equal to 2

account for narrow interconnects in predicting the manufacturing yield are very rare and existing ones are ineffective. Moreover, no silicon data is currently available to verify any model against.

In this paper, we proposed a very simple yet efficient methodology to predict the probability of narrow interconnects in any layout given some basic information such as interconnect width, spacing, and density. Subsequently, the probability of chip failure due to narrowing defects can be inferred and narrows can be considered in modeling of semiconductor manufacturing yield and reliability analysis. Based on the simulation results using our model, it is apparent that narrowing defects will become a significant issue for 32 nm technology node and beyond.

Acknowledgments The authors would like to acknowledge the fruitful discussions with Chuck Hawkins at University of New Mexico and Edward Cole of Sandia Research Labs.

Appendix A. Complete derivation of layout sensitivity model for narrow defects

In this appendix, we present a thorough derivation of the layout sensitivity model for narrow defects. The model is based on the layout sensitivity presented in [16].

Some assumptions are made in order to simplify the derivation of the model. First, we assume that interconnect routing is performed using a grid based approach. The layout grid consists of channels that can be either empty or occupied by interconnects. We also assume that the routing of different interconnects are independent of each other. These assumptions are made without loss of generality of the model since the same assumptions are also made in most yield analysis tools to perform critical area studies.

We define channel density, d, as the probability of a random channel to be filled. Therefore, the probability of a random channel to be empty is given by $(1-d)$. Channel density, d, can be deduced from the metal density, D, using the following expression:

$$D = d\frac{w}{w+s}, \tag{7}$$

where w and s are the interconnect width and spacing, respectively.

It is important to note that a defect of a specific size r does not always cover the same number of channels. In fact, the number of channels covered by a defect depends on the size of the defect as well as its location. Therefore, to determine the probability for a defect of size r to cause an open defect, we need to find out the possible number of channels that can be covered and the chances for each case to occur. This is achieved by moving the defect a distance of $(w+s)$ away from its original location, with steps equal to the smallest unit of distance, while checking the number of covered channels for every different location. The probability for the defect to cover a certain number of channels, N, is the ratio of all locations at which the defect covers N channels to the distance $(w+s)$[1] i.e. the total number of possible locations of the defect.

Let m be the minimum number of channels covered by the defect. It is recommended to refer to Fig. 14 for a better understanding of the derivation of the model. The defect covers a minimum number of channels when its leftmost (rightmost) edge coincides with the right (left) edge of the interconnect with the minimum width, w_n, units of distance to the right (left) of the left (right) edge of a particular channel. At this point, the partially covered channel (channel B in example of Fig. 14) is not considered as a cut channel and will be referred to as the first channel. A part of the defect with distance $(w-w_n)$ is needed to cover the first channel and the remaining part of distance $(r-(w-w_n))$ is

[1] If the particle is moved furthermore, then the same positioning with respect to the channels would be repeated. Thus, moving the particle up to a distance of $(w+s)$ would include all possible locations that a particle can have.

to cover the minimum number of channels m (refer to Fig. 14).

The last channel (channel D in the example of Fig. 14) needs a distance of $(w - w_n + s)$ to be covered. Other channels i.e. excluding first and last channels that we call m_1, need a distance of $(w+s)$ to be covered by the defect and cause a channel cut. The number of channels m_1 that can be covered by the width $(r-(w-w_n))$ of the defect is determined as follows:

$$m_1 = \left\lfloor \frac{r - (w - w_n)}{w + s} \right\rfloor. \tag{8}$$

For the remaining part of the defect that neither covers one of the m1 channels nor covers the first channel, which is equal to $r - (w - w_n) - m_1(w + s)$, we check if it cuts an additional channel (the last channel). The additional channel is considered as cut if the defect covers more than $(w-w_n)$ of its total width. Therefore, m can be written as follows:

$$\begin{aligned} m &= m_1 + \left[\left\lfloor \frac{r-(w-w_n)-m_1(w+s)}{w-w_n+s} \right\rfloor > 0 \right] \\ &= \left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor + \left[\left\lfloor \frac{r-(w-w_n)-\left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor (w+s)}{w-w_n+s} \right\rfloor > 0 \right] \end{aligned}, \tag{9}$$

where $[x]$ is Iverson's convention that evaluates to 1 if x is true, and 0 if x is false.

Now, we start moving the defect toward cutting the first channel with steps equal to the smallest unit of distance. We assume that the movement is always made to the left to simplify the explanation. At this stage, $(m+1)$ channels are cut, i.e. the first channel as well as all other channels that were considered in the minimum number m of channels. $(m+1)$ channels remains cut for a distance of $r - (w - w_n) - (w + s - w_n) - (m - 1)(w + s)$, i.e. width of defect minus width of defect to cover first channel minus width of defect needed to cover the last channel minus width of defect needed to cover all other channels ($m-1$ channels) as depicted by Fig. 14. This distance can be expressed by $r - w - m(w + s) + 2w_n$.

After the defect is moved $r - w - m(w + s) + 2w_n$, the last channel that was considered in the m channels will be uncovered instantly. There will be m cut channels until the left (right) edge of the defect coincides with the right (left) edge of the interconnect with the minimum width i.e. w_n units of distance to the right (left) of the left (right) edge of the channel neighboring the first channel to its left (right). The defect would have moved for $(w + s) - (r - w - m(w + s) + 2w_n)$, which evaluates to $2w + s + m(w + s) - r - 2w_n$.

Thus, the defect either covers m channels with a probability of

$$\frac{2w + s + m(w + s) - r - 2w_n}{w + s}, \tag{10}$$

or $(m+1)$ channels with a probability of

$$\frac{r - w - m(w + s) + 2w_n}{w + s} \tag{11}$$

The probability for the chip to overcome a defect that covers N channels is the probability for the N consecutive channels to be empty, which is $(1-d)^N$. Therefore, in the general case, the probability for the chip to overcome a defect of size r, i.e., the probability of survival, referred to as P_s, is the product of the probability of a defect to cover a number N of channels by $(1-d)^N$ summed up for all possible number of channels that the defect can cover. Since the defect can either cover m channels or $(m+1)$ channels as demonstrated earlier, then P_{NF} is computed as in Eq. 12 (shown at the bottom of the page).

The layout sensitivity S_n is defined to be the probability of chip failure P_F. Thus, the layout

$$\begin{aligned} P_s = &\frac{2w + s + m(w + s) - r - 2w_n}{w + s} \\ &\times (1 - d)^m + \frac{r - w - m(w + s) + 2w_n}{w + s} \\ &\times (1 - d)^{m+1} \end{aligned} \tag{12}$$

sensitivity is modeled as in Eq. 13 (shown at the bottom of the page).

$$S_n = P_F = 1 - P_s = 1 - \begin{pmatrix} \frac{2w+s+m(w+s)-r-2w_n}{w+s} \times & (1 - d)^m \\ + \frac{r-w-m(w+s)+2w_n}{w+s} \times & (1 - d)^{m+1} \end{pmatrix} \tag{13}$$

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