Random Yield Prediction Based on a Stochastic Layout Sensitivity Model

Rani S. Ghaida, *Student Member, IEEE*, Ken Doniger, *Senior Member, IEEE*, and Payman Zarkesh-Ha, *Senior Member, IEEE*

***Abstract*—Yield loss caused by random defects is an important manufacturability concern. Random yield of modern integrated circuits is associated with layout sensitivity to defects defined as the ratio of critical area to the overall layout area. This paper proposes a methodology to predict random yield with high fidelity based on a stochastic layout sensitivity model that uses very basic layout information. The model has very important applications including pre-layout yield prediction and yield forecasting for future process technologies.**

***Index Terms*—Critical area analysis, defect density, design for manufacturability, layout sensitivity, random yield modeling and prediction.**

I. Introduction

THE MOVE to advanced nanometer nodes and new process materials is diminishing semiconductor designers' ability to estimate and realize device yields. Mechanisms of reducing yield loss have become ever more dependent on designs, not just improvement of the manufacturing process.

Yield loss is caused by manufacturing defects such as printability errors related to lithography [1], variations caused by chemical mechanical planarization (CMP) [2], and circuit failure induced by random particles [3].

Yield loss caused by random particles is referred to as random yield loss. On the other hand, yield loss resulting from printability errors and CMP can be classified into systematic or parametric yield loss. The product of all three yield losses is the overall yield loss, which is also defined as the ratio of devices performing properly to the total number of devices of produced wafers. This paper is concentrated only on random yield loss which has the highest percentage among all other yield loss components according to International Technology Roadmap for Semiconductor (ITRS) [4]. In order to predict requirements of future technologies, ITRS assumes 75% overall yield mainly composed of 83% random yield and 90% systematic yield for microprocessor technology, and 85% overall yield mainly composed of 89.5% random yield and 95% systematic yield for DRAM technology.

Random yield of semiconductor fabrication is a major factor affecting the overall fabrication yield. Yield modeling is traditionally based on the analysis of the "critical areas" i.e., portions of the layout where the center of a defect must fall to cause a functional failure of the device [5]. Layout robustness is characterized by the ratio of critical areas to the layout area, also known as the "layout sensitivity" [6]. The layout sensitivity to defects varies between 0 and 1. High layout sensitivity indicates the layout's high chances of failing defects and low layout sensitivity indicates the layout's high chances of surviving defects.

As the functionality of ICs grows and feature dimensions are scaling down, modern VLSI devices are becoming evermore complex and analysis of their critical areas becomes more computationally expensive and time-consuming.

This paper offers a new method for critical area computation using a stochastic layout sensitivity model. The new method can significantly expedite random yield analysis and prediction for current and future complex VLSI devices.

Section II explains different types of interconnect manufacturing defects. Section III illustrates the definitions of critical area and layout sensitivity. Section IV gives an overview of existing methods of random yield modeling based on critical area analysis. A model predicting the layout sensitivity to spot defects is derived in Section V. Results of testing the model and comparisons with actual data extracted from layouts are presented in Section VI. Section VII proposes some applications of the layout sensitivity model.

II. Major Types of Manufacturing Defects Caused by Random Particles

Random particles are either particles floating in the air and particles originating from etching of material involved in many steps of the fabrication process. Failure to eliminate such particles from the surface of the wafer during the processing of each layer can generate manufacturing defects and circuit failure. Even the presence of tiny particles as small as 1/2 to 1/3 of the size of the minimum feature can be risky and result in a failure [3]. Manufacturing defects can be classified into catastrophic and non-catastrophic defects. Catastrophic defects lead to circuit failure during the manufacturing process, and consequently, result in yield loss. Whereas, non-catastrophic defects, such as narrow defects [7], represent a concern for semiconductor reliability.

Manuscript received February 11, 2008; revised September 09, 2008; accepted March 10, 2009. First published July 07, 2009; current version published August 05, 2009.

R. S. Ghaida was with the Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, NM 87131 USA. He is now with the Electrical Engineering Department, NanoCAD Lab, University of California, Los Angeles, CA 90095 USA (e-mail: rani@ee.ucla.edu).

P. Zarkesh-Ha is with the Department of Electrical and Computer Engineering, University of New Mexico, Albuquerque, NM 87131 USA (e-mail: payman@ece.unm.edu).

K. Doniger is with the Abbott Laboratories, Alameda, CA 94502 USA (e-mail: k.doniger@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TSM.2009.2024821

0894-6507/$26.00 © 2009 IEEE

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

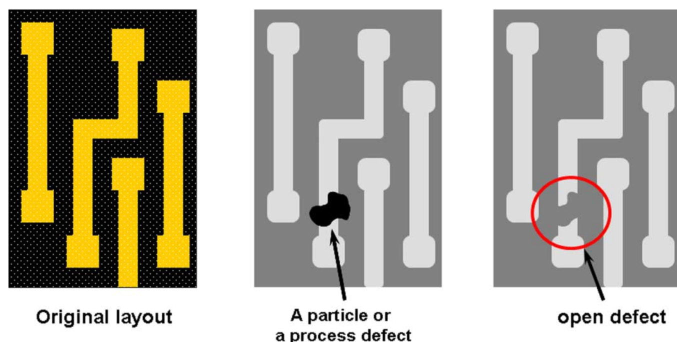

Fig. 1. Sample of a layout showing an open defect (reprinted from [8]).

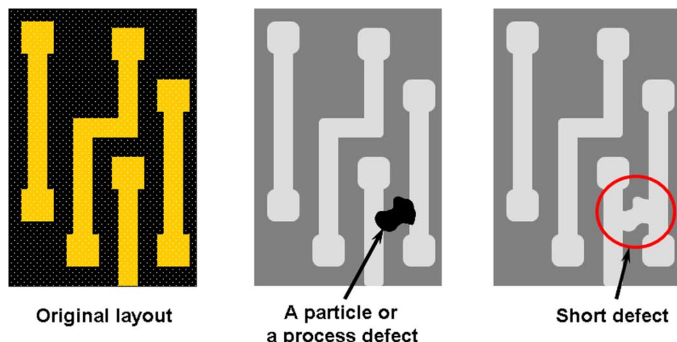

Fig. 2. Sample of a layout showing a short defect (reprinted from [8]).

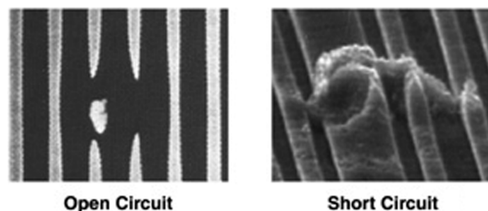

Fig. 3. Spot defect photographs (Photograph used with permission of *EE Times*, a CMP Media LLC publication) [12].

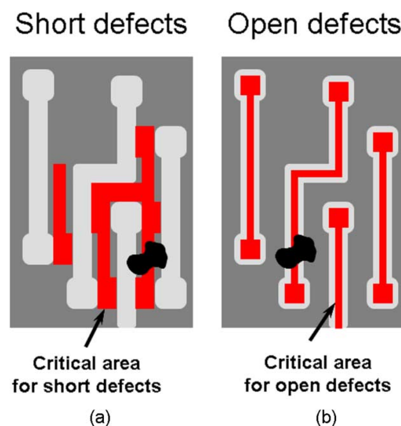

Fig. 4. Critical area for (a) short defects and (b) open defects.

There are two types of catastrophic defects caused by random particles: open and short defects.

A. Open Defects

An open spot defect or cut occurs when a nonconductive defect creates an electrical "break" or disconnection in a signal path. Fig. 1(c) illustrates an example of an open defect for the layout in Fig. 1(a). Fig. 1(b) shows the location of a particle or a spot defect that can create such an open failure.

With the shift to dual-damascene copper backend, probability of failure caused by open defects has become a challenging issue [9]. Moreover, open defects are usually complex and hard to diagnose during test procedures [10], [11].

B. Short Defects

A short or bridge defect occurs when a conductive defect creates an electrical connection between two neighboring wires. Fig. 2(c) illustrates an example of a short defect for the layout in Fig. 2(a). Fig. 2(b) shows the location of a particle or a spot defect that can create such a short failure.

III. Critical Area and Layout Sensitivity

The term, "critical area," was first introduced by C. Stapper in 1976 [5]. Since then, critical area has become a widely accepted measure of the sensitivity of VLSI design to defects occurring during the manufacturing process.

By definition, critical area is the area of a layout where the occurrence of a defect would cause functional failure. Depending on the defect size, there are only certain regions in the layout that the placement of defect could result in a failure.

For instance, the region highlighted in Fig. 4(a) shows the area at which the placement of the center of a defect would cause a short failure. Similarly, the region highlighted in Fig. 4(b) shows the area at which the placement of the center of a defect would cause an open failure. The area of these highlighted regions is the critical area.

Critical area depends on the defect size. Larger defect size creates a larger critical area. For instance, the critical area of a very large defect can be the entire layout area if the placement of such defect anywhere on the layout causes a failure. Obviously, the larger the critical area (highlighted regions in Fig. 4), the more sensitive the layout becomes to the defect.

The layout sensitivity is defined as the ratio of critical area to the layout area. Layout sensitivity, therefore, ranges from 0.0 to 1.0.

To perform yield analysis, the critical area must be computed at each level of metal layer for a range of defect sizes over the entire chip layout. Considering the modern VLSI designs with billions of interconnect segments, this would require an extensive computational effort.

The focus of this paper is to develop a stochastic model for layout sensitivity that can significantly expedite random yield analysis and prediction for current and future complex VLSI designs.

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

IV. Random Yield Modeling Based on Critical Area Analysis

Critical area is a widely accepted figure of merit that describes the layout sensitivity to manufacturing defects. As a result, random yield modeling is traditionally based on critical area analysis. This section presents conventional methods for random yield modeling.

Random yield can be evaluated using the Poisson model as follows:

$$Y_m = e^{-\lambda} \tag{1}$$

where Y_m is the random yield for metal layer m, and λ is the average number of defects.

Random yield of the whole die, Y, is given by:

$$Y = \prod_{m=1}^{M} Y_m \tag{2}$$

where M is the maximum number of metal layers.

λ is given by:

$$\lambda = \sum_{j} D_0 A_{c,j} \tag{3}$$

where j is the type of defect (open or short defect), D_0 is the average defect density, and $A_{c,j}$ is the average critical area for all defect sizes. $A_{c,j}$ is evaluated using the following equation:

$$A_{c,j} = \int_0^{\infty} \mathrm{A}_{c,j}(r) \times f_s(r) \cdot dr \tag{4}$$

where $A_{c,j}(r)$ is the critical area of defect size r for a defect type j, and $f_s(r)$ is the probability density function of defect size.

The Poisson model is known to give pessimistic results when applied to actual designs. This is because defects tend to group in clusters, and do not have a uniformly random distribution over the die as assumed in the Poisson model [13]. Many other random yield models that include the effect of clustering were derived from the Poisson model [14]–[16]. A comparison of yield models is presented in [17] and [18].

Application of any random yield model requires the critical area extraction. Widely used methods for critical area extraction are categorized into the following types [19]: Monte Carlo simulation, geometric method, and virtual artwork approach.

Monte Carlo simulation [20] consists of randomly placing a large number of virtual defects on the layout and, checking for device failure for each defect. The probability of failure is determined by dividing the number of defects causing a failure by the total number of defects that was placed. Critical area is then inferred from the probability of failure by multiplying it by the chip area.

An early contribution to the geometric approach is offered in [21]. This approach is based on the computation of the critical areas for different intervals of defect size. These critical areas are typically computed by applying a shape-contraction on the layout, followed by a shape-expansion, and then a subtraction of the resulting layout from the original one [22]. The grid method, proposed in [23], is another way of the geometric method. In grid method, the critical area is approximated by using a grid over the layout and determining, at every point of the grid, the radius of the smallest defect that causes a failure. [19] offers another important method of the geometric approach that is based on the concept of Voronoi diagrams. This method has significantly faster run time performance than other geometric methods.

The virtual artwork approach is proposed by Maly [24]. It consists of computing the critical area of a virtual layout, extracted from the original one, that allows an easy determination of a histogram of interconnect widths and spacings as well as the interconnect lengths of specific widths.

Critical area extraction requires huge amount of computations and is time consuming. One way to avoid this limitation is proposed by Allan and Walton [25], [26]. Their approach consists of performing critical area extraction in sample regions rather than extracting the critical area at every point of the design. This approach extensively reduces the time and effort of critical area analysis and has a minor effect on the accuracy of yield estimation.

All discussed methods of critical area computation are only applicable to actual layouts. A different approach, known as the stochastic method, is used for pre-layout yield prediction. Essentially, the stochastic method consists of critical area modeling based on some basic information about the layout. The earliest contribution to this method is offered by Stapper [27], [28]. In his work, Stapper used linear approximations to model the critical area as a function of defect size. His model makes use of basic layout information such as the interconnect width, spacing, and length as well as the total number of interconnects. Heineken *et al.*, [29] also uses a linear approximation of the critical area to predict the yield. This approximation is either performed using least square function fit or based on transistors density. Another contribution to the stochastic method is made by Christie and de Gyvez [30] where information about interconnect length distribution and interconnect widths were used to model the critical area as a function of the defect size. The stochastic method is necessary for pre-layout yield prediction and is extremely fast and easy. However, existing models of the stochastic method are all characterized by noticeable inaccuracy in modeling the critical area.

In this paper, we contribute to the stochastic method for critical area analysis by offering a model for predicting the layout sensitivity with good fidelity.

V. A Stochastic Layout Sensitivity Model

Assumptions

Some assumptions are made in order to simplify the derivation of the model. First, we assume that interconnect routing is performed using a grid of channels. Channels can be either empty or occupied by interconnects and are separated by a distance equal to the interconnect spacing. We also assume that the routing of different interconnects are independent of each other. These assumptions are made without loss of generality of the model since the same assumptions are also made in many yield analysis tools to perform critical area studies.

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

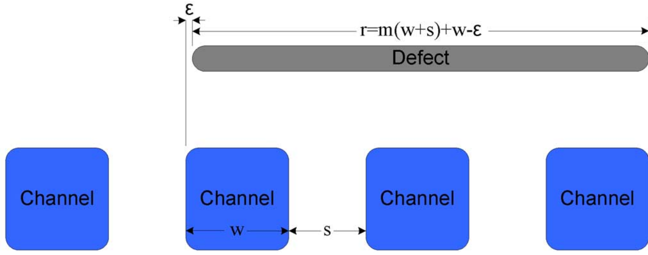

Fig. 5. Example of an open defect covering two channels.

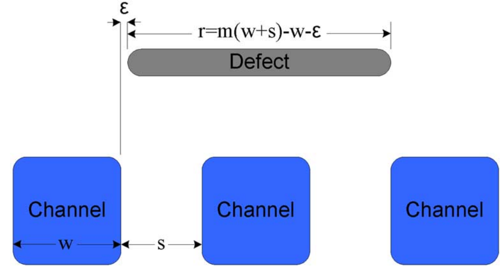

Fig. 6. Example of a short defect covering two channels.

A. Parameter Definitions

We define channel density, d, as the probability of a random channel to be filled. Therefore, the probability of a random channel to be empty is given by $(1-d)$. Channel density, d, can be deduced from the metal density, D, using the following expression:

$$D = d\frac{w}{w+s} \tag{5}$$

where w and s are the interconnect width and spacing, respectively.

Since w and s are preset by the fabrication technology and D can be easily computed from the layout, the channel density is easily determined.

Also, we define m as the number of channels covered by a defect and r as the defect size.

B. Layout Sensitivity Model for Open Defects

The largest open defect size that has a probability of covering *exactly* m channels is given by

$$r = m(w+s) + w - \varepsilon \tag{6}$$

where ε is an infinitesimal distance. An open defect must cover at least 1 channel to have a probability to create an open circuit failure. Therefore, m in (6) has a minimum value of 1. ε is included in (6) to make sure that exactly m channels can contribute to an open defect in case it occurs. For instance, if $m=1$, then $r = 2w + s - \varepsilon$ and exactly 1 channel is covered by the defect. If $m=2$, then $r = 3w + 2s - \varepsilon$ and exactly 2 channels are covered by the defect. This is also depicted by Fig. 5 where $m=2$. All m consecutive channels must be empty for the device to overcome the defect. Therefore, the probability of the device survival is

$$P_s = (1-d)^m. \tag{7}$$

Consequently, the probability of the device failure is given by

$$P_f = 1 - P_s = 1 - (1-d)^m. \tag{8}$$

The layout sensitivity to open defects is in fact the probability of failure due to an open defect. Hence, by substituting m in (8) by its value from (6) and neglecting ε, the layout sensitivity model for opens becomes

$$S_{open} = 1 - (1-d)^{((r-w)/(w+s))}. \tag{9}$$

This model for layout sensitivity to open defects uses very basic layout information i.e., defect size r, wire width w, wire spacing s, and the channel density d.

C. Layout Sensitivity Model for Short Defects

The largest short defect size that has a probability of shorting *exactly* m channels is given by:

$$r = m(w+s) - w - \varepsilon \tag{10}$$

where ε is an infinitesimal distance. A short defect must involve at least two channels to induce a short circuit failure. Therefore, m in (10) has a minimum value of 2. ε is included in (10) to make sure that exactly m channels can contribute to a short defect in case it occurs. For instance, if $m=2$, then $r = w + 2s - \varepsilon$ and exactly two channels can contribute to a short circuit. If $m=3$, then $r = 2w + 3s - \varepsilon$ and exactly 3 channels can contribute to a short circuit. This is illustrated by Fig. 6 where $m=2$. For the device to overcome the defect, either all m consecutive channels must be empty, or *only one* channel is filled and the remaining channels are empty since a defect involving a single interconnect cannot create a short circuit.

The probability of having m consecutive empty channels, P_1, is

$$P_1 = (1-d)^m \tag{11}$$

and the probability of having one filled channel and $m-1$ empty channel, P_2, is

$$P_2 = md(1-d)^{m-1} \tag{12}$$

where the coefficient m accounts for arbitrary location of the filled channel in m different positions. Consequently, the probability of the device survival is given by

$$P_s = P_1 + P_2 = (1-d)^m + md(1-d)^{m-1} \tag{13}$$

and the probability of failure, P_f, is then

$$P_f = 1 - P_s = 1 - (1-d)^m - md(1-d)^{m-1}. \tag{14}$$

It can be also written as

$$P_f = 1 - [1 + (m-1)\cdot d]\cdot(1-d)^{m-1}. \tag{15}$$

The layout sensitivity to short defects is in fact the probability of failure due to a short defect. Hence, by substituting m in (15)

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

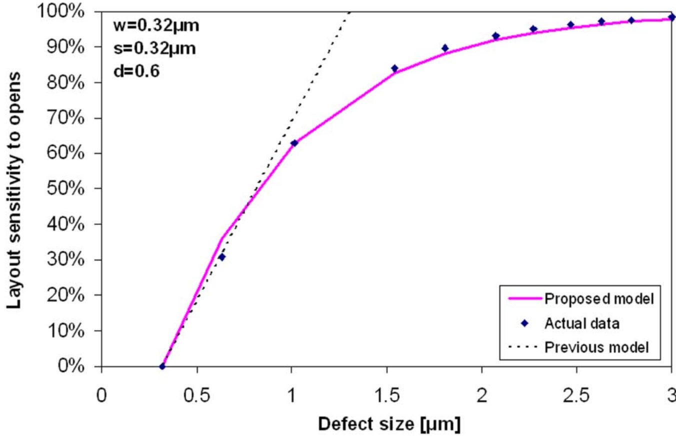

Fig. 7. Comparison of the proposed sensitivity model with extracted layout sensitivity and a previous sensitivity model [30] for open defects.

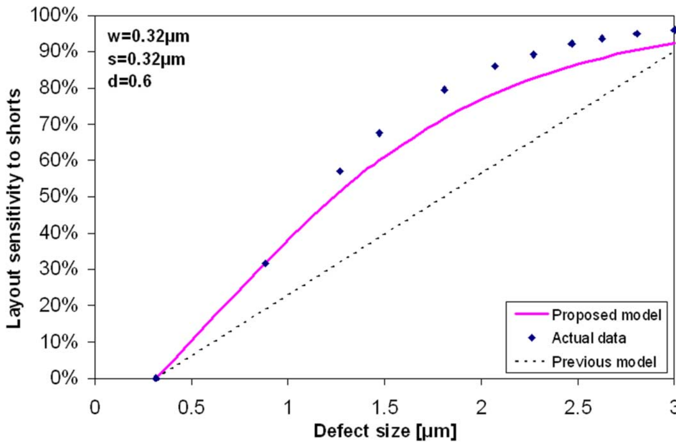

Fig. 8. Comparison of the proposed sensitivity model with extracted layout sensitivity and a previous sensitivity model [30] for short defects.

by its value from (10) and neglecting ε, the layout sensitivity model for shorts becomes

$$S_{short} = 1-\left[1+\left(\frac{r-s}{w+s}\right)\cdot d\right]\cdot(1-d)^{((r-s)/(w+s))}. \quad (16)$$

This model for layout sensitivity to short defects uses very basic layout information i.e., defect size r, wire width w, wire spacing s, and the channel density d.

VI. Model's Validation

The sensitivity model for short and open defects was tested for 0.32-μm technology node with an interconnect density of 0.6. Figs. 7 and 8 shows the result of testing the layout sensitivity model for open and short defects respectively, and a comparison with the sensitivity extracted from an actual layout as well as the previous stochastic model offered in [30]. The average percent errors of the model's outcomes when compared to actual data was found to be 2.4% for opens and 6.2% for shorts, which is an indication of the high fidelity of the model.

The sensitivity model for shorts was again tested for 1ìm technology node and compared in Fig. 9 to actual data extracted from a microprocessor design [31]. In the plots of Fig. 9, $w = s = 1$ μm for all metal layers, and $d = 0.3$, 0.15, 0.12 and 0.09

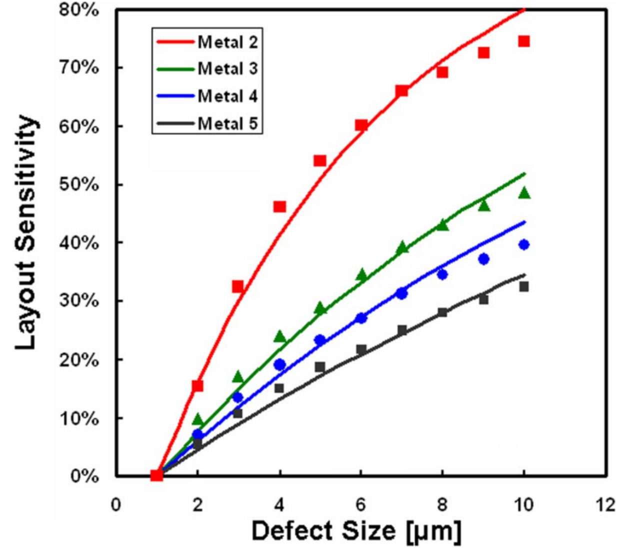

Fig. 9. Comparison of the proposed model with layout sensitivity for shorts extracted from a real microprocessor chip [31] (points represent actual data and lines represent the model).

for metal layers M2, M3, M4, and M5, respectively. The channel densities for the different metal layers were chosen to have the best fit of the model to the extracted data. This was done because of the absence of information about the channel or metal densities for the data in [31]. In this figure, metal density, and therefore channel density, decreases at higher metal levels as expected. This is because it becomes harder to pack long wires densely at higher metal levels.

The sensitivity model for short and open defects was also tested on actual designs with a 45-nm technology node. This is performed using PRS, a placement and routing software previously developed in [32]. PRS is used to create the layout of a small circuit (52 logic gates) that computes the absolute value of the difference between two 2-bit numbers. The channel density is then extracted from the layout and provided to the predictive model for shorts and opens. Results were compared then to the outcomes of simulations. These simulations were performed by expanding PRS tool to generate defects and check for the resulting open (or short) circuits. A large number of defects with different sizes (100 000 defects per defect size) are randomly placed on the layout and the number of resulting opens (or shorts) for a single metal layer is determined. The probability of failure associated with each defect size is then obtained by the ratio of the total number of resulting opens (or shorts) to the total number of generated defects for each defect size.

Figs. 10 and 11 present comparisons between the simulated and predicted probabilities of failure of open and short defects, respectively, for different defect sizes. Results show the accuracy of the model in predicting open and short defects, i.e., 1.4% error for opens and 6.2% for shorts.

Results show that the model estimates opens more accurately than it estimates shorts. The main reason for this difference is the reproduction of estimation error in layout sensitivity model for shorts. In this model, layout sensitivity depends on P_2 given in (12), which is the product of two estimated probabilities: 1) probability of having exactly one filled channel at the different

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

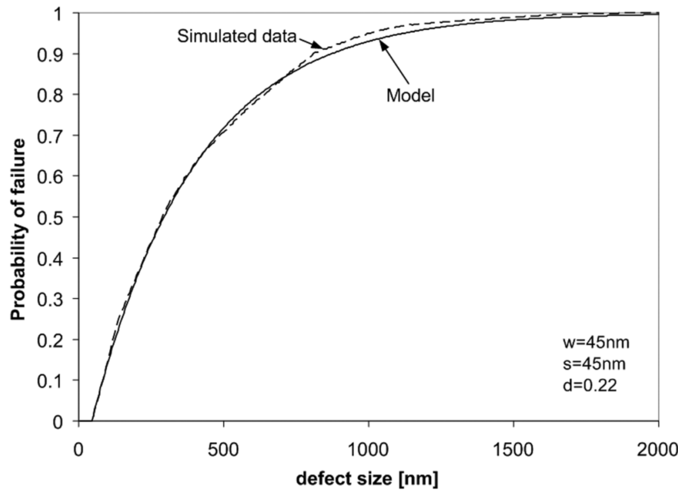

Fig. 10. Comparison between probability of failure estimated by the layout sensitivity model for open defects and probability of failure due to open defects extracted from an actual design.

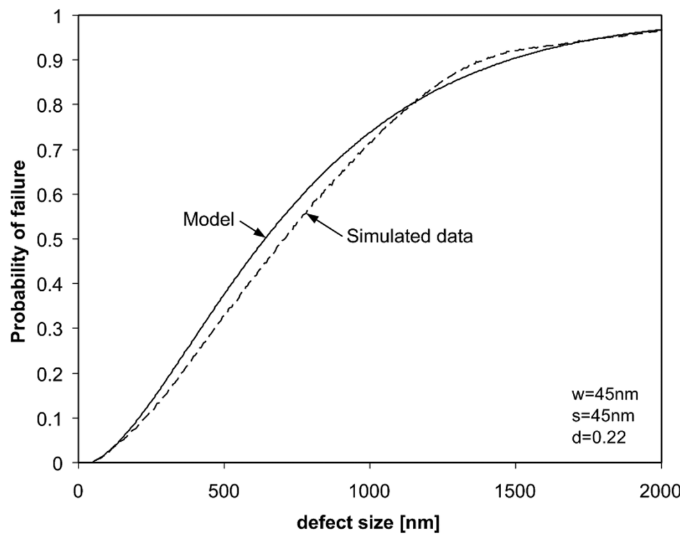

Fig. 11. Comparison between probability of failure estimated by the layout sensitivity model for short defects and probability of failure due to short defects extracted from an actual design.

locations, and 2) probability of having all remaining channels empty. Another reason for the reduced accuracy in the estimation of shorts is that the model does not account for shorts between line-ends of the same channel.

VII. Applications

A. Pre-Layout Yield Estimation

The layout sensitivity to spot defects can be predicted using the model presented in this paper. The only unknown variable in the model is the channel density d which can be inferred from the metal density D using (5). The metal density is usually available through post-layout extraction tools for use in other applications such as metal thickness variation analysis. In case the metal density is not available, it can be calculated from the layout using information about interconnects length. The metal density can also be estimated even before coming up with the actual layout. Specifically, this can be performed for designs that belong to a family of products using statistical information. Also, the metal density can be predicted using a heuristic approach [33] based on an estimation of interconnect length distribution derived in [34]. Consequently, implementation of the model to predict the layout sensitivity of a product becomes very easy and can be done even before starting the design phase. Since the layout sensitivity to spot defects is defined as the ratio of critical area to the overall layout area, the yield can be estimated using any of the existing yield models that are based on a critical area analysis [35].

It is very important to be able to predict if a design meets the acceptable device yield at a very early stage. This will ensure that the design decisions, such as number of metal layers, are made such that the layout meets the yield requirement after the design completion. Because layout sensitivity is considered at an early phase of design, time consuming application of post-layout modifications such as design for manufacturability (DFM) techniques and wire spreading [12], which are necessary for achieving acceptable yield [36], is reduced.

B. Yield Forecasting for Future Technologies

The most widely used model is the negative binomial yield model offered in [16]. The model is given by [18]:

$$Y = \left(1 + \frac{\lambda}{\alpha}\right)^{-\alpha} \tag{17}$$

where α is the cluster parameter, also called clustering factor. It determines the degree of defect clustering. A smaller value of α indicates more clustering. Typical values range between 0.3 and 5 [13], [18]. ITRS adopts also the negative binomial yield model and uses a cluster parameter of 2 [4].

The model of (17) requires the computation of λ which can be evaluated using (3). D_0 of (3) can be estimated. Furthermore, ITRS has published a roadmap for the value of D_0 for future technologies [4]. $A_{c,j}$ of (3) can be evaluated using (4). $A_{c,j}(r)$ of (4) can be inferred from the layout sensitivity computed using the model presented in Section V. Specifically,

$$A_{c,j}(r) = S_j(r) \times \text{die area} \tag{18}$$

where $S_j(r)$ is the sensitivity to defect type j of size r. For the probability density function of defect size $f_s(r)$, studies indicate that it has a specific distribution. A well established probability density function of defect size is of the form [27]:

$$f_s(r) = \begin{cases} \frac{2(n-1)r}{(n+1)r_0^2}, & 0 \le r \le r_0 \\ \frac{2(n-1)r_0^{n-1}}{(n+1)r^n}, & r > r_0 \end{cases} \tag{19}$$

where r_0 is the defect size with the peak density, and n is a parameter that depends on the cleanliness of fabrication process and is typically equal to 3 [6], [27]. Moreover, it is believed that r_0 is typically less than the minimum feature size [6]. Fig. 12 depicts the plot of (13) for 90-, 68-, 45-, 32-, and 22-nm technology nodes in a typical fabrication line, i.e., $n = 3$, and where r_0 are chosen in accordance with ITRS [4].

We have just proposed a method for determining random yield due that uses layout sensitivity to defects and some in-

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

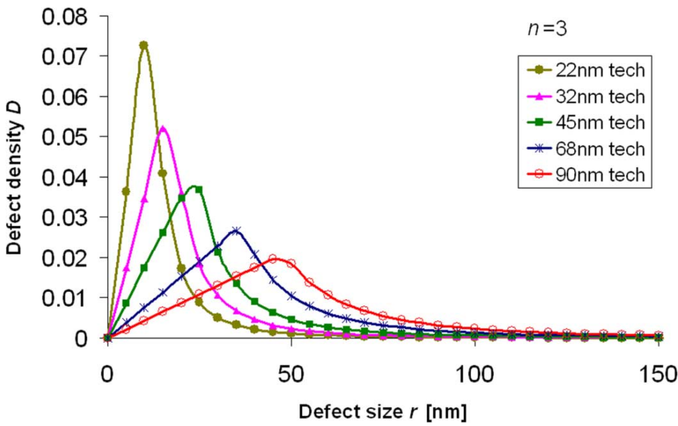

Fig. 12. Defect size distribution for 90-, 68-, 45-, 32-, and 22-nm technology nodes in a typical fabrication line.

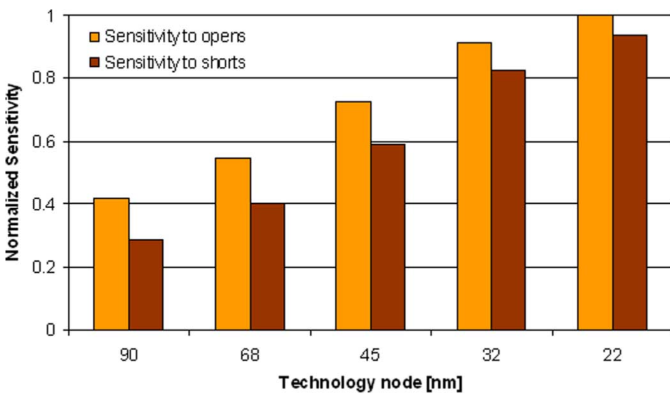

Fig. 13. Normalized sensitivity to open and short defects of a fictitious layout with 90-, 65-, 45-, and 32-nm technology nodes.

formation about defect density. Layout sensitivity can be determined using the proposed model once the channel (or metal) density is predicted. Subsequently, yield forecasting for future technologies can be performed if information about critical defect size and average defect density is given or estimated.

C. Predicting Requirements of Defect Density for Sub-45-nm Technologies

The proposed layout sensitivity model is applied to a fictitious design with 90-, 68-, 45-, 32-, and 22-nm technology nodes. The channel density is chosen to be the same for all metal layers and is equal to 0.6. The technology nodes, and therefore interconnect width w and spacing s, as well as the maximum number of metal layers and the number of metal layer per tier were chosen in accordance with ITRS [4] (refer to Table I). The normalized layout sensitivities to spot defects associated with the different technology nodes are shown in Fig. 13.

The chart of Fig. 13 shows that the layout sensitivity to defects almost doubles every three technology generations. And because the fabrication yield is very dependent on the sensitivity to defects and defect density, then reduction in defect density is necessary in order to achieve acceptable yield for sub-45-nm technologies. This is achieved by defect reduction in process equipment that remains paramount to achieving defect density goals.

TABLE I
PARAMETERS USED IN COMING UP WITH THE RESULTS OF THIS SUBSECTION

Technology node [nm]	90	68	45	32	22
w & s for local wires [nm]	90	68	45	32	22
w & s for semi-global wires [nm]	200	140	90	64	44
w & s for global wires [nm]	300	210	135	96	66
r_0 [nm]	45	34	22.5	16	11.5
Chip size [mm^2]	111	n/a	140	n/a	140
Number of metal layers	11	11	12	13	13
Number of metal layers for local/semi-global/global tiers	4/4/3	4/4/3	4/4/4	5/4/4	5/4/4
Channel density for all metal layers	0.6	0.6	0.6	0.6	0.6

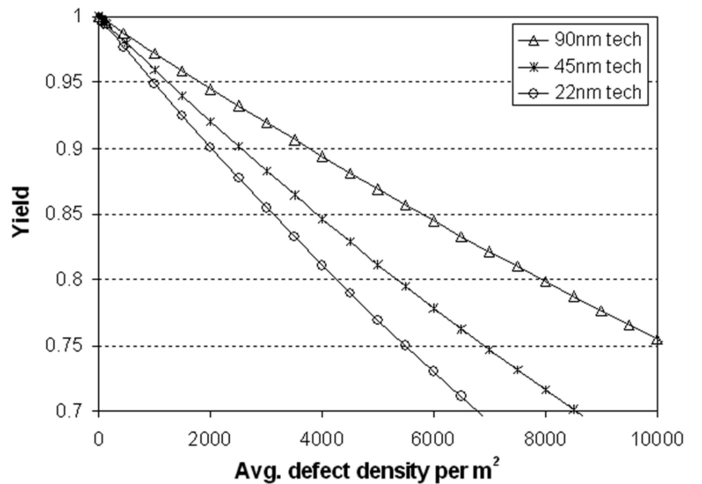

Fig. 14. Plot of random yield as a function of average defect density for 90-, 45-, and 22-nm technology nodes.

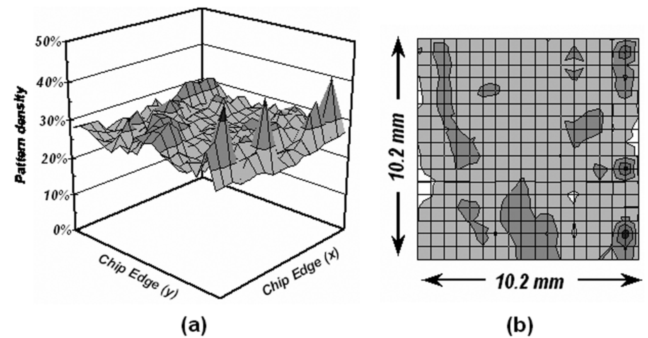

Fig. 15. Pattern density distribution in (a) 3-D and (b) 2-D.

The procedure for setting requirements of defect density for future technologies is illustrated by a case study for some current and future technology nodes. We start by determining the critical area using (16). To do this, the critical defect size, r_0, for which the defect size distribution peaks, is required. This parameter can be easily estimated because its scaling is uniform as technology node scales down. By applying the procedure of Section VII-B, we determine the random yield associated with the average defect density for different technology nodes. The chip area is required for that. So, it was chosen in accordance with ITRS. Table I summarizes all parameters used to come up with the results shown in this subsection. Fig. 14 plots the

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

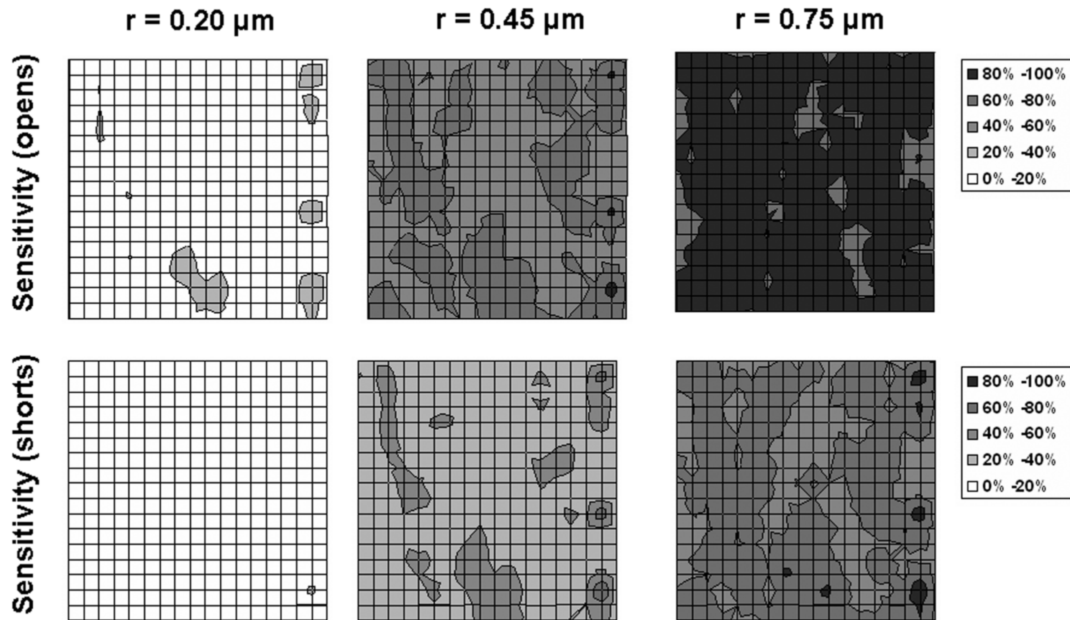

Fig. 16. Layout sensitivity patterns in a real design using the proposed layout sensitivity model, i.e., (9) and (16) (reprinted from [8]).

random fabrication yield versus the average defect density for 90-, 45-, and 22-nm technology nodes. Now, requirements of the defect density can be set according to the targeted yield. For instance, if the acceptable yield is at least 90%, then the minimum average defect density is 3500, 2500, and 2000 $\mathrm{faults/m^2}$ for 90-, 45-, and 22-nm technology nodes, respectively.

D. Layout Diagnosis and Yield Enhancement

Layout modifications such as wire spreading and nets re-routing are performed on the design to enhance the yield. Layout modifications are extremely time-consuming if applied to the entire layout. The layout sensitivity model offers a solution for this problem. In particular, the layout sensitivity of the different parts of the circuit can be determined using the model. Then, layout sensitivity patterns can be generated. Parts having high sensitivity to spot defects are marked for diagnosis. Their sensitivity is reduced during placement and routing and the application of pre- and post-layout modifications for yield enhancement. An example is illustrated in Figs. 15 and 16. Fig. 15 shows the metal density patterns extracted from a real design using *Quickcap*[1] tool. Fig. 16 shows the layout sensitivity patterns inferred from the metal density patterns of Fig. 15 using the layout sensitivity model.

Traditionally, the layout sensitivity is determined using post-layout extraction tools. This method has major drawbacks when compared to the proposed layout sensitivity estimation approach. First, the traditional method does not allow for major placement and routing modifications which can be performed before and during the design phase when the proposed method is adopted. In addition, the previous method is extremely time-consuming since it requires performing expansion, shrinkage, and overlap of polygons, where there exists billions of interconnect segments (polygons) on the chip. Moreover, it must be performed for a range of defect sizes and at each metal level. On the other hand, the process becomes efficient when the layout sensitivity is estimated using the model described in this paper.

VIII. Conclusion

Typically, modeling of semiconductor fabrication random yield is either based on spot defect simulations or an analysis of the critical area. In both cases, the process is time consuming for today's complex VLSI designs, where good accuracy is necessary. On the other hand, the layout sensitivity model presented in this work can approximate the critical area with good fidelity and no delay. The efficiency of the sensitivity model makes its application in modeling, predicting, and enhancing the semiconductor random yield very beneficial. Another main advantage of the layout sensitivity model is its ability to predict the yield of a particular product even before coming up with its actual design. Even though this prediction *can never* be accurate enough for a design or business decision to be solely based on, it can give insights about cost and yield by comparison of predicted yield of the design when different architectures or design rules are embraced.

Acknowledgment

The authors would like to acknowledge the fruitful discussions with C. Hawkins from the University of New Mexico and M. Wisniewski from IBM, NY. In addition, the authors gratefully recognize the in-depth review and constructive comments of D. De Vries from NXP Semiconductor, France.

References

[1] S. Raghvendra and P. Hurat, "DFM: Linking design and manufacturing," in *Proc. IEEE Int. Conf. VLSI Design*, Jan. 2005, pp. 705–708.

[2] J. T. Pan, P. Li, K. Wijekoon, S. Tsai, and F. Redeker, "Copper CMP integration and time dependent pattern effect," in *Proc. Int. Interconnect Technol. Conf.*, 1999, pp. 164–166.

[1]Quickcap is a trademark of the Random Logic Corporation, Fairfax, VA.

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.

[3] S. W. Jones, *Introduction to Integrated Circuit Technology*. Georgetown, MA: ICKnowlegde LLC, Revision, 2005.
[4] ITRS 2006 Update, International Technology Roadmap for Semiconductors, Report International Technology Roadmap for Semiconductors, 2006.
[5] C. H. Stapper, "LSI yield modeling and process monitoring," *IBM J. Res. and Dev.*, vol. 20, no. 3, 1976.
[6] J. P. de Gyvez, "Yield modeling and BEOL fundamentals," in *Proc. Int. Workshop System Level Interconnect Prediction (SLIP)*, 2001, pp. 135–163.
[7] R. S. Ghaida and P. Zarkesh-Ha, "Estimation of electromigration-aggravating narrow interconnects using a layout sensitivity model," in *Proc. IEEE Int. Symp. Defect and Fault-Tolerance in VLSI Systems (DFT)*, 2007, pp. 59–67.
[8] P. Zarkesh-Ha and K. Doniger, "Stochastic interconnect layout sensitivity model," in *Proc. Int. Workshop System Level Interconnect Prediction (SLIP)*, 2007, pp. 9–14.
[9] D. K. de Vries and P. L. C. Simon, "Calibration of open interconnect yield models," in *Proc. IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems*, 2003, pp. 26–33.
[10] J. Segura and C. Hawkins, *CMOS Electronics, How It Works, How It Fails*. Piscataway, NJ: IEEE Press, Wiley-Interscience, 2004, ch. 6, pp. 161–163.
[11] A. Nardi and A. L. Vincentelli, "Logic synthesis for manufacturability," *IEEE Design & Test of Computers*, vol. 21, no. 3, pp. 192–199, May-Jun. 2004.
[12] F. Lee, A. Ikeuchi, Y. Tsukiboshi, and T. Ban, Critical Area Optimizations Improve IC Yields [Online]. Available: http://www.eetimes.com/showArticle.jhtml?articleID=175802288
[13] I. Koren and Z. Koren, "Defect tolerance in VLSI circuits: Techniques and yield analysis," *Proc. IEEE*, vol. 86, no. 9, pp. 1819–1837, Sep. 1998.
[14] B. T. Murphy, "Cost-size optima of monolithic integrated circuits," *Proc. IEEE*, vol. 52, no. 12, pp. 1537–1545, Dec. 1964.
[15] R. B. Seeds, "Yield, economic, and logistic models for complex digital arrays," in *1967 IEEE Int. Conv. Rec., pt. 6*, Apr. 1967, pp. 61–66.
[16] C. H. Stapper, "Defect density distribution for LSI yield calculations," *IEEE Trans. Electron Devices*, vol. 20, no. 7, pp. 655–657, Jul. 1973.
[17] L. Peters, "Choosing the best yield model for your product," in *Semiconductor Int.*, May 01, 2000.
[18] W. Kuo and T. Kim, "An overview of manufacturing yield and reliability modeling for semiconductor products," *Proc. IEEE*, vol. 87, no. 8, pp. 1329–1344, Aug. 1999.
[19] E. Papadopoulou and D. T. Lee, "Critical area computation via Voronoi diagrams," *IEEE Trans. Computer-Aided Design*, vol. 18, no. 4, pp. 463–474, Apr. 1999.
[20] H. Walker and S. W. Director, "VLASIC: A catastrophic fault yield simulator for integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, no. 4, pp. 541–556, Oct. 1986.
[21] W. Maly and J. Deszczka, "Yield estimation model for VLSI artwork evaluation," *Electron. Lett.*, vol. 19, no. 6, pp. 226–227, Mar. 1983.
[22] S. Gandemer, B. C. Tremintin, and J. J. Charlot, "Critical area and critical levels calculation in IC yield modeling," *IEEE J. Solid State Circuits*, vol. 35, no. 2, pp. 158–166, Feb. 1988.
[23] I. A. Wagner and I. Koren, "An interactive VLSI CAD tool for yield estimation," *IEEE Trans. Semicond. Manuf.*, vol. 8, no. 2, pp. 130–138, May 1995.
[24] W. Maly, "Modeling of lithography related yield losses for CAD of VLSI circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-4, no. 3, pp. 166–177, Jul. 1985.
[25] G. A. Allan and A. J. Walton, "Yield prediction by sampling with the eyes tool," in *Proc. IEEE Int. Symp. Defect and Fault-Tolerance in VLSI Systems (DFT)*, 1996, pp. 39–47.
[26] G. A. Allan, "Yield prediction by sampling IC layout," *IEEE Trans. Computer-Aided Design of Integr. Circuits and Syst.*, vol. 19, no. 3, pp. 359–371, Mar. 2000.
[27] C. H. Stapper, "Modeling of integrated circuit defect sensitivities," *IBM J. Res. and Dev.*, pp. 549–557, Nov. 1983.
[28] C. H. Stapper, "Modeling of defects in integrated circuit photolithographic patterns," *IBM J. Res. and Dev.*, vol. 28, no. 4, pp. 462–475, Jul. 1984.
[29] H. T. Heineken, J. Khare, and W. Maly, "Yield loss forecasting in the early phases of the VLSI design process," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1996, pp. 27–30.
[30] P. Christie and J. P. de Gyvez, "Pre-layout prediction of interconnect manufacturability," in *Proc. Int. Workshop System Level Interconnect Prediction (SLIP)*, 2001, pp. 167–173.
[31] J. Segal, L. Milor, and Y. Peng, Reducing Baseline Defect Density Through Modeling Random Defect-Limited Yield [Online]. Available: www.Micromagazine.com
[32] R. S. Ghaida and I. Ouaiss, A Different Approach to Fabricating Three-Dimensional Integrated Circuits Lebanese American Univ., Report, 2005.
[33] P. Zarkesh-Ha, S. Lakshminarayann, K. Doniger, W. Loh, and P. Wright, "Impact of interconnect pattern density information on a 90 nm technology ASIC design flow," in *Proc. Int. Symp. Quality Electronic Design (ISQED)*, 2003, pp. 405–409.
[34] J. A. Davis, V. De K, and J. D. Meindl, "A stochastic wire-length distribution for gigascale integration (GSI)-Part I: Derivation and validation," *IEEE Trans. Electron Devices*, vol. 45, no. 3, pp. 580–589, Mar. 1998.
[35] P. V. Zant, *Microchip Fabrication, a Practical Guide to Semiconductor Processing*, 5th ed. New York: McGraw-Hill Professional, 2004, ch. 6, pp. 139–157.
[36] EDA Tools Aim at Improving Yield Mentor Graphics Corp., 2005 [Online]. Available: www.SOCcentral.com

Rani S. Ghaida (S'04) received the B.E. degree in computer engineering from the Lebanese American University, Byblos, Lebanon, in 2006 and the M.S. degree in computer engineering from the University of New Mexico, Albuquerque, in 2008. He is currently working toward the Ph.D. degree in the Electrical Engineering Department, University of California, Los Angeles.

His research interests include design for manufacturability/yield/reliability, design-manufacturing interface, and system-level modeling of integrated circuits. He is a student member of SRC, IMPACT, ACM, and SPIE.

Ken Doniger (A'89–M'95–SM'09) received the Ph.D. degree in plasma physics from the University of California at Berkeley in 1984.

Since then, he has worked at various high tech companies in Silicon Valley, mostly doing mathematical modeling. He has worked in the microwave tube industry and the semiconductor industry. His current employer is in the medical device industry, and makes blood sugar meters for diabetics.

Payman Zarkesh-Ha (A'92–S'97–M'01–SM'04) received M.S. and Ph.D. degrees in electrical and computer engineering from Sharif University, Tehran, Iran, in 1994 and Georgia Institute of Technology, Atlanta, GA, in 2001, respectively.

He is an assistant professor at Electrical and Computer Engineering Department at University of New Mexico in Albuquerque, NM. During 2001–2006, he was with LSI Logic Corporation, Milpitas, CA; where he worked on interconnect architecture design for the next ASIC generations. In 2006, he joined the faculty of the Department of Electrical and Computer Engineering in the University of New Mexico, where he currently is engaged. Dr. Zarkesh-Ha served as industry liaison for LSI Logic Corp. with Semiconductor Research Corporation (SRC) and Microelectronics Advanced Research Corporation (MARCO) from 2001–2006. His research interests are Statistical modeling of VLSI systems, design for manufacturability, low-power and high-performance VLSI design. He has published over 40 refereed papers and a book chapter in these areas. He also holds five issued and four pending patents in this field. He is currently serving as technical committee member of System Level Interconnect Prediction Workshop.

Authorized licensed use limited to: Univ of Calif Los Angeles. Downloaded on August 9, 2009 at 02:22 from IEEE Xplore. Restrictions apply.