

## **SAI-WANG (ROCCO) TAM**

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Phone: 626-297-5582

**Objective: Internship Position;**

**Availability: June 2007 to Sept 2007**

**Interest: Challenging position in circuit design and related areas**

### **EDUCATION:**

Ph.D in Electrical Engineering in (IC&S) (Passed PhD Preliminary Exam)

UNIVERSITY OF CALIFORNIA, LOS ANGELES

Expected Graduation: June 2008

Master Science in Electrical Engineering

UNIVERSITY OF CALIFORNIA, LOS ANGELES

Graduation: June 2005

Current GPA: 3.73/4.0

Bachelors of Science in Electrical Engineering with Honor

UNIVERSITY OF CALIFORNIA, LOS ANGELES

Graduation: June 2003

Major GPA: 3.85/4.0

### **MOST RELEVANT COURSEWORK:**

Advanced Analog Integrated Circuit, Analog Circuit I&II, RF Circuit, VLSI Design, Advance Digital Circuit, Analog circuit lab, Digital Communication System, Digital Filter Design, Fiber Optics System Design, Applied Quantum Mechanics, Photonics Device, Classical Laser Theory, Optoelectronics, Photonics & Communication Design Lab, Laser Lab, Detection Theory of Communication and Radar Engineering, Digital Signal Processing, Engineering Electromagnetism

### **COMPUTER SKILLS/Languages:**

Proficiency in Verilog, Cadence, ADS, HSPICE , PCB Layout, UNIX, Perl, C++, C, Matlab, Maple, L-Edit, HFSS, Spice, FORTRAN, Mentor Graphics, ADMS

### **MAJOR RELATED EXPERIENCE**

**Intel Corporation, Santa Clara, CA, Jun 2006 – Sep 2006 (Three Months)**

**Internship Analog Mixed Signal Circuit Design Engineer**

- Implemented 45nm calibration circuit for high speed I/O buffer
- Designed voltage regulator for power management system in multi-core processor s
- Part of work group in the preliminary analog scaling design in 32nm process

**Intel Corporation, Portland, Oregon, Jun 2005 – Dec 2005 (Six Months)**

**Co-op Analog Mixed Signal Circuit Design Engineer**

- Implemented various large scale transistor level (order of +100,000 devices) mixed-signal circuit system model for the latest Dual Core and Multi Core Micro-Processor such as PLL and DLL with 65/45nm CMOS technology
- Designed fast PLL adaptive start-up circuit in transistor level which provides multiple start-up frequency for Multi-Core Processor
- Implemented various PLL and DLL models such as digital PLL and Bang-Bang PLL for fast locking and clock data recovery (CDR)system
- Responsible for developing Mixed-Signal validation model for multiple PLLs and DLL clocking generation system
- Co-developed new design and validation methodology for very large scale mixed-signal circuit

**Intel Corporation, Santa Clara, CA, Mar 2004 – Sep 2004 (Six Months)**

**Co-op Analog Mixed Signal Circuit Design Engineer**

- Successfully designed and debugged various deep sub-micron (65nm) digital and mixed-signal circuit on the latest Pentium Processor project
- Designed and verified high speed I/O data path circuit such as sensing amplifier and internal reference generator and performed various layout planning with mask designers
- Individually developed methodology and automation flows for an in-house design tool which can estimate glitch value in critical data path for the whole project. Trained the whole design team with this new process and automation tool
- Developed and simulated a transistor level I/O buffer timing model which can estimate one of the most critical product specification parameter of the latest Pentium Processor project
- Developed and designed a Noise Digital Filter with challenging specifications which can greatly improve I/O buffer performance

**UCLA High speed Electronics Lab, Los Angeles, CA, Dec 2004 - Present**

**Graduate Researcher**

- Leader of 60GHz PLL synthesizer design in 90nm
- Co – Design 10 bit 1/Gs folding interpolating BICMOS A/D convertor
- Implemented 10 bit 1G/samples high speed BiCMOS comparator with 1mV resolution
- Designed the Delay Locked Loop (DLL) operated from 500MHz to 1GHz with 10ps jitter for the whole A/D converter chip
- Responsible for design of 1GHz low voltage differential signal (LVDS) buffer

**Zero-IF receiver for 5 GHz Wireless LAN (IEEE 802.11a) Design, Winter 2005**

**UCLA Advance RF Integrated Circuit Class Project**

- Designed LNA with switchable gain from 5dB to 25dB with 50 ohm matching
- Designed 5.2GHz I/Q quadrature voltage control oscillator (VCO) with  $-105\text{dBc/Hz}$  at 100kHz offset
- Designed single balance mixer with 5dB conversion gain
- The cascade IIP3 of the front-end is about 0 dBm and 3.1dB noise figure
- Successfully implemented the design utilizing Cadence Spectra RF with 0.18um CMOS technology

**256X256 static content access memory (CAM) design, Winter 2005**

**UCLA Advance Digital Circuit Design Project**

- 16 bit input decoder design with self-timing circuit
- Design Sense Amplifier with offset consideration
- Noise simulation of the bit cell under different process corner
- Completed the whole design with 3ns access and match cycle time in 0.25um CMOS technology

**UCLA Microwave Electronics Laboratory, Los Angeles, CA, Summer 2003**

**Undergraduate Summer Researcher**

- Designed and fabricated forward coupler by using Defected Ground Structure
- Gained hands-on experience in designing and testing RF circuits

**Lawrence Berkeley National Laboratory, UC Berkeley, CA, Summer 2001**

**Undergraduate Summer Research Fellowship**

- Studies Advance Applied Electromagnetism for Accelerator and Advanced Light Source
- Used finite elements method to simulate the geometry of the coil and computed numerical magnetic field of the super-conducting magnet in C language

**Honors:**

- Made Dean's List in every quarter from Fall 01 to Spring 03

**Citizenship Status: U.S. Citizen**