

## HIGH LEVEL SPECIFICATION OF DES VERILOG MODEL

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In this homework, you will think of how a simulation of a hardware block can be accelerated. The exercise requires you to have access to and use a Verilog simulator and a C compiler. We will use only standard ANSI-C code and do developments at the UNIX command line using an editor (vi, emacs), makefiles and any other utilities you see fit of. You can use any C compiler you want for development, but the code must be tested on the gcc compiler before you turn it in.

### THE ASSIGNMENT

Alice was a very clever Verilog designer at CheapChips who had designed a DES encryption/decryption block in hardware. She has left the company since, but her DES block still is part of the IP portfolio of CheapChips. When you joined CheapChips, you have been given the responsibility over the maintenance and customer support of this block.

One of the new customers of CheapChips wants to integrate the DES block in a network processor, and is asking for a way to increase the simulation speed of this Verilog model. Obviously one way to increase simulation speed is to build a model at higher abstraction level, for example using programming in the C language. First, you must convince management that a C model can run faster on a comparative testbench than the Verilog model. So you plan to take Alice's DES block and one of the testbenches, port both of these to C, and show how fast the resulting C-model runs.

### GETTING STARTED

You can do this homework in teams of two. Find a teammate that will work with you during the EE201A projects. Follow the link on the ee201a class webpage to the projects homepage and find the package `hw1.tar` in the homework section. Upon unpacking this file, you will find the following directories

```
hw1 - verilog_code      : DES block of Alice along with testbench
    - c_skeleton        : A partially filled out c file for your solution
```

First look at the verilog code and find out what is happening. Simulate it using verilog-XL. Your goal is to recreate this simulation in a C-model, and get the resulting model to run as fast as possible the same testvectors as used in the verilog model. In the `c_skeleton` you find a file `demain.c` to help you get started. You need to code a C function

```
void des(long long *desOut, long long desIn, long long key, int decrypt)
```

that represents the DES block functionality. In the main function you put the testbench code that exercises the C function. You cannot change the existing structure in the C-program, but of course you are free to (and should!) extend it.

Questions regarding the homework should be directed to the EE201A class bulletin board. Find the link to it on the class webpage. Be sure to check the instructions – you have to log in in order to post messages.

### WHAT TO TURN IN

Due Date: 4/11/2002 at 12 o'clock noon at Letty's desk (7440 Boelter Hall).

What: 1 sheet stating the following

- The two members in your team.
- A link to your EE201A project homepage (1 per team) where the resulting C-program is posted. The program will be checked using gcc under UNIX.
- How fast is your C program compared to Verilog ?
- Give the three most important reasons why the C is faster/slower than Verilog
- Your login name on the class bulletin board. On the class bulletin board itself, post a message stating the link to your EE201A project homepage.