# Plasma-Damaged Oxide Reliability Study Correlating Both Hot-Carrier Injection and Time-Dependent Dielectric Breakdown

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***Abstract*—The oxide damage resulting from exposure to a plasma environment in four different dry-etch tools was investigated using both hot-carrier injection (HCI) and time-dependent dielectric breakdown (TDDB). A strong correlation was observed between hot-carrier injection results and time-dependent dielectric breakdown results. It was found that a damaged oxide has both a lower critical energy for HCI to create an interface trap, and a lower activation energy for Fowler–Nordheim injection to create a hole in the oxide. These results also suggest that in dry etching, possibly more damage occurs in the metal etch step than in the contact etch step.**

## I. INTRODUCTION

THE gate oxide of modern transistors continues to decrease in thickness with scaling and hence becomes more susceptible to damage. Dry etching using a plasma process is employed in VLSI processing for stringent controls on the dimensions of the patterns of device layout. Damage is known to occur in the gate oxide during plasma etching [1]–[3]. The damaged oxide becomes vulnerable to severe hot-carrier-injection (HCI) induced degradation and time-dependent dielectric breakdown (TDDB). Earlier workers have identified HCI degradation and TDDB as two major issues in evaluating device reliability [4]–[7]. In this paper, we report the results of our study on the effects of damage due to the plasma etching process on the oxide quality using HCI and TDDB measurements. The measurements indicate that a strong correlation between HCI and TDDB exists among the plasma-damaged samples. The oxide quality is shown to be related to two physical parameters: the critical energy needed to create an interface trap in HCI, and the activation energy for Fowler–Nordheim injection to create a hole in the oxide.

## II. EXPERIMENTAL

The devices used in this study are conventional LDD and nMOS transistors. The substrate material is p-type silicon with doping of $2 \times 10^{17}$ cm$^{-3}$. The 120-Å gate oxide was grown at 900°C in dry oxide atmosphere. After a 3500-Å-thick n-type poly-gate silicon was formed, phosphorus was implanted to create an LDD structure. Titanium was then deposited to form a TiSi$_2$ layer to realize a good contact. Finally, tungsten was used for metallization. The wafers were split four ways representing four different etching conditions, two for contact etch and two for metal etch as shown in Table I. The plasma etching machines were reactive ion etchers. The pressure, power, and the exposure time for each machine are also given in Table I. For hot-carrier injection measurements, devices with $L = 0.5$ $\mu$m and $W = 10$ $\mu$m were used. The stressing conditions were at intermediate gate voltages ($V_g = V_d/2$) which correspond to damage dominated by interface state generation [4]. Charge-pumping measurements were made to confirm the generation of interface states under hot-carrier stress. For time-dependent dielectric breakdown measurements, devices with $L = 1$ $\mu$m and $W = 10$ $\mu$m were used with a negative constant current injection to the gate. All the measurements were done using a HP4145B semiconductor parameter analyzer.

## III. RESULTS AND DISCUSSION

Linear region transconductance ($g_m$) for the four splits was measured as a function of gate voltage with a drain voltage of 0.1 V. It was found that samples $S1$ and $S3$ had higher peak transconductance than samples $S2$ and $S4$. Hot-carrier injection under different drain voltages ($V_d$ = 7, 6.5, 6, 5.5 V) with the gate voltage $V_g$ equal to $V_d/2$, was performed to extract lifetime $\tau$. The lifetime is defined to be the time taken for 10% change in the linear region peak transconductance. According to the model proposed by [4], it can be shown that

$$\ln(\tau I_d) \propto -\frac{\phi_{it}}{\phi_i}\ln\left(\frac{I_{sub}}{I_d}\right) \qquad (1)$$

where $\phi_{it}$ is the critical electron energy required for generating an interface trap and $\phi_i$ is the minimum energy needed for the creation of a hot electron in an impact ionization. By monitoring $I_{sub}$ and $I_d$ for different

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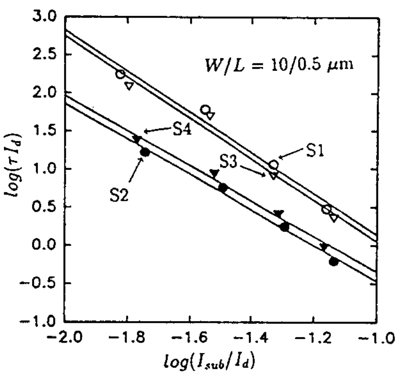

Fig. 1. *Log* $(\tau I_d)$ versus $\log(I_{sub}/I_d)$ with slope $-(\phi_{it}/\phi_i)$ for the four splits.

TABLE I
PLASMA ETCHING PROCESS CONDITIONS FOR THE FOUR SPLITS

| | Contact Etch | | Metal Etch | |
|---|---|---|---|---|
| | Machine 1 | Machine 2 | Machine 3 | Machine 4 |
| | 75 mT, 2.0 min | 50 mT, 2.2 min | 400 mT, 3.0 min | 200 mT, 2.8 min |
| split | 600 W | 425 W | 250 W | 500 W |
| $S1$ | X | | X | |
| $S2$ | X | | | X |
| $S3$ | | X | X | |
| $S4$ | | X | | X |

stress conditions, we can plot $\log(\tau I_d)$ versus $\log(I_{sub}/I_d)$ as shown in Fig. 1. The slope is equal to $-(\phi_{it}/\phi_i)$. It is seen that samples $S1$ and $S3$ have both larger lifetime and slope in comparison with samples $S2$ and $S4$.

TDDB measurements were made with different Fowler–Nordheim injection current levels. In each case the time to breakdown was measured. In Fig. 2, charge to breakdown ($Q_{bd}$) is shown as a function of injection current density $J$. We can see that samples $S1$ and $S3$ have larger $Q_{bd}$ than samples $S2$ and $S4$, which is consistent with the results from linear region transconductance measurements (not shown) and hot-carrier injection measurements (shown in Fig. 1). According to the model in [5], oxide breakdown is due to accumulated hole trapping in oxide. The charge to breakdown $Q_{bd}$ can be shown to have the following dependence:

$$\ln(Q_{bd}) \propto -\frac{H}{B}\ln(J) \qquad (2)$$

where $B = 8\pi(2m^*)^{1/2}(q\phi_B)^{3/2}/(3hq)$, $m^*$ is electron effective mass, $\phi_B$ is the barrier height, $h$ is Planck's constant, $q$ is the electron charge, and $H$ is critical electric field for hole generation in oxide. The slopes of the plots in Figs. 1 and 2 are listed in Table II. Samples $S1$ and $S3$ have larger slopes in both hot-carrier injection and TDDB plots than samples $S2$ and $S4$.

In the expression for the slope of the hot carrier injection plot (Fig. 1), the denominator, $\phi_i$, which is dependent on impact ionization process in the substrate (bulk semiconductor), is not expected to be affected by the oxide damage. On the other hand, the numerator $\phi_{it}$ is strongly dependent on the interface characteristic which is influenced by the oxide quality. Hence, a lower slope implies a lower energy required for the creation of an interface trap. Thus, it can be inferred that samples $S2$ and $S4$ are more damaged than samples $S1$ and $S3$ since a lower energy is needed to create interface traps in $S2$ and $S4$. Charge-pumping results also confirmed this inference. We found evidence of a larger interface state density in samples $S2$ and $S4$ than in samples $S1$ and $S3$.

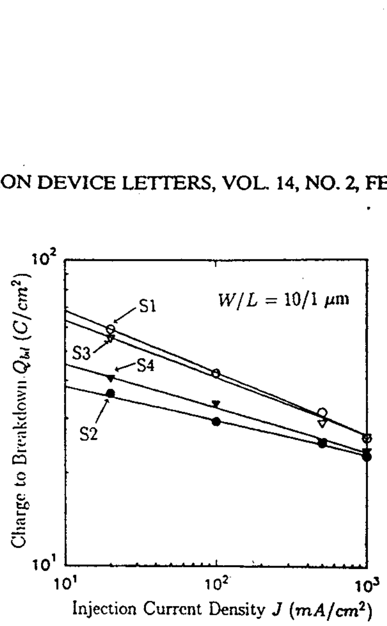

Fig. 2. Charge to breakdown $Q_{bd}$ as a function of injection current density $J$ for the four splits. Each data point is an average of several measurements.

TABLE II
THE SLOPE $(-\phi_{it}/\phi_i)$ OF HOT-CARRIER INJECTION PLOT AND THE SLOPE $(-H/B)$ OF TDDB PLOT FOR THE FOUR SPLITS

| Split | $-\phi_{it}/\phi_i$ | $-H/B$ |
|---|---|---|
| $S1$ | −2.7 | −0.20 |
| $S2$ | −2.3 | −0.11 |
| $S3$ | −2.7 | −0.19 |
| $S4$ | −2.3 | −0.14 |

The slope of the TDDB plot (Fig. 2) is equal to $-H/B$ where $B$ is determined by the barrier height between the substrate and the oxide. It can be assumed that the barrier height is not affected by the oxide damage. On the other hand, $H$ is related to the hole creation in the oxide and is therefore strongly influenced by the oxide quality. It is therefore reasonable to expect a reduced slope in damaged oxide. The oxide in samples $S2$ and $S4$ are seen to be damaged more than the oxide in samples $S1$ and $S3$ from the difference in the slope in Fig. 2. In damaged samples the time to breakdown is also shorter similar to the decrease in the slope of the plot. This observation parallels the earlier one regarding HCI results.

$S1$ and $S2$ have a contact etch different from $S3$ and $S4$. Similarly, $S1$ and $S3$ have a metal etch different from $S2$ and $S4$. Since the split at the metal etch seems to make a difference, it is reasonable to infer that the sample is more susceptible to damage in the metal etch step than in the contact etch in our processing. In a typical VLSI process, less than 10% of the wafer is exposed to the plasma during the contact etch step, while a larger portion of the wafer is exposed to the plasma during the metal etch step. This is a possible explanation why the damage seems to be more sensitive to the metal etch step.

## IV. SUMMARY

In summary, we have used both hot-carrier injection and time-dependent dielectric breakdown measurements to evaluate plasma-damaged nMOS transistors. A strong correlation is observed between HCI and TDDB results. A more heavily damaged oxide has a lower critical energy for hot-carrier injection to create an interface trap and a lower activation energy as well for Fowler–Nordheim injection to create a hole in the oxide. Finally, the results suggest that oxide damage measured by these techniques may be more severe with metal-etch step in our processing.

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