

YAN LIN

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OBJECTIVE

Full time position in 2007 on VLSI CAD algorithms and optimization

EDUCATION

University of California, Los Angeles March 2003 – Present (expected in 2007)

Ph.D. program, Electrical Engineering

M.Sc. in Electrical Engineering

March 2003 – June 2004

- Related core coursework in:
 - Graph Algorithms, CAD Algorithms, Optimization
 - VLSI Architecture, Digital Circuit Design, Computer Architecture, Embedded Systems
- Related course projects:
 - Designed a single-ported 256x64 Content Addressable Memory (CAM)
 - A High /Low-pass/Gain digital filter micro-architecture and circuit design
 - Simulated annealing based configurable sensor network deployment
 - Detailed placement for standard cell based placement

Tsinghua University, P.R.China

Sep 1998 – Jun 2002

B.S. in Department of Automation (GPA:88/100 Rank: 5/160)

PROFESSIONAL EXPERIENCE

- March 2003 – present, Graduate Student Researcher, UCLA Design Automation Lab
- June 2006 – Sept. 2006, Intern Research Engineer, Altera Corp., San Jose, CA
 - Developed various tools integrated in Quartus II for next generation FPGA architecture research
- July 2005 – Dec. 2005, Intern Research Engineer, Altera Corp., San Jose, CA
 - Evaluated various academic logic synthesis and technology mapping algorithms compared to Altera Quartus II
 - Analyzed statistical timing considering guard-banding and speed-binning with process variations
 - Developed a novel stochastic placement algorithm with 25X yield loss reduction (US Patent)
- March 2004 – June 2004, Teaching Assistant, “EE M16: Digital Logic Design”, EE Department, UCLA

RESEARCH

Power: “Novel Circuit and Fabric Design for Power Efficient FPGAs and related CAD”

- Developed low-power FPGA circuits and architectures using dual-Vdd/Vt technique and related CAD
- Developed timing slack allocation algorithms for Vdd-programmable interconnects for power reduction
- Performed FPGA architecture evaluation considering Vdd programmability
- Performed FPGA device and architecture co-optimization considering power, area and performance

Variation: “Process Variation Modeling and Variation-Aware Physical Synthesis for FPGAs”

- Developed closed-form chip-level timing and power models with process variations
- Performed FPGA architecture and device co-optimization considering variations
- Developed stochastic physical synthesis, e.g. clustering, placement, routing, retiming, and studied the interaction between them

- Developed statistical dual-Vdd assignment algorithm considering timing yield constraint
- Reliability: “Early-stage Technology Optimization for FPGA Reliability”**
- Developed efficient and accurate trace-based chip-level transient soft error rate (SER) estimator
 - Performed FPGA architecture and device co-optimization considering soft error rate
 - Ongoing work on early stage device optimization considering architecture-level delay, power and reliability including soft error rate and negative bias temperature instability (NBTI) etc

PUBLICATIONS

Journal articles

- **Yan Lin**, Fei Li and Lei He, “Circuits and Architecture Evaluation for Field Programmable Gate Array with Configurable Supply Voltage”, *IEEE Transactions on Very Large Scale Integration(VLSI) Systems*, Vol. 13, No. 9, Sept. 2005, pp. 1035-1047
- Fei Li, **Yan Lin**, Lei He, Deming Cheng and Jason Cong, “Power modeling and characteristics of field programmable gate arrays”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems*, Vol. 24, No. 11, Nov. 2005, pp. 1712-1724
- **Yan Lin** and Lei He, “Dual-Vdd Interconnect with Chip Level Time Slack Allocation for FPGA Power Reduction”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems*, Vol. 25, No. 10, Oct. 2006, pp. 2023-2034
- Fei Li, **Yan Lin** and Lei He, “Field Programmability of Supply Voltage for FPGA Power Reduction”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems*, Vol. 26, No. 4, pp. 752-764, April 2007
- Lerong Cheng, Fei Li, **Yan Lin**, Phoebe Wong and Lei He, "Device and Architecture Co-optimization for FPGA Power Reduction", accepted by *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*
- **Yan Lin**, Mike Hutton and Lei He, “Statistical Placement for FPGAs Considering Process Variation”, accepted by *IET Computers and Digital Techniques*
- **Yan Lin**, Lei He and Mike Hutton, “Stochastic Physical Synthesis Considering Pre-routing Interconnect Uncertainty and Process Variation for FPGAs”, revision submitted to *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*
- Yu Hu, **Yan Lin**, Lei He and Tim Tuan, “Physical Synthesis for FPGA Interconnect Power Reduction by Dual-Vdd Budgeting and Retiming, revision submitted to *ACM Transactions on Design Automation of Electronic Systems (TODAES)*

Conference papers

- Fei Li, **Yan Lin**, Lei He and Jason Cong, “Low-Power FPGA using Pre-Defined Dual-Vdd/Dual-Vt Fabrics”, *FPGA Symposium*, pp. 42-50, Feb 2004
- Fei Li, **Yan Lin** and Lei He, “FPGA Power Reduction Using Configurable Dual-Vdd”, *Design Automation Conference*, pp. 735-740, June 2004
- Fei Li, **Yan Lin** and Lei He, “Vdd Programmability to Reduce FPGA Interconnect Power”, *Intl. Conference on Computer Aided Design*, pp. 760-765, Nov 2004
- **Yan Lin**, Fei Li and Lei He, “Routing Track Duplication with Fine-Grained Power-Gating for FPGA Interconnect Power Reduction”, *Asia South Pacific Design Automation Conference*, pp. 645-650, January 2005

- **Yan Lin**, Fei Li and Lei He, “Power Modeling and Architecture Evaluation for FPGA with Novel Circuits for Vdd Programmability”, *FPGA Symposium*, pp. 199-207, Feb 2005
- **Yan Lin** and Lei He, “Leakage Efficient Chip-level Dual-Vdd Assignment with Time Slack Allocation for FPGA Power Reduction”, *Design Automation Conference*, pp. 720-725, June 2005
- Lerong Cheng, Phoebe Wong, Fei Li, **Yan Lin** and Lei He, “Device and Architecture Co-optimization for FPGA Power Reduction”, *Design Automation Conference*, pp. 915-920, June 2005
- Phoebe Wong, Lerong Cheng, **Yan Lin** and Lei He, “FPGA Device and Architecture Evaluation Considering Process Variation”, *Intl. Conference on Computer Aided Design*, pp. 19-24, Nov 2005
- Yu Hu, **Yan Lin**, Lei He and Tim Tuan, “Simultaneous Time Slack Budgeting and Retiming for Dual-Vdd FPGA Power Reduction”, *Design Automation Conference*, pp. 478-483, July 2006
- **Yan Lin**, Mike Hutton and Lei He, “Placement and Timing for FPGA considering Variations”, *International Conference on Field Programmable Logic and Applications*, pp. 37-43, August 2006
- **Yan Lin**, Yu Hu, Lei He and Vijay Raghunat, "An Efficient Chip-level Time Slack Allocation Algorithm for Dual-Vdd FPGA Power Reduction", *International Symposium on Low Power Electronics and Design*, pp. 168-173, October 2006
- **Yan Lin** and Lei He, “Stochastic Physical Synthesis for FPGAs with Pre-routing Interconnect Uncertainty and Process Variation”, *FPGA Symposium*, pp. 80-88, Feb 2007
- **Yan Lin** and Lei He, “Statistical Dual-Vdd Assignment for FPGA Interconnect Power Reduction”, *Design Automation and Test in Europe*, pp. 636-641, April 2007
- **Yan Lin** and Lei He, “Device and Architecture Concurrent Optimization for FPGA Transient Soft Error Rate”, accepted by *Intl. Conference on Computer Aided Design*, Nov 2007

Patents

- Mike Hutton and **Yan Lin**, “Timing-Driven Placement For On-Chip Variations”, U.S. Patent Pending

COMPUTER SKILLS

- Proficient in C/C++
- Familiar with Verilog, SpecC, MIPS, 80x86 assembly, Matlab, Perl
- Familiar with Synopsys tools, Cadence tools, VPR, HSPICE, FPGAEVA-LP2, Quartus II
- Familiar with UNIX/LINUX/WINDOWS

PERSONAL DATA

Chinese/Male/Birth date: Dec. 28th, 1980

REFERENCES

Prof. Lei He, Department of Electrical Engineering, UCLA

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Dr. Mike Hutton, Software Department, Altera Corp., San Jose CA

mhutton@altera.com, (408) 544-8253

Dr. Fei Li, Actel Corp., Mountain View, CA

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