A 40-Gb/s 9.2-mW CMOS Equalizer

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Abstract — A 40-Gb/s equalizer incorporates a one-stage CTLE with 5.5-dB boost, a one-tap discrete-time linear equalizer with 5.4-dB boost, a two-tap half-rate/quarter-rate DFE, and charge-steering techniques. Realized in 45-nm CMOS technology, the equalizer achieves BER $< 10^{-12}$ with a clock phase margin of 0.28 UI with a channel loss of 20 dB at Nyquist.

With the recent interest in 40-Gb/s WDM systems [1], low-power techniques for wireline receivers have become even more critical. This paper describes a 40-Gb/s equalizer with an efficiency of 0.23 mW/Gb/s. This performance is achieved through the use of a one-stage continuous-time linear equalizer (CTLE), a one-tap discrete-time linear equalizer (DTLE), a two-tap decision-feedback equalizer (DFE), and two new latch topologies. Since in recent designs, the CTLE draws significant power, this work introduces the DTLE as an efficient means of creating a high-frequency boost with only 0.3 mW.

Architecture Shown in Fig. 1, the overall equalizer (excluding the second DFE tap for clarity) demultiplexes D_{in}, generating half-rate streams D_{odd} and D_{even}. The demultiplexed streams are applied to their corresponding summing junctions, whose outputs drive another set of demultiplexers (DMUX_2). The resulting 10-Gb/s outputs of latches L_1-L_4 are multiplexed, weighted by a factor of β_1 (first tap coefficient) and returned to the summers. In addition, the DTLE delays D_{odd} and D_{even} by 1 UI (= 25 ps), weights their strength by a factor of α, and applies the result to the proper summer. Thus, the direct and delayed paths of D_{odd} and D_{even} in essence create a transfer function equal to $1-\alpha z^{-1}$ and hence a boost factor of $(1+\alpha)/(1-\alpha)$ with a low frequency gain of $1-\alpha$. In this design, α can be programmed from 0 to 0.3 in 15 steps, providing a maximum boost of 5.4 dB. The CTLE therefore is afforded a relaxed boost, allowing a more favorable trade-off between its boost factor and its low-frequency gain as well as reducing its power drain to 22% of that of the overall system. Correcting for precursors, the DTLE can potentially obviate the CTLE altogether in the future.

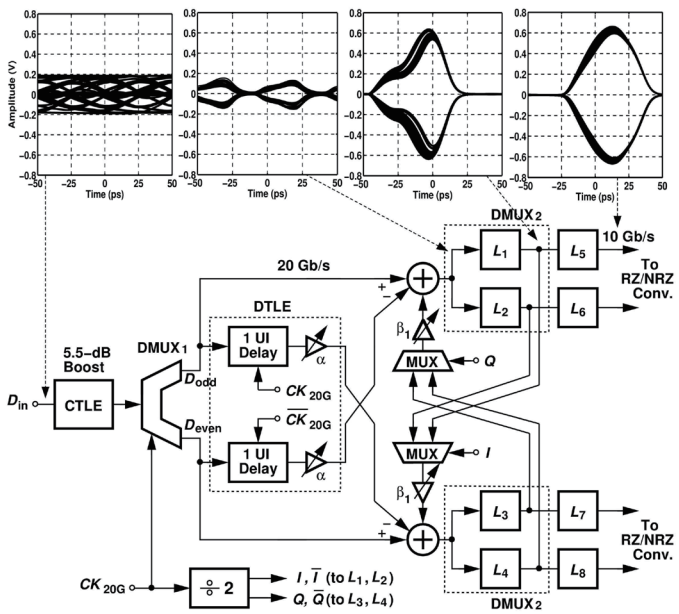


Fig. 1. Equalizer architecture.

Shown in Fig. 2 are the CTLE stage, one branch of DMUX_1,

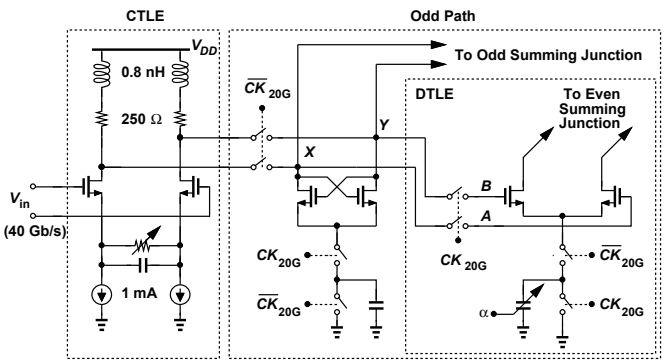


Fig. 2. Implementation of CTLE, one half-rate path, and the DTLE.

the 1-UI delay unit, and the input stage of the summer. The CTLE provides a maximum boost of 5.5 dB near Nyquist while driving the input capacitance of DMUX_1 ($\approx$ 45 fF single-ended). When CK_{20G} is low, the CTLE output is demultiplexed passively and impressed at X and Y. When CK_{20G} goes high, the regenerative pair amplifies the swing and the result is stored at A and B. After CK_{20G} falls, the differential pair is activated, drawing charge from the summing junction in proportion to α. Clocked at 20 GHz, the differential pair also produces a 1-UI delay necessary for $1-\alpha z^{-1}$. Note that without the DTLE, a second stage would need to be added to the CTLE, at least doubling its power consumption and *reducing* its bandwidth.

Latches To meet the higher speeds in this work, Fig. 3 introduces the new charge-steering implementation of L_1-L_4. In addition to the PMOS cross-coupled pair, M_7-M_8 (used for restoring the high level to V_{DD} [2]), the proposed circuit also employs two cross-coupled NMOS pairs, M_3-M_4 and M_5-M_6. The latch begins with nodes X, Y, P, and Q precharged to V_{DD} and the tail capacitors discharged to ground. When CK_{10G} goes high, M_1 and M_2 draw a differential current from X and Y, M_5-M_6 are off, and M_3-M_4 amplify $V_X - V_Y$ regeneratively. The circuit can achieve a high gain from V_{in} to V_{XY} through the use of a large tail capacitor (e.g., 100 fF)

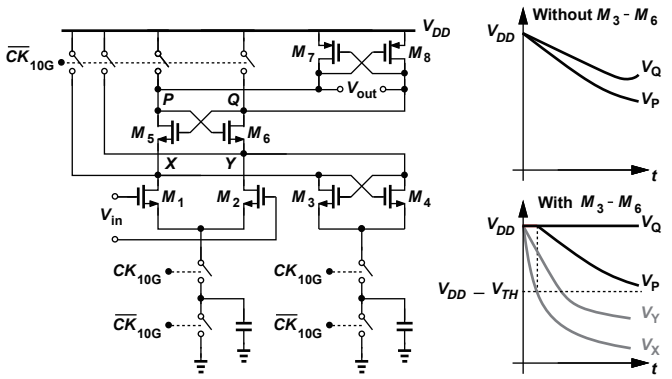
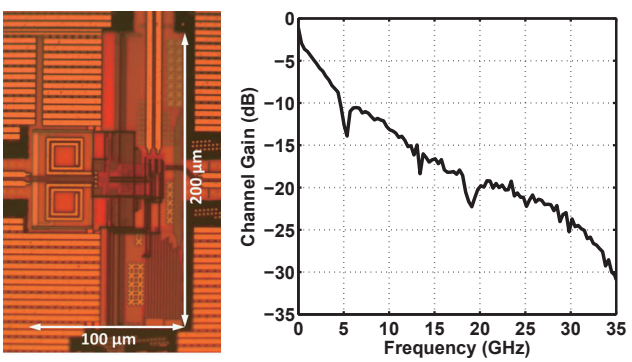


Fig. 3. Implementation of charge-steering latches L_1-L_4

but at the cost of CM degradation at the output. This issue is resolved by M_5 and M_6, which remain off until either V_X or V_Y falls to about $V_{DD} - V_{TH}$. At this point, the large voltage difference between V_X and V_Y allows only M_5 or M_6 to turn on and transfer the amplification to P or Q, minimizing the CM degradation at these nodes. That is, M_5 and M_6 isolate P and Q from the large common-mode drop inevitably imposed by the need for a high differential gain. Consequently, the latch provides 2.5 times the output swing of the topology in [2].

It is important to draw two distinctions between the topology of Fig. 3 and the StrongArm latch. (1) Our circuit operates with a finite tail charge, producing moderate (rather than rail-to-tail) swings ($\approx$ 500 mV_{pp}, single-ended) at X, Y, P and Q, improving the speed, and reducing the power consumption ($\approx$ $fCV_{DD}V_{swing}$ for each node). (2) The additional gain provided by M_3-M_4 also enhances the speed of the latch.

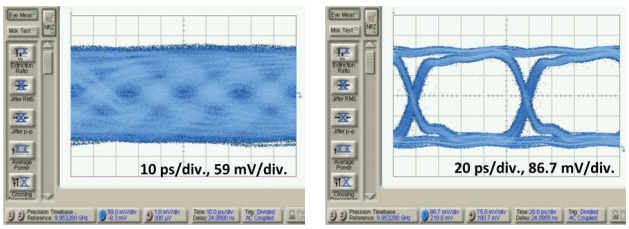
Experimental Results Figure 4(a) shows a photograph of the



(a) (b)

Fig. 4. (a) Equalizer die photograph, (b) measured frequency response of lossy channel.

die in 45-nm CMOS. The equalizer draws 9.2 mW from a 1-V supply, with 2 mW consumed by the CTLE, 3.3 mW by the DTLE + summers + latches, 0.526 mW by the RZ-NRZ conversion, and 3.4 mW by the divide-by-2 circuit. The measured results reported here are for a channel with a loss of 20 dB at 20 GHz [Fig. 4(b)]. Figure 5 shows the eye diagrams of the received 40-Gb/s data and one of the quarter-rate outputs of the equalizer. Figure 6 plots the bathtub curve for 40 Gb/s, suggesting a horizontal eye opening of 0.28 UI with a bit error rate (BER) below 10^{-12}. We should remark that the



(a) (b)

Fig. 5. Measured eye diagram of (a) equalizer input at 40 Gb/s, and (b) equalized and demultiplexed output data at 10 Gb/s.

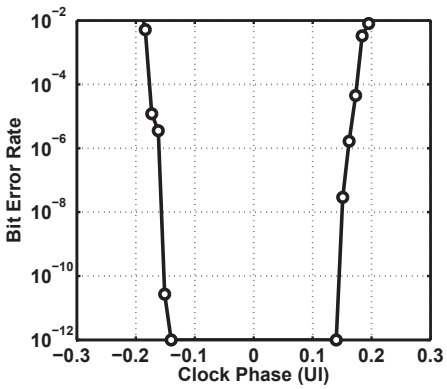


Fig. 6. Measured bathtub curve at 40 Gb/s with 20-dB channel loss.

PRBS generator output jitter is equal to 8 ps_{pp} (0.32 UI). Even though this generator and the DFE clock are mutually locked, the PRBS generator jitter substantially degrades the measured bathtub curve width. This is because the locking occurs by sharing the 10-MHz references of the generators, which creates little correlation between their jitters.

Table I summarizes the performance of state-of-the-art equalizers in the range of 32 Gb/s to 66 Gb/s.

TABLE I. Performance summary and comparison to prior art

Reference	Hsieh VLSI 2009	Toifl VLSI 2012	Lu ISSCC 2013	Manian CICC 2014	This Work
Data Rate (Gb/s)	40	32	66	32	40
Architecture	1−tap DFE	CTLE + 15−tap DFE	3−tap DFE	CTLE + 1−tap DFE	CTLE + DTLE + 2−tap DFE
DFE Clocking	Full−Rate	Quarter−Rate	Half−Rate	Full−Rate	Half−Rate/ Quarter−Rate
Channel Loss @ Nyquist	15 dB	36 dB	NA	18 dB	20 dB
BER/ Eye Opening	$<10^{-11}$/ NA	$<10^{-12}$/ 19% UI	$<10^{-12}$/ 60% UI	$<10^{-12}$/ 44% UI	$<10^{-12}$/ 28% UI
Supply (V)	1.2	1.15	1.2	0.73	1.0
Power (mW)	45	97.6	46	9.3	9.2
Power Efficiency (pJ/bit)	1.125	3.05	0.697	0.29	0.23
Area (mm^2)	0.05	0.018	0.00165	0.068	0.02
Technology	65−nm CMOS	32−nm SOI CMOS	65−nm CMOS	45−nm CMOS	45−nm CMOS

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