14.2 A 2.75Gb/s CMOS Clock Recovery Circuit with Broad Capture Range

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Use of CMOS technology for optical fiber communications creates challenges in circuit design. In particular, multi-gigaHertz clock recovery circuits require techniques coping with speed, power, and noise trade-offs. A critical issue in these circuits is the conflict between a narrow loop bandwidth imposed by optical standard jitter specifications and a broad capture range required by CMOS technology to encompass oscillator frequency variations with process and temperature. This dual-loop phase-locked architecture incorporates a digital frequency search algorithm, thereby extending the capture range by more than one order of magnitude without external references.

Figure 14.2.1 shows the architecture of the clock recovery circuit. In addition to the phase-locked loop (PLL), a frequency-locked loop (FLL) consisting of a quadrature frequency detector, a digital search algorithm, a counter, and a capacitor array controls the frequency of the voltage-controlled oscillator (VCO). The circuit begins by disabling the PLL and allowing the FLL to drive the VCO frequency within about 1.4MHz of the input data rate. The results are stored digitally and the PLL is subsequently enabled to perform phase locking. All building blocks are fully differential.

An important drawback of typical FLLs (for random data) is their limited capture range. Behavioral simulations of FLLs reported in References 1and 2 indicate a capture range of 10%-15%, a value perhaps adequate for bipolar technology but insufficient to accommodate VCO frequency variations in CMOS implementations. The FLL presented in this work overcomes this drawback. To arrive at the FLL design, first consider the average output voltage of a binary quadrature frequency detector [2] as a function of the difference between the data and clock rates, depicted in Figure 14.2.2a. In the near-lock region, where the clock frequency is within the capture range of the FD, the dc content is large enough to reliably signify the polarity of the frequency difference. However, in the far-from-lock regions, the output carries little information. In this work, the VCO frequency is set to its minimum value and stepped up with adequate resolution until Δf enters the near-lock region and subsequently changes polarity.

The FLL operation is illustrated conceptually in Figure 14.2.2. A counter controlling the capacitor array sets the VCO frequency to the lowest value. Under this condition, Δf is negative and V_{FD} is close to zero. Thus the two comparators generate logical zeros, the signal D_{stop} remains low, and the counter continues to count up (with the aid of a slow external clock) until V_{FD} drops below V_L. This is an indication that V_{FD} has reached a reliable level. Now the two flipflops begin to save each state before the next count is carried out. The counter continues to count until Δf crosses zero and V_{FD} jumps from negative to positive. The two flipflops then record this change, disabling the counter and enabling the PLL.

The frequency resolution provided by the FLL is primarily determined by the capacitor array. With a tuning range of 350MHz and 8b resolution, the minimum frequency step is about 1.37MHz, accommodating a PLL capture range of a few megahertz. The FLL also allows a small VCO gain, K_{VCO}, thus minimizing the jitter resulting from ripple on the control voltage. This is particularly important at low supply voltages because, to obtain a given relative tuning range, K_{VCO} must increase as the supply decreases. In this design, K_{VCO} is 50MHz/V.

The VCO core consists of two LC oscillators coupled to operate in quadrature (Figure 14.2.3a). The continuous frequency tuning is by varying the tail current in the coupling differential pairs [3]. To maintain relatively constant VCO gain across the tuning range, input voltage-to-current converter, M_1-M_2, incorporates linearization devices M_3 and M_4 [4]. An important advantage of this tuning technique over a varactor-based method is that the control voltage is fully differential.

The capacitor arrays added to the tanks in each VCO (Figure 14.2.3b) entail several design issues. First, the resolution of the array determines how close the frequency can come to the desired value. The resolution is limited by capacitor mismatch, parasitic capacitance in routing, and bottom-plate capacitance. In this work, a resolution of 8b is chosen, comprising a 4b segmented section containing 16 equal capacitors and a 4b binary-weighted section. This combination generates monotonicity even in the presence of 12.5% capacitor mismatch. The second issue relates to the on-resistance of the switches in series with the capacitors. This resistance is chosen to yield a capacitor Q of ten at the oscillation frequency.

The phase detector is similar to that in Reference 5, modified to equalize delays in the inputs of the two exclusive-OR gates. The charge pump implementation is shown in Figure 14.2.4. Since the circuit must provide a differential control for the VCO, it is important that the outputs not droop in the absence of up and down pulses. For this reason, the charge pump turns off all the devices connected to the output nodes when both up and down pulses are low. The common-mode feedback (CMFB) network senses the average differential output, adjusting the on-resistance of M_{c1} and M_{c2}. Since this approach results in substantial process and temperature variability, transistor M_{c3}, sensing the desired voltage V_{CM}, and the diode-connected device M_{b3} control the gate of $Mb_{1,2}$ [6]. With reasonable matching, the output CM level remains close to V_{CM}.

The clock recovery circuit in digital 0.25μm CMOS is shown in Figure 14.2.7. The die has 0.9x0.6mm² active area. Figures 14.2.5 and 14.2.6 show the recovered clock and the jitter histogram in response to a 2.75Gb/s PRBS of length 2^{23}-1. The rms and peak-to-peak jitters are 5.1ps and 35.8ps, respectively. The output spectrum of the recovered clock depicts -89.2dBc/Hz phase noise at 1MHz offset. The capture range is 350MHz and the tracking range, determined by the fine-tuning range, is 45MHz. The circuit operates reliably at data rates to 3Gb/s. Total power dissipation is 50mW from 2.7V power supply.

Acknowledgments:
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References:

[1] L. De Vito, et. al., "A 52MHz and 155MHz Clock –Recovery PLL," ISSCC Digest of Technical Papers, pp. 142-143, Feb. 1991.
[2] A. Pottbaker, U. Langman, H. Schreiber, "A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s," IEEE JSSC, vol. SC-27, pp. 1747-1751, Dec. 1992.
[3] T. P. Liu, "A 6.5GHz Monolithic CMOS Voltage-Controlled Oscillator," ISSCC Digest of Technical Papers, pp. 404-405, Feb. 1999.
[4] F. Krummenacher, N Joehl, "A 4-MHZ CMOS Continuous-Time Filter with On-chip Automatic Tuning," IEEE JSSC, vol. 23, pp. 750-758, June 1988.
[5] C. Hogge, "A Self Correcting Clock Recovery Circuit," IEEE J. of Lightwave Technology, vol. LT-3, pp. 1312-1314, Dec. 1985.
[6] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.

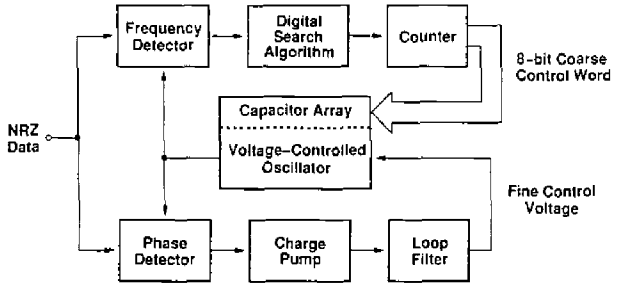

Figure 14.2.1: Clock recovery architecture.

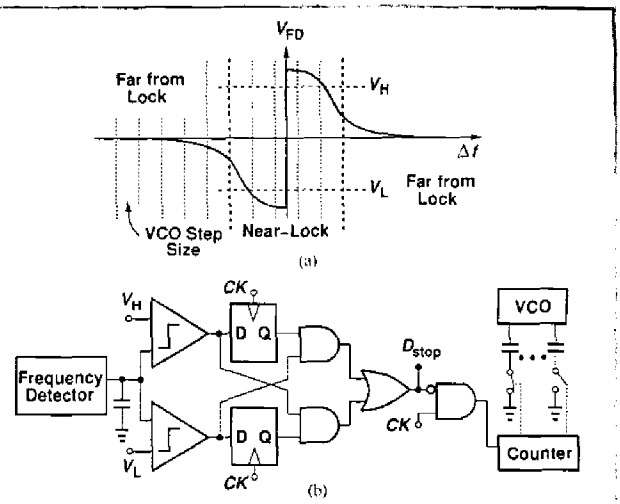

Figure 14.2.2: Conceptual illustration of digital search algorithm, (b) hardware implementation.

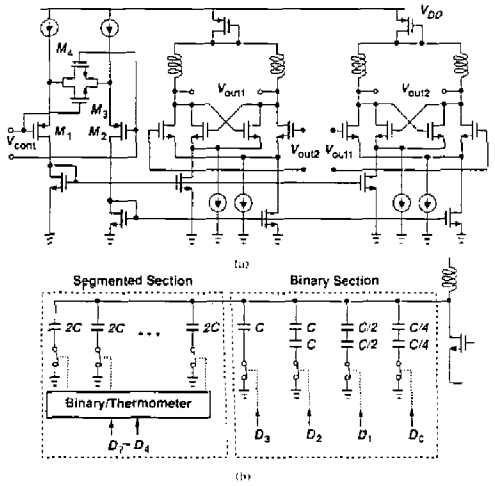

Figure 14.2.3: (a) Quadrature coupled LC oscillator; (b) capacitor array for LC tank.

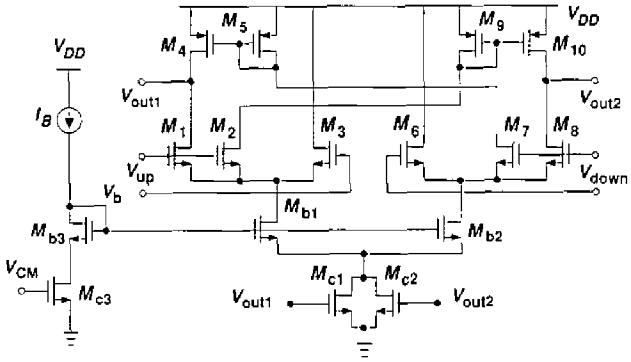

Figure 14.2.4: Implementation of charge pump.

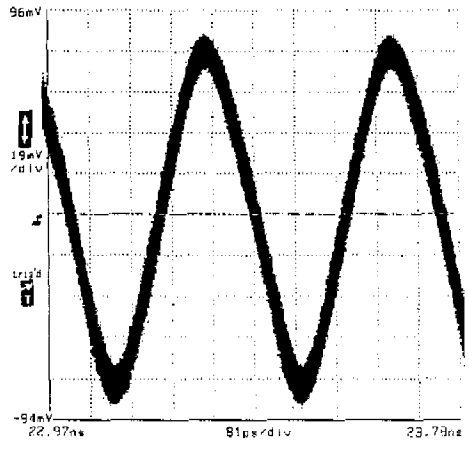

Figure 14.2.5: Recovered clock at 2.75GHz.

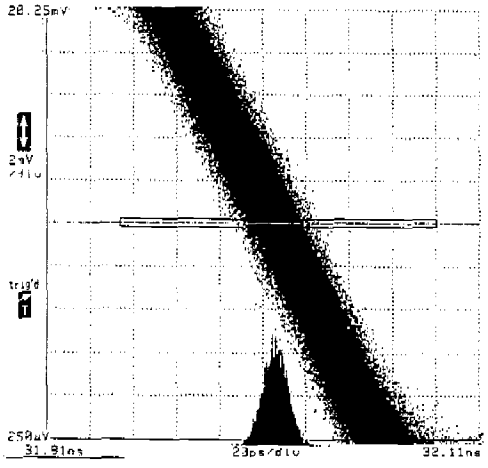

Figure 14.2.6: Jitter histrogram for PRBS of 2^{23}-1.

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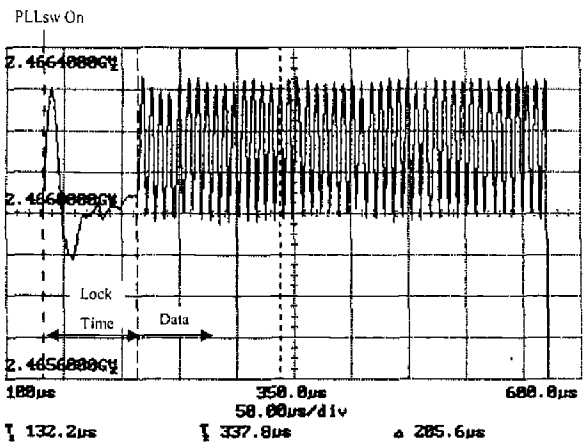

Figure 13.6.6: Measured output frequency of all TX blocks operation for 00001111pattern.

PA	Linear Gain	10.0dB
	Output Power	0.0dBm
LNA	Small Signal Gain	15.6dB
	Noise Figure	3.6dB
	Input-Referred IP3	-9.0dBm
IRM	Conversion Gain	10.8dB
	Noise Figure	24dB
	Input-Referred IP3	-8.5dBm
	Image Rejection Ratio	31dB
BPF	Rejection Ratio@1MHz offset	24dB
	Rejection Ratio@2MHz offset	60dB
Limitter/ RSSI	Input Sensitivity	-74dBm
	Dynamic Range of RSSI	> 40dB
Demodulator	Input Frequency Range	> 400kHz
LPF	Rejection Ratio@1MHz offset	27dB
PLL with Freq. Doubler and VCO	Lock Time	< 120µs
	Frequency Range	2.4~2.5GHz
	VCO Current Consumption	4.5mA
	Current Consumption	20.1mA
Total (Including PLL)	Current in Transmit Mode	34.4mA
	Current in Receive Mode	44.0mA
	Current in Sleep Mode	< 1µA
	Supply Voltage	2.7~3.3V

Figure 13.6.7: Measurement results for the transceiver.

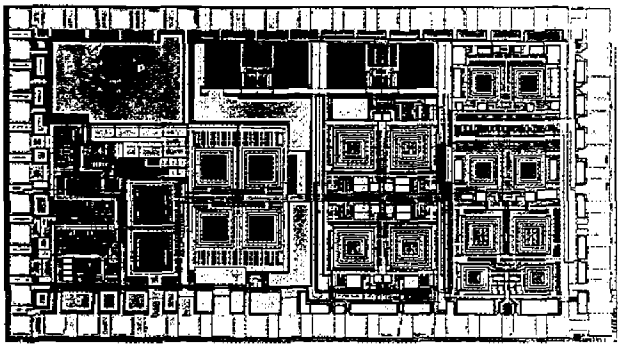

Figure 13.7.7: Die micrograph of the receiver.

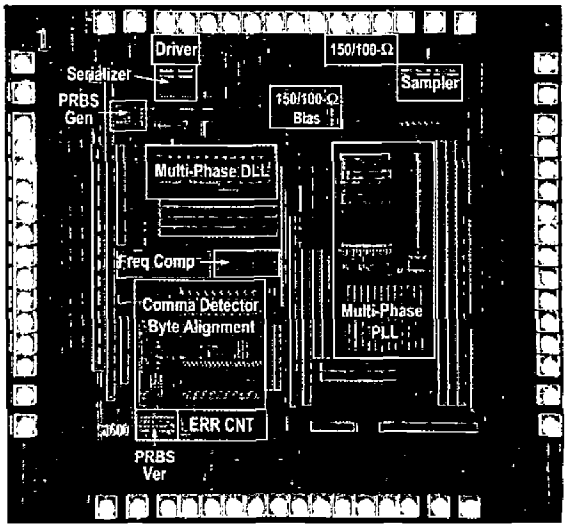

Figure 14.1.6: Chip micrograph.

Process		0.25 µm N-well 4-metal CMOS process
Supply voltage		2.5V (core), 3.3V (I/O)
DLL frequency range		30 - 250MHz
Data rate range		0.6 - 2.5GBaud
Area	Total	4.9 mm²
	DLL	0.1 mm²
	PLL	0.36 mm²
Power dissipation	Total	57.5 (mW / GBaud) × Data rate + 125.5 (mW) (197mW @ 1.25GBaud, 269mW @ 2.5GBaud)
	DLL	16.8mW @ 1.25GBaud
	PLL	29.4mW @ 1.25GBaud (6.6mW for VCO only)
Accumulated Jitter (with link activated) (@ 1.87 GBaud)	Tx data	7.3ps RMS / 46ps pk-to-pk
	DLL	6.0ps RMS / 40ps pk-to-pk
	PLL	5.5ps RMS / 35ps pk-to-pk (locked to ref-clk)
BER		$< 10^{-12}$ with a 10m 150Ω STP cable @ 2.5GBaud $< 10^{-12}$ with a 25m 150Ω STP cable @ 1.25GBaud

Table 14.1.1: Performance characteristics of prototype chip.

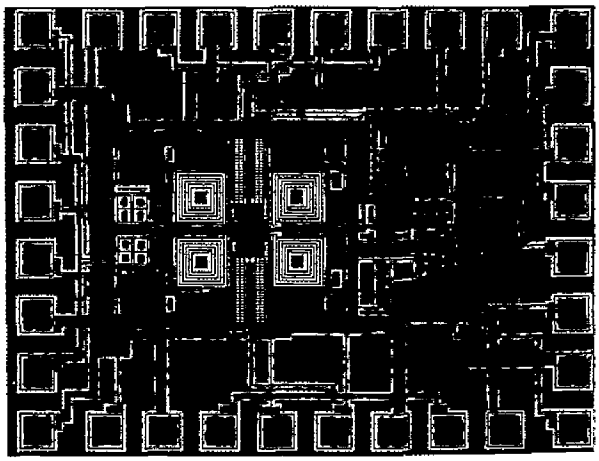

Figure 14.2.7: Die micrograph.