# The Role of Translational Circuits in RF Receiver Design

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## Abstract

**This paper provides an overview of translational or commutated circuits and their role in RF receivers. Insights are offered into the frequency translation of impedances, their modeling, and their application in input matching, blocker rejection, and channel selection. A new front end is also described that rejects blockers at the third harmonic of the local oscillator frequency.**

## I. Introduction

In the past 10 years, tremendous progress has been made in the area of RF receivers. Driven by such factors as cost, power consumption, and proliferation of wireless standards, RF designers have continually exploited CMOS integration and new circuit techniques to push the performance envelope of receivers. This paper provides an overview of recent receiver design efforts, focusing, for the sake of depth, on examples that employ translational circuits. Such circuits have created a new paradigm in RF design, helping to avoid external filters and realize compact, low-power receivers.

Section II deals with the properties of translational circuits, particularly, commutated impedances. Sections III and IV review the use of translation in input matching and blocker rejection, respectively. Section V is concerned with channel selection and Section VI presents a new harmonic-rejecting commutated front end.

## II. Translational Circuits

In this paper, we deal with a class of receivers exploiting translational circuits, an example of which are $N$-path filters. Such circuits have overcome two serious difficulties in RF design: they can realize RF transfer functions with a precise center frequency, and, by virtue of frequency translation, they can provide arbitrarily high quality factors. It is important to recognize the significance of these two attributes; the only non-translational filters exhibiting a similar behavior are SAW (or crystal) devices but with a fixed center frequency and a $Q$ that trades with the insertion loss.

Transfer functions and impedances can be translated in frequency by means of mixing or other frequency conversion methods. The idea can be traced back to "signal scanning" or "commutated" networks introduced in the late 1940s [1] and early 1950s [2, 3]. It was proposed that $N$ capacitors scanning a signal path periodically synthesize a comb filter. Shown in Fig. 1, the implementation employs $N$ non-overlapping

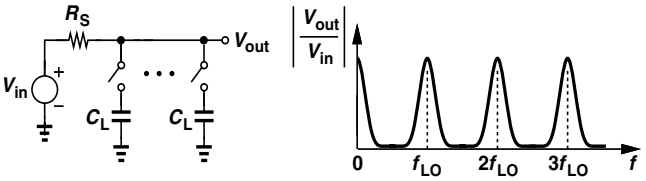


Fig. 1. Comb filter based on impedance translation.

LO phases, yielding a two-sided $-3$-dB bandwidth of approximately $1/(\pi N R_S C_L)$ around each peak if $R_S C_L$ is much grater than the on-time [2]. The center frequency is precise and the $Q$ can be arbitrarily high if $N R_S C_L$ is arbitrarily large.

An elegant and exact analysis of "commutated" impedances was presented by Smith in 1953 [3]. Suppose, as shown in Fig. 2(a), $N$ equal impedances are switched to the input under

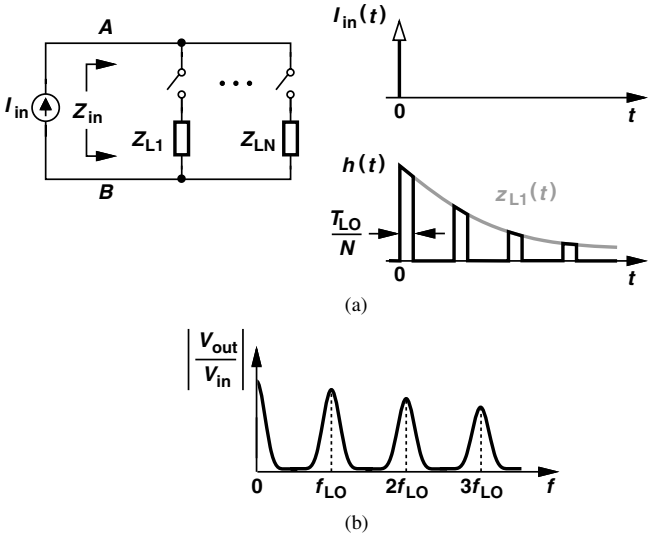


Fig. 2. (a) Example of commutated impedances and their current impulse response, and (b) resulting response translations.

the command of $N$ non-overlapping LO phases. To determine $Z_{in}$, we first compute the impulse response. If an impulse of current is applied to the circuit at $t = 0$ while all $Z_L$'s have a zero initial condition, then the voltage across $Z_{L1}$ is the impulse response, $z_{L1}(t)$, but $V_{in}$ scans this voltage only at multiples of $T_{LO}$ and for a duration of $T_{LO}/N$ seconds. In other words, $V_{in}$ is equal to the load impulse response, $z_{L1}(t)$, multiplied by a train of pulses with a width of $T_{LO}/N$. In the frequency domain, therefore, $Z_{L1}(f)$ is convolved with the Fourier transform of these pulses [Fig. 2(b)].

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The foregoing concepts can be more generally illustrated as shown in Fig. 3(a) [4], where input $X$ is downconverted,

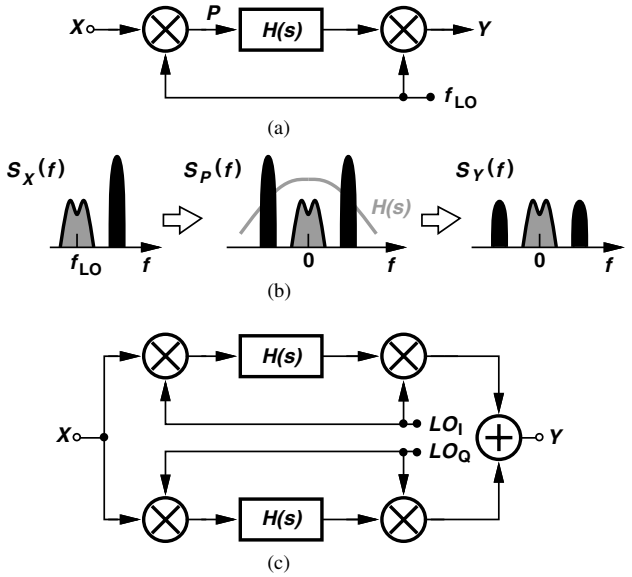



Fig. 3. (a) Translational circuit model, (b) modeling error in presence of asymmetric spectrum, and (c) accurate model.

applied to a transfer function $H(s)$, and subsequently upconverted to produce $Y$. The transfer function from $X$ to $Y$ is thus equal to $H(s - 2\pi f_{LO})$. In the circuit of Fig. 1, for example, the switches perform downconversion, applying the results to the capacitors and generating displacement currents. These currents are then upconverted by the same switches and flow through $R_S$, producing a bandpass output.

The above model proves incomplete if $X$ has an asymmetric spectrum. Consider, for example, the scenario depicted in Fig. 3(b), where $S_X(f)$ contains a desired channel centered around $f_{LO}$ and an interferer on one side. The downward translation by $f_{LO}$ places the interferer on both sides of the channel and the upward translation retains the two-sided interference. In other words, $S_Y(f) \neq S_X(f)H(s-2\pi f_{LO})$. Similarly, if the desired signal itself has an asymmetric spectrum, the downconversion corrupts each sideband by the other, an effect that is not undone by the upconversion. These issues are resolved by quadrature frequency translation [Fig. 3(c)].

Translational circuits can be even more generally envisioned as shown in Fig. 4(a), where mixing is replaced by any frequency conversion method. A familiar example are phase-locked loops [Fig. 4(b)], which downconvert by mixing and upconvert by frequency modulation, thereby creating an arbitrarily narrow bandwidth around the carrier.

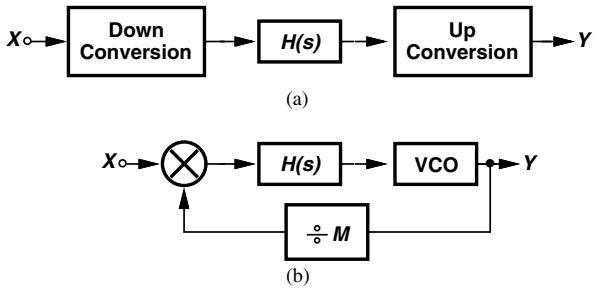



Fig. 4. (a) General model of translational circuits, (b) example showing a PLL.

## III. Input Matching by Translation

One important application of translational circuits is to establish, at blocker frequencies, a low impedance at the LNA output by means of commutated impedances. Shown in Fig. 5(a) [5, 6], such an arrangement minimizes the voltage swings

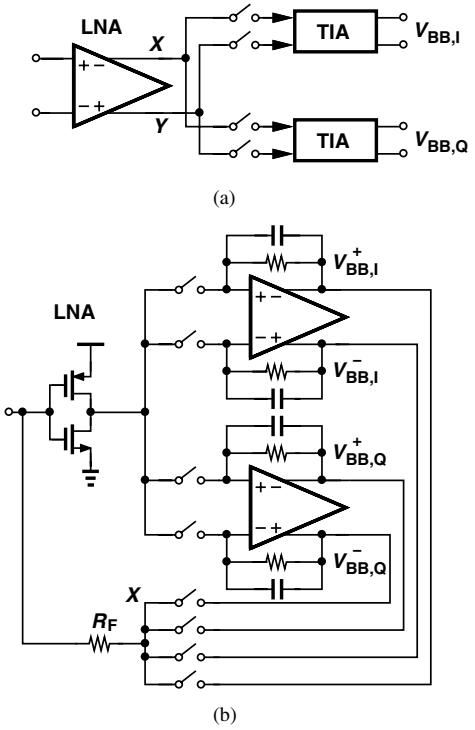



Fig. 5. (a) LNA with low load impedance, and (b) use of translational feedback to create input matching.

at the LNA output, experiencing compression only at the *input* of the LNA. Unfortunately, due to the virtual ground at $X$ and $Y$, this topology does not lend itself to broadband input matching by resistive feedback around the LNA; hence the need for inductive degeneration [5] or a common-gate stage [6].

Interestingly, it is possible to apply resistive feedback to the input through the use of a translational loop. Illustrated in Fig. 5(b) [7], the idea is to upconvert and sum the baseband $I$ and $Q$ components and return the resulting RF signal to the LNA input through a resistor. If the total voltage gain from the input to $X$ is equal to $-A_v$, then the input resistance at the LO frequency is equal to $R_F/(1 + A_v)$.

It can be proved that the overall noise figure is unaffected by the feedback if the upconversion mixer and $R_F$ contribute negligible noise. The stability of the loop is guaranteed by ensuring that the baseband transimpedance amplifiers produce a dominant pole [7].

An alternative approach employs a multi-stage feedback LNA with low impedance levels at each port [8]. Shown in Fig. 6, the circuit generates approximately differential signals

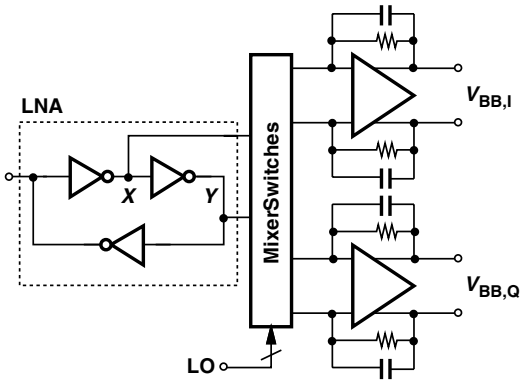



Fig. 6. LNA with low-impedance loads and feedback to create input matching.

at $X$ and $Y$ while the feedback loop within the LNA establishes input matching. This receiver achieves a noise figure of 3.8 dB at 2 GHz while drawing 15 mW [8].

In applications demanding moderate noise figures (e.g., 6 to 8 dB), one can consider eliminating the LNA and applying the received signal directly to quadrature mixers. This approach, however, must deal with the issue of input matching. Since inductive degeneration and common-gate topologies are not attractive, we ask, can a commutated network provide input matching with acceptable noise figure?

Figure 7 depicts an example, where the baseband resistance

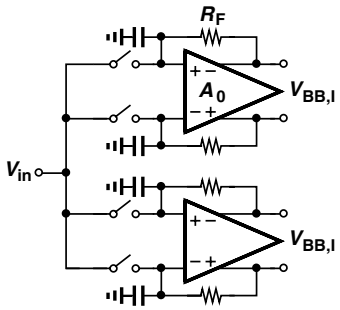



Fig. 7. Receiver front end using baseband impedance translation to create input matching.

produced by the TIAs, $R_F/(1+A_0)$, is used to create input matching [9]. This occurs if $R_F/(1+A_0)$ is chosen roughly equal to $4\pi^2 R_S/(16-\pi^2) \approx 6.4R_S$, where $R_S = 50$ . To minimize the noise figure, both $R_F$ and $A_0$ must be maximized, and the switch resistance, $R_{sw}$, must be minimized. However, to drive the wide mixer switches at 2.4 GHz, the LO phase generation circuitry in [9] consumes 40 mW. The receiver provides a noise figure of 10 dB at 2.4 GHz while drawing 70 mW [9].

It is possible to create input matching even if the mixing switches are loaded by only capacitors. This can be seen by the four-path, differential model shown in Fig. 8(a), where $Z_S$ denotes a general source impedance. It can be proved that, in the vicinity of the LO frequency, the circuit simplifies to that in Fig. 8(b), revealing that frequency-translated copies of $Z_S$ appear *in parallel*. If $Z_S$ is real and has a value of $R_S$, then matching occurs provided that $I_{in}$ sees a resistance equal to $R_S/2$. Unfortunately, in this case the net resistance shunting $Z_S$ is given by $8R_S/(\pi^2-8) \approx 4.3R_S$, failing to provide matching. On the other hand, if $Z_S$ is a *bandpass* impedance,

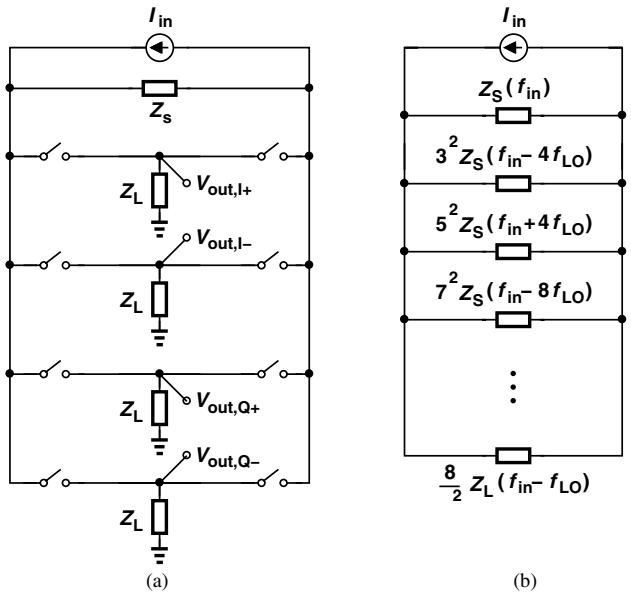



Fig. 8. (a) Model of a quadrature downconverter with 25% LO duty cycle, (b) equivalent circuit for input impedance calculation.

then $I_{in}$ can see $R_S/2$.

The equivalent circuit of Fig. 8(b) suggests that not only the load impedance but also the *source* impedance is translated in frequency. Thus, depending on the nature of $Z_S$ and $Z_L$, interesting scenarios can arise. For example, $Z_S$ can be real, a narrowband resonant circuit, or a wideband resonant circuit.

The foregoing observations lead to the "passive-LNA" front end shown in Fig. 9(a) [10]. Here, a transformer provides volt-

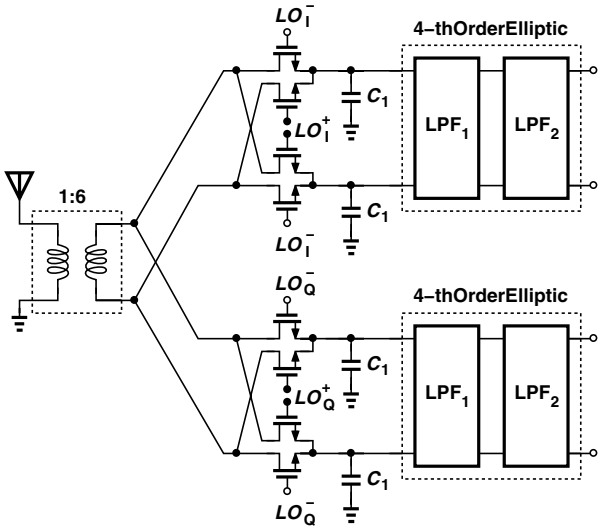



Fig. 9. 5-GHz receiver using transformer as LNA.

age gain while allowing matching as a result of its bandpass response. In addition to offering ESD protection and differential outputs, the transformer serves two other critical purposes: (1) raising the source impedance seen by the mixers, it permits the use of smaller switches and hence a power consumption of 1.6 mW in the LO phase generation circuit at 5 GHz, and (2) it reduces the effect of the baseband filters' noise, saving considerable power. This receiver achieves a noise figure of 6

dB at 5 GHz while providing channel-selection filtering in the baseband.

## IV. Blocker Rejection

The high-$Q$ filtering afforded by translational circuits is particularly attractive for the suppression of blockers. Figure 10 depicts an example [11], where the bottom path downconverts,

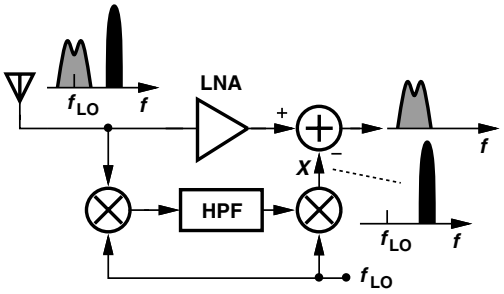



Fig. 10. Blocker-tolerant receiver using translational feedforward.

high-pass filters, and upconverts the received signals, reproducing the blocker at $X$ without the desired channel. Subtracting this result from the LNA output suppresses the blocker. To avoid corrupting the signal by itself, the translational path must utilize quadrature downconversion and upconversion [11].

The gain and phase mismatches between the two paths in Fig. 10 and quadrature imbalances within the translational path degrade the rejection to some extent. More importantly, both paths must handle large blockers with minimal compression. For this reason, [11] employs a differential LNA with an external balun, reducing the single-ended signal swing by 6 dB, and also attenuates the signal applied to the bottom path by 12 dB. Moreover, the translational path raises the overall noise figure from 3.9 dB to 6.8 dB while drawing an additional supply current of 21 mA.

If attached in parallel to the signal path, commutated networks can provide a high impedance in the desired channel and a low impedance at blocker frequencies, thereby attenuating the blockers. Let us return to the topology shown in Fig. 1 and determine how much blocker rejection the circuit can provide. It appears that an arbitrarily large $C_L$ yields an arbitrarily amount of rejection at a given offset frequency, but the finite resistance of the switches limits the performance. Redrawing the circuit as shown in Fig. 11, where $R_{sw}$ is factored out, we observe that the far-out rejection is roughly given by $R_{sw}/(R_{sw} + R_S)$.

An example of this approach is illustrated in Fig. 12 [12]. Here, two commutated networks are tied to the input of the LNA and to the cascode nodes, in essence creating a second-order roll-off for blockers. Fighting the low resistance levels at these ports, the $N$-path circuits must employ wide switches. With the aid of these two networks and $N$-path filters at the output, the receiver exhibits a channel bandwidth of 14 MHz and a noise figure of 11.4 dB in the presence of a 0-dBm blocker at 80-MHz offset.

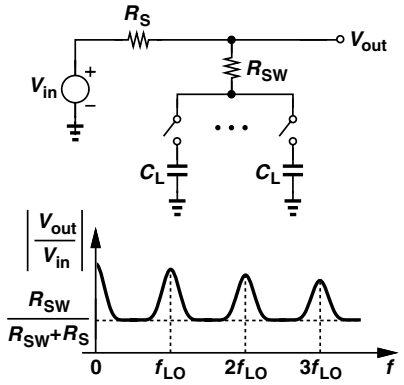



Fig. 11. Commutated circuit showing effect of switch on-resistance.

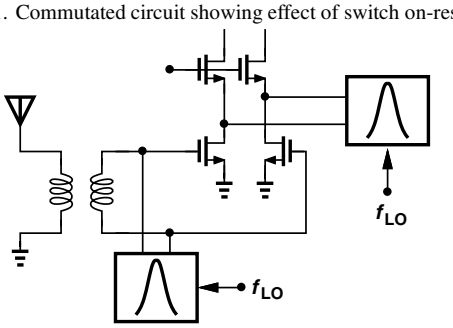



Fig. 12. Blocker-tolerant RX front end using translated impedances.

## V. RF Channel Selection

Channel selection filtering at RF, specifically at the LNA input, holds numerous attractions:

(1) It can suppress large far-out blockers, thereby eliminating the front-end SAW filters that are commonly used for multiple bands and/or relaxing the linearity required of the LNA and the mixers.

(2) It can also attenuate close-in interferers, allowing higher nonlinearity in the *entire* receive chain. These two properties are distinctly different: tolerance to large blockers (as in [12]) does not necessarily provide channel selection, and, conversely, small-signal narrow-band filtering is not necessarily linear enough to reject large blockers.

(3) Channel selection at the LNA input can ease the LO phase noise requirements: if the various switches used in the front-end commutated circuits see only attenuated blockers, then the tolerable phase noise to avoid reciprocal mixing is proportionally relaxed.

(4) If close-in AM blockers are also suppressed, then the necessary $IP_2$ values fall, obviating the need for differential front ends and hence baluns.

Channel selection at RF faces three principal challenges. First, fighting the low impedance of the antenna, the filter must incorporate very large capacitors for narrow channels, occupying substantial area. Second, the capacitors can introduce significant parasitics in the RF signal path, degrading the gain, input matching, and noise figure. Third, in the presence of a large blocker (e.g., with 0-dBm power as in GSM), the front end may experience nonlinearity, providing less or no channel selection.

An example of channel selection filtering by means of trans-

lational circuits is shown in Fig. 13 [13]. Here, the down-

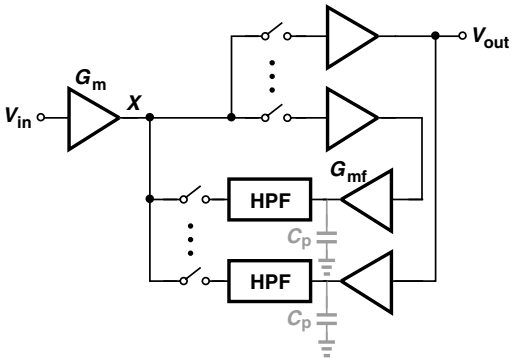



Fig. 13. Receiver using translational feedback loop to provide channel selection.

converted signal is amplified, converted to current, applied to a high-pass filter, and upconverted, thus creating a $-3$-dB bandwidth of 5 MHz at node $X$. Due to the large parasitic capacitance, $C_p$, of the high-pass filter (HPF), the receiver potentially experiences instability and must consume 62 mW [13] to place the pole at sufficiently high frequencies. Moreover, in the presence of a large blocker, the baseband amplifiers may compress, yielding less selectivity than the small-signal measurements indicate.

### A. Translational Notch Filter

The receiver design described below incorporates a passive translational notch filter. We develop in this section such a filter from first principles.

Consider the transformation depicted in Fig. 14(a), where the capacitor in a low-pass filter is replaced with commutated capacitors. As a result, the baseband frequency response is transformed to its bandpass counterpart. If $R_1C_1 \gg T_{on}$ (the on-time of the switches), then the output voltage contains a harmonically-rich signal and the translated response has a reasonable magnitude. On the other hand, if $R_1C_1 \ll T_{on}$, the output closely resembles the input, exhibiting only a small fraction of the translated response.

Let us now apply the above concepts to the high-pass section shown in Fig. 14(b), obtaining a *notch* response centered around $f_{LO}$. This topology was originally published by Smith in 1953 [3] and recently by Ghaffari et al [14]. Smith derives the notch bandwidth as $1/(\pi N R_1 C_1)$, but another important parameter is the on-resistance of the switches, $R_{sw}$. As evident from Fig. 14(c), $R_{sw}$ limits the magnitude of the response to $R_1/(R_1 + R_{sw})$ at high offset frequencies, demanding wide switches and hence a high power dissipation in the LO phase generation circuit.

### B. Channel Selection by Miller Notch Filter

It is possible to place an RF notch filter around an LNA so as to provide stronger feedback—and hence greater rejection—at higher offset frequencies [15]. Illustrated in Fig. 15(a), such a topology employs switches on *both* sides of the commutated capacitors, upconverting their parasitic, $C_p$, which would

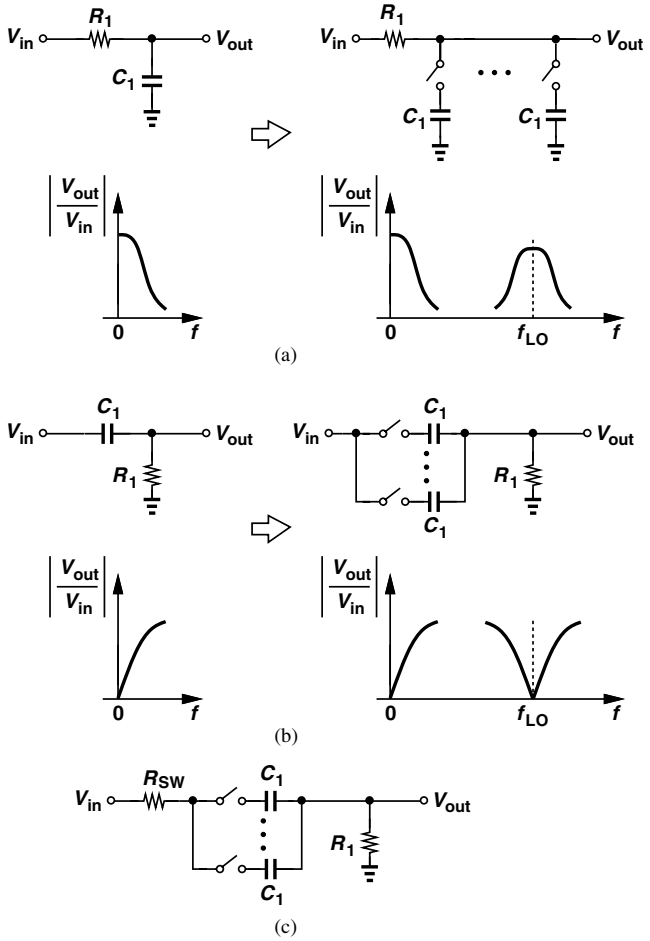
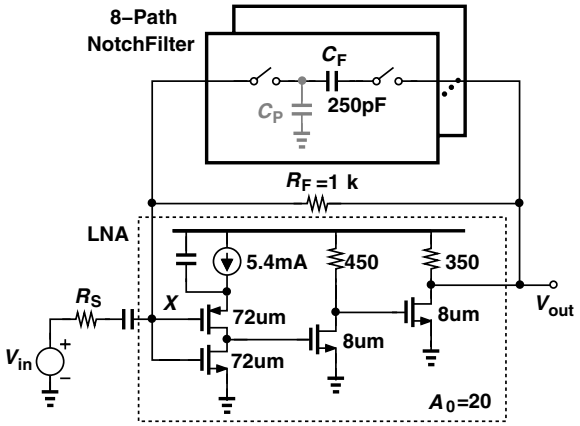



Fig. 14. (a) Translation from a low-pass response, (b) translation from a high-pass response, and (c) effect of switch resistance on the latter.

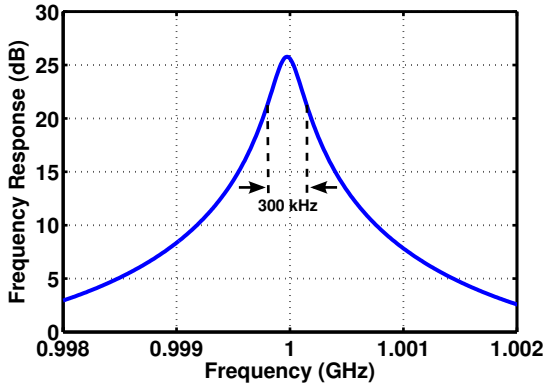
otherwise heavily load the RF input. In addition, $R_F$ establishes input matching. We call this arrangement the "Miller notch filter" [15] and point out two of its advantages: (1) the equivalent (translated) capacitance seen at the input is equal to $(1+A_0)C_F$, saving area, and (2) the resistance of the switches falls by a factor of $1 + A_0$, improving the out-of-channel rejection. Figure 15(b) plots the simulated frequency response of the circuit with eight commutated capacitors, each of value 250 pF, and $A_0 = 20$. A $-3$-dB bandwidth of 300 kHz is obtained with more than 25 dB of far-out rejection and a total capacitance of 2 nF.

The Miller notch filter deals with two of the challenges mentioned above, namely, it reduces the capacitor area by a factor of $1 + A_0$ and avoids large parasitics in the RF path. The circuit nonetheless faces difficulty in the presence of a 0-dBm blocker. If at the blocker frequency, the LNA input acts as a virtual ground, then the large blocker current ($= 632\,\text{mV}_0/50 \quad = 12.64\,\text{mA}_\text{p}$) must flow through the feedback network and be absorbed by the last stage of the LNA. This current level, however, is far too high for this stage. Consequently, the LNA input sees large swings, the last two stages saturate, the equivalent loop gain falls dramatically, and the noise figure rises from 2.1 dB to 12 dB.

We now seek a means of attenuating the blocker before it reaches the last two stages of the LNA. To this end, we add a

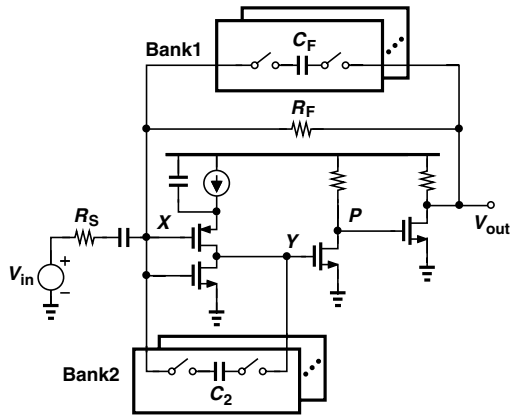



(a)

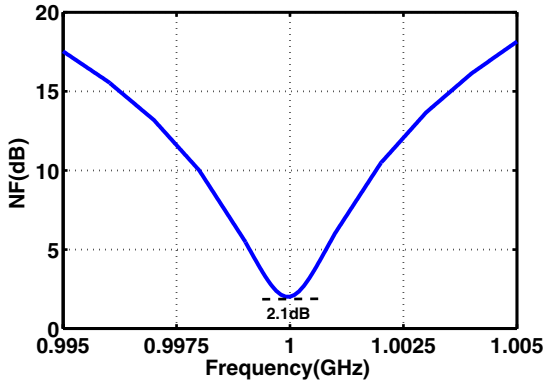



(b)

Fig. 15. (a) Use of double-switch translated notch filter in feedback around LNA, (b) resulting frequency response.




(a)




(b)

Fig. 16. (a) Addition of local notch filter to avoid compression of LNA, simulated noise figure in presence of 0-dBm blocker at 20-MHz offset.

local Miller notch filter around the first stage as shown in Fig. 16(a) [15] and reallocate some of the 2-nF total capacitance from Bank 1 to Bank 2. With $C_F = 50$ pF and $C_2 = 100$ pF, the NF does not degrade within the desired channel [Fig. 16(b)], but the reallocation increases the $-3$-dB bandwidth to 420 kHz because Bank 2 experiences less Miller multiplication.

### C. Unilateral Miller Notch Filter

It is generally possible to boost Miller multiplication by inserting an amplifier in the feedback path. This idea can be applied to the translational notch filter as depicted in Fig. 17(a), where Bank 3 employs $A_1$ so as to present a translated input capacitance of $(1 + A_1A_0)C_M$. Owing to this boost, the total capacitance necessary for a bandwidth of 200 kHz falls from 2 nF to 1.3 nF. While even a higher $A_1$ is desirable, this gain is bounded by the compression of this amplifier in the presence of a 0-dBm blocker at the main input. It can be shown that the noise of $A_1$ sees a high-pass transfer function as it travels to the output and is greatly suppressed. Also, the stability of the loop is guaranteed because Bank 1 dominates the feedback by virtue of its much smaller phase shift than that of Bank 3.

The foregoing methods create a first-order (translated) response, providing only a gradual roll-off in the adjacent

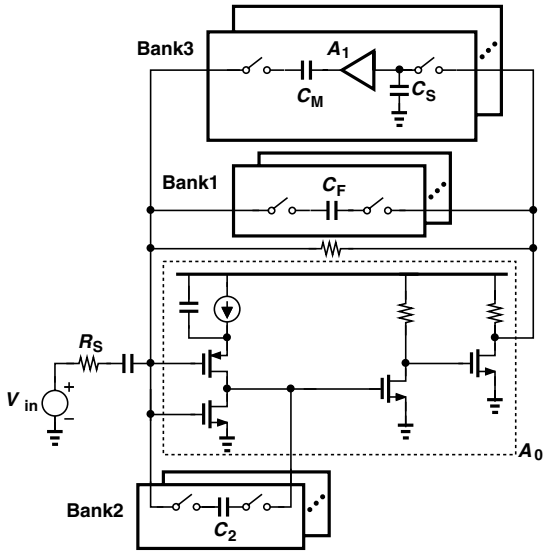
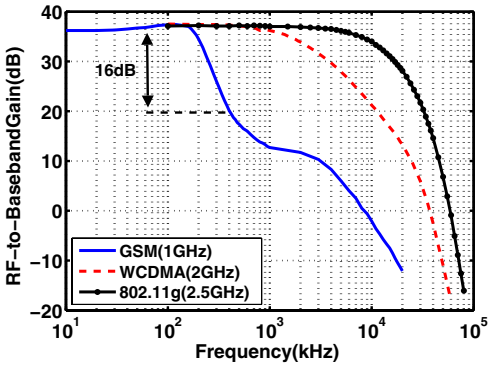



Fig. 17. (a) Use of Miller notch filter to increase apparent value of capacitors and shape the response, (b) implementation of zeros within $A_1$.

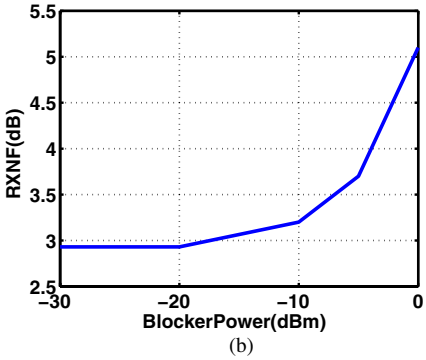
channels—unless a large droop is allowed in the desired channel. To raise the order, we grant $A_1$ a certain frequency response so that the Miller effect of $C_M$, $(1+A_1A_0)C_M 2j\pi(f - f_{LO})$, becomes *larger* at greater frequency offsets. For example, if $A_1(s) = ks$, then $(1 + A_1A_0)C_M 2j\pi(f - f_{LO}) \approx -kA_0C_M(4\pi)^2(f - f_{LO})^2$, as if the capacitor's admittance

rose with $f^2$ rather than $f$. This "super capacitor" property is accentuated by including two zeros (in the form of capacitive degeneration) in $A_1$.

Figure 18(a) shows the measured characteristics of the receiver developed above [15]. Programmable capacitor arrays permit configurability for GSM (with $f_{LO} = 1$ GHz), WCDMA (with $f_{LO} = 2$ GHz), and IEEE802.11b/g ($f_{LO} = 2.5$ GHz). It is observed that the receiver provides at least 16 dB of rejection in the alternate adjacent channel. Figure 18(b) plots the measured noise figure as a function of the power of a blocker at 20-MHz offset. The NF rises from 2.9 dB to 5.1 dB.




(a)



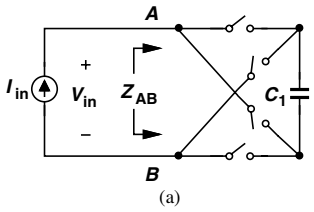

(b)

Fig. 18. (a) Measured frequency response of receiver with different capacitor settings, (b) measured noise figure as a function of blocker level at 20-MHz offset.

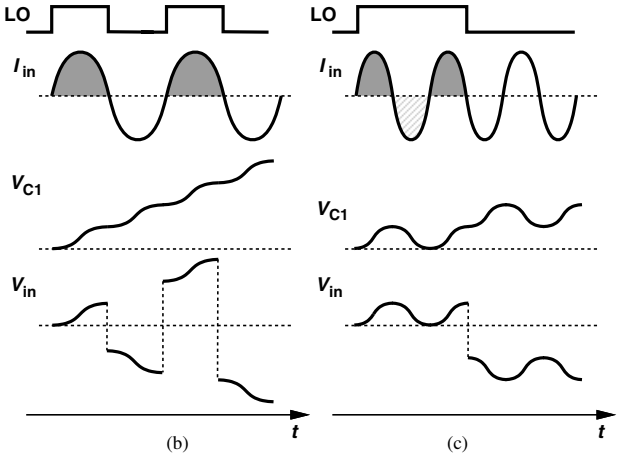
## VI. LO Harmonic Rejection

Commutated networks exhibit translated responses around not only the first harmonic of the LO but also around higher harmonics. If at least eight phases of the LO are available, then the downconversion mixing can utilize conventional harmonic-rejection techniques. Alternatively, we can envision new commutated circuits that suppress blockers at the LO harmonics. In this section, we propose such a circuit for the rejection of the third harmonic.

Let us first assume that only differential LO phases are available and ask whether a commutated network with useful frequency translation can be synthesized. Figure 19(a) shows an example. Here, $C_1$ connects to nodes $A$ and $B$ in one direction for one-half of the LO period and in the opposite direction for the other half. We invoke a time-domain perspective to




(a)




(b) (c)

Fig. 19. (a) Single commutated capacitor, (b) growth of capacitor voltage and input swing for $f_{in} = f_{LO}$, (c) similar growth for $f_{in} = 3f_{LO}$.

prove that $Z_{AB} = \infty$ at $f_{in} = f_{LO}$. As shown in Fig. 19(b), for a sinusoidal input current having this frequency (and in phase with the LO), the switches act as a full-wave rectifier, allowing the positive half cycles to charge $C_1$ and the negative half cycles to *add* to this charge. Consequently, the voltage across $C_1$, $V_{C1}$, increases indefinitely, and the input voltage appears as a waveform with a period equal to $T_{LO} = 1/f_{LO}$ but with a growing amplitude. As $t \rightarrow \infty$, $V_{in}$ can be viewed as a very tall square wave; hence $V_{in}/I_{in} \rightarrow \infty$ at $f_{in} = f_{LO}$.

A similar analysis suggests an infinite impedance at $f_{in} = 3f_{LO}$. Illustrated in Fig. 19(c), this case also entails indefinite growth of $V_{C1}$ because the charge delivered to the capacitor in each half cycle of the LO is positive. As a result, the input voltage experiences increasingly larger swings, eventually resembling a very tall square wave and yielding $V_{in}/I_{in} \rightarrow \infty$ at $f_{in} = 3f_{LO}$.

If a commutated circuit is to reject a signal around $3f_{LO}$, then its input impedance must remain finite at $3f_{LO}$. This occurs only if capacitor $C_1$ in Fig. 19(a) does not accumulate charge indefinitely. In other words, the net charge delivered to $C_1$ must be zero at the end of *each* LO period. This can be accomplished through the use of three commutated capacitors driven by 1/3-duty-cycle LO phases [Fig. 20(a)]. We note that during each LO pulse, the net area under the input current waveform is zero. For $f_{in} = f_{LO}$, on the other hand, the capacitors continue to accumulate charge, producing very large input voltage swings.

The foregoing topology has been implemented in a feedback path around the LNA of Fig. 15(a) as shown in Fig. 21(a). With $C_1 = C_2 = C_3 = 100$ pF and a switch aspect ratio of 10 $\mu$m/60 nm, the circuit exhibits the simulated gain responses depicted in Fig. 21(b) around the first and third harmonics.

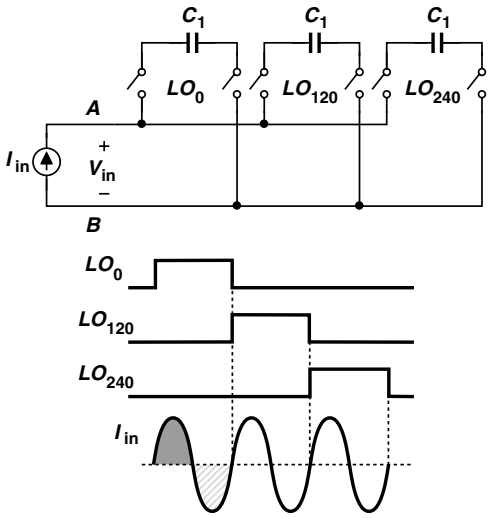
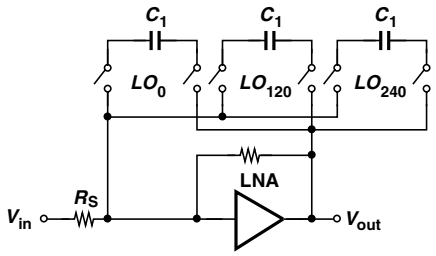
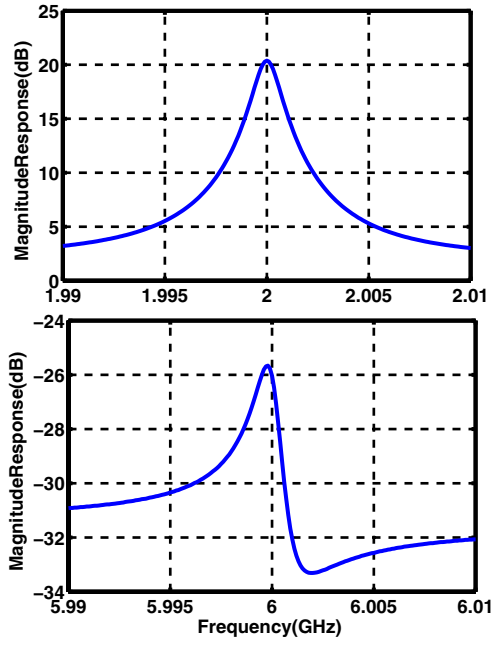



Fig. 20. (a) Commutated capacitors by 1/3-duty-cycle LOs, and (b) behavior for $f_{in} = f_{LO}$.




(a)




(b)

Fig. 21. (a) LNA using harmonic-rejection translational circuit, (b) simulated responses around first and third harmonics.

We observe a $-3$-dB bandwidth of 2 MHz around $f_{LO}$ and heavy suppression around $3f_{LO}$. (The second harmonic is also rejected.) The three LO phases can be generated by injection-locking a low-power ring oscillator to the main oscillator in a manner similar to [16].

In the presence of mismatches, the above architecture provides a finite rejection. For example, a 2° mismatch between two of the LO phases limits the attenuation of the third harmonic to 35 dB. Nonetheless, the output RF signal can still be processed by conventional harmonic-rejection mixing to achieve a higher rejection. The key point here is that the proposed approach affords an almost free rejection independent of the subsequent operations on the signals.

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