26.6 40Gb/s Amplifier and ESD Protection Circuit in 0.18μm CMOS Technology

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Optical systems operating at 40 Gb/s require broadband amplifiers and ESD protection circuits in both the receive and transmit paths. This paper describes an amplifier design that can precede or follow an equalizer in the receiver or act as a predriver in the transmitter front end. An ESD circuit is also presented that can be used for input or output nodes of 40Gb/s circuits.

While distributed circuits have been considered as an attractive candidate for high-speed amplification, several issues make their realization in CMOS technology difficult. First, since the bias currents of all stages flow through the same loads, the circuit suffers from a severe trade-off between voltage gain and voltage headroom, especially if MOSFETs are biased at a high current to maximize their f_T. Second, the loss of transmission lines in CMOS processes limits the number of sections that can be added to the amplifier. Third, the finite output resistance of short-channel transistors yields additional loss in the output transmission line.

The above issues arise because of the additive nature of the gain in distributed amplifiers. On the other hand, multiplicative gain and hence cascaded stages do not face these difficulties but require a large bandwidth per stage. This paper introduces a technique that raises the bandwidth of cascaded differential pairs by a factor of $2\sqrt{3}\approx3.5$, well above the factors corresponding to inductive or T-coil peaking.

Consider the inductively-peaked cascade of two stages shown in Fig. 26.6.1, where it is assumed M_1 and M_2 contribute approximately equal capacitances (C/2) to node X. As the frequency approaches $\omega_1=1/\sqrt{(L_1C)}$, the impedance of L_1 rises, allowing a greater fraction of I_{D1} to flow through $C_1 + C_2$ and hence extend the bandwidth.

To increase the bandwidth, an inductor, L_2 is inserted in series with C_2 such that L_2 and C_2 resonate at ω_1, thereby acting as a short and absorbing all of I_{D1}. Now, I_{D1} flows through C_2 rather than $C_1 + C_2$, leading to a more gradual roll-off of gain. For L_2 and C_2 to resonate at ω_1, $L_2 = 2\ L_1$.* Moreover, to minimize peaking, the output voltage at this frequency, $I_{in}/(C_2\ \omega_1)$, must be equal to that at low frequencies, $I_{in}R_1$, yielding $R_1 = 2\sqrt{(L_1/C)}$. For reasons that are subsequently described, this topology is called a "triple-resonance amplifier" (TRA).

The TRA exhibits the frequency response shown in Fig. 26.6.1, which is derived by examining the circuit at different frequencies (Fig. 26.6.2). The series resonance of L_2 and C_2 not only forces all of I_{in} to flow through C_2, but reverses the sign of the impedance Z_X, thus making V_X negative for $\omega > \omega_1$. As illustrated in Fig. 26.6.2, I_1 and I_2 must therefore flow into node X and, together with I_{in}, pass through C_2. The capacitive current I_2 multiplied by the impedance of C_2 creates a relatively constant output voltage as ω increases, while the inductive current I_1 introduces a roll-up in V_{out}. Consequently, $|V_{out}/I_{in}|$ continues to rise until the π network consisting of C_1, L_2, and C_2 begins to resonate, presenting an infinite impedance at node X and allowing all of Iin to flow through R_1 and L_1. This resonance frequency is given by

$$\omega_2 = \left[\sqrt{L_2C_1C_2/(C_1+C_2)}\right]^{-1} = \sqrt{2}\omega_1.$$

Since at ω_2, C_1 and C_2 carry equal and opposite currents,

$$|V_{out}| = |V_X| = |I_{in}|\sqrt{R_1^2 + L_1^2\omega_2^2} = |I_{in}|\sqrt{3/2}R_1.$$

That is, the magnitude response of the amplifier exhibits a peaking of $\sqrt{(3/2)}\approx1.8$dB.

For $\omega > \omega_2$, the π network becomes capacitive and $|V_{out}/I_{in}|$ begins to fall, returning to the midband value, R_1, when the impedance of the π network resonates with L_1. (See Fig. 26.6.2) This third resonance frequency is given by $\omega_3 = \sqrt[4]{6}\ \omega_1$. The –3dB bandwidth exceeds this value and is approximately equal to $\sqrt{3}\omega_1\approx2\sqrt{3}/(R_1C)$. In other words, the triple-resonance amplifier improves the bandwidth of resistively-loaded differential pairs by a factor of $2\sqrt{3}\approx3.5$.

Figure 26.6.3 depicts the overall 40Gb/s amplifier. Five differential triple-resonance stages provide multiplicative gain, with each stage achieving a small-signal bandwidth of 32GHz. With a loss of 5.3 dB in the last stage (due to a total load impedance of 25 Ω), the overall gain reaches 15 dB. The total input-referred noise voltage is 0.4 mV_{rms} from simulations.

The circuit of Fig. 26.6.3 exhibits several advantages over distributed amplifiers (DAs). First, the load resistance of the internal stages need not be equal to 50Ω, allowing greater gain. Second, the series resistance of the inductors impacts the performance to a much lesser extent than in the input transmission line of DAs. Third, the voltage headroom constraints remain independent of the number of stages.

The 1.8-dB peaking illustrated in Fig. 26.6.1 is of concern in cascaded stages. However, the finite Q of the inductors lowers this effect considerably. Simulations indicate that the overall 40Gb/s amplifier incurs a peaking of only 2dB.

Figure 26.6.4 shows the input ESD protection circuit. As proposed in [1], T-coil networks can improve both the input matching and the bandwidth of ESD protection circuits. However, for a given ESD capacitance, losses in the T-coil still limit the bandwidth. This work describes two modifications of T-coil-based ESD circuits that extend the speed from 10Gb/s to 40Gb/s with little compromise in voltage tolerance. The first modification is to lower the capacitance seen by the T-coil through the use of a negative impedance converter. As illustrated in Fig. 26.6.4, M_3-M_4 and C_c introduce a negative capacitance between nodes X and Y [2]. The upper bound on the value of C_c is that which places the circuit at the edge of relaxation oscillation. For random data, C_c must remain well below this bound to ensure minimal ringing and intersymbol interference.

The second modification is to employ pn junctions rather than MOS-based topologies as ESD protection devices. Comparison of the results in [1] with those in this work suggests that pn junctions exhibit less capacitance for a given voltage tolerance. Both concepts can be applied to output ESD protection circuits as well.

Both circuits have been fabricated in 0.18-μm CMOS technology and tested on a probe station with 40Gb/s random data. The die photographs are shown in Fig. 26.6.5.

Figure 26.6.6 shows the single-ended eye diagram of the amplifier for an input level of 100 mV_{pp}. The small-signal measured differential gain is 15dB. Single-ended S-parameter measurements indicate a -3dB bandwidth of 22GHz. The circuit consumes 190mW from a 2.2V supply and achieves substantially larger bandwidth and gain-bandwidth product than the distributed amplifiers reported in [3-5]. Also comparison of [2] (cascaded stages) and [4] reveals that practical DAs achieve a much lower gain-bandwidth product than cascaded stages. None of the circuits in [3, 4, 5] have been tested with random data to reveal effects such as ringing or intersymbol interference.

Figure 26.6.7 shows the measured single-ended 40Gb/s output eye of the ESD circuit. For four samples, the human-body model tolerance is 700-800 V while the machine model tolerance is 100V.

*Since in practice, C_1 and C_2 are not exactly equal, the ratio of L_1 and L_2 can be slightly adjusted to compensate for the difference.

References:

[1] S. Galal and B. Razavi, "Broadband ESD Protection Circuits in CMOS Technology," *ISSCC Dig. Tech. Papers*, pp.182-183, Feb. 2003.

[2] S. Galal and B. Razavi, "10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18-μm CMOS Technology," *ISSCC Dig. Tech. Papers,* pp.188-189, Feb. 2003.

[3] P.F. Chen et al., "Silicon-on-Sapphire MOSFET Distributed Amplifier with Coplanar Waveguide Matching," *IEEE RFIC Symp. Dig. of Tech. Papers*, pp. 161-164, 1998.

[4] B.M. Frank et al., "Performance of 1-10GHz Traveling Wave Amplifiers in 0.18-μm CMOS," *IEEE MWCL Dig. of Tech. Papers*, vol. 12, pp. 327-329, Sept. 2002.

[5] Ren-Chieh Liu et al., "A 0.5-14-GHz 10.6-dB CMOS Cascode Distributed Amplifier," *IEEE Symp. VLSI Cir. Dig. of Tech. Papers*, pp.139-140, 2003.

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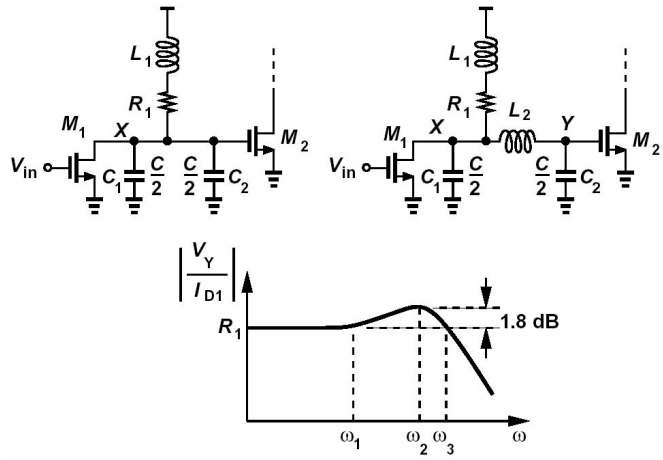

Figure 26.6.1: Inductively-peaked stage, triple-resonance amplifier, and frequency response of TRA.

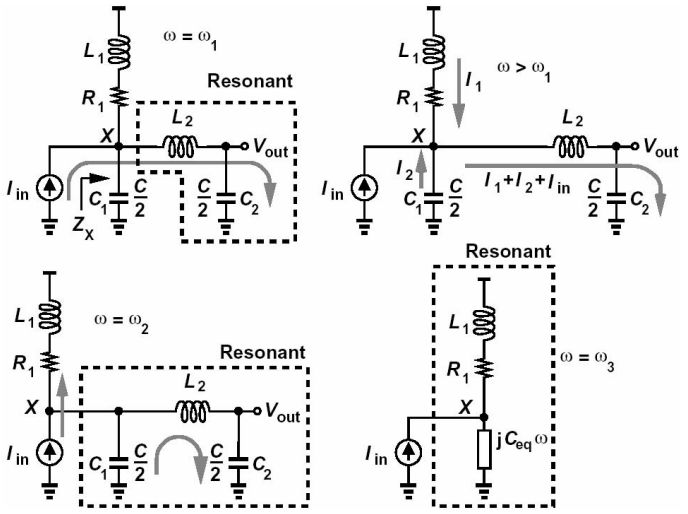

Figure 26.6.2: Behavior of a triple-resonant circuit at different frequencies.

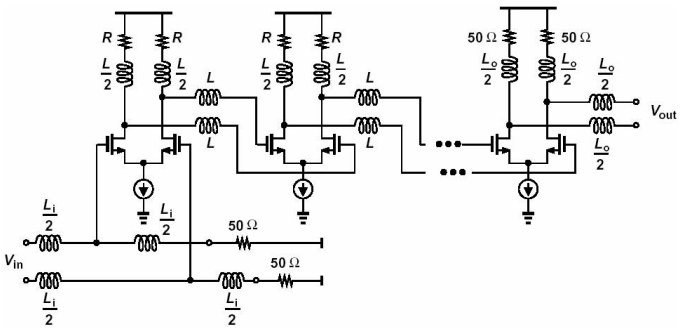

Figure 26.6.3: Differential triple-resonant amplifier (TRA).

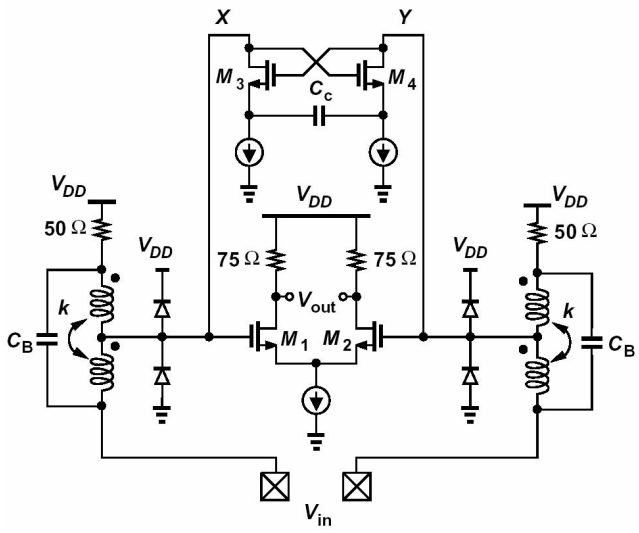

Figure 26.6.4: Input ESD protection circuit.

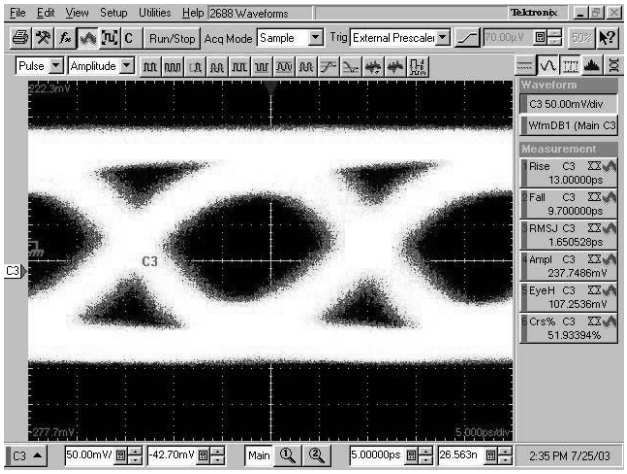

Figure 26.6.6: Measured amplifier single-ended output eye for an input signal level of 100mVpp (Vertical scale: 50mV/div., horizontal scale: 5ps/div.)

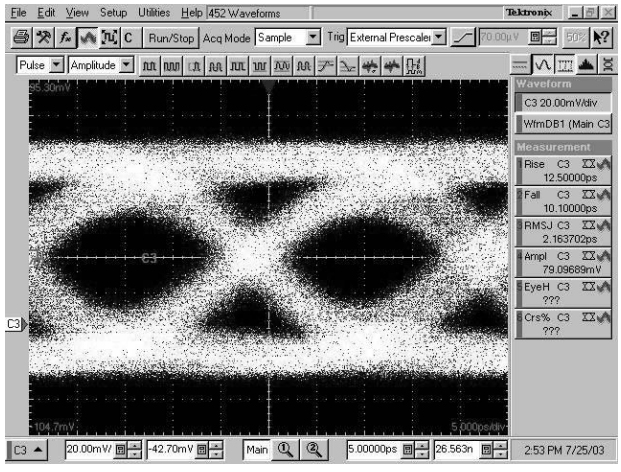

Figure 26.6.7: Measured output eye of the ESD circuit (Vertical scale: 20mV/div., horizontal scale: 5ps/div.).

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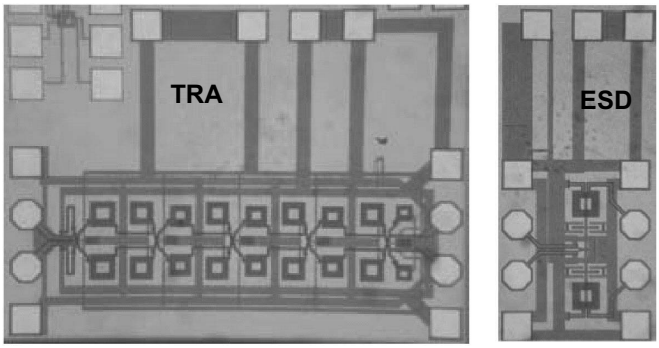

Figure 26.6.5: Die photograph of TRA and ESD protection circuit.

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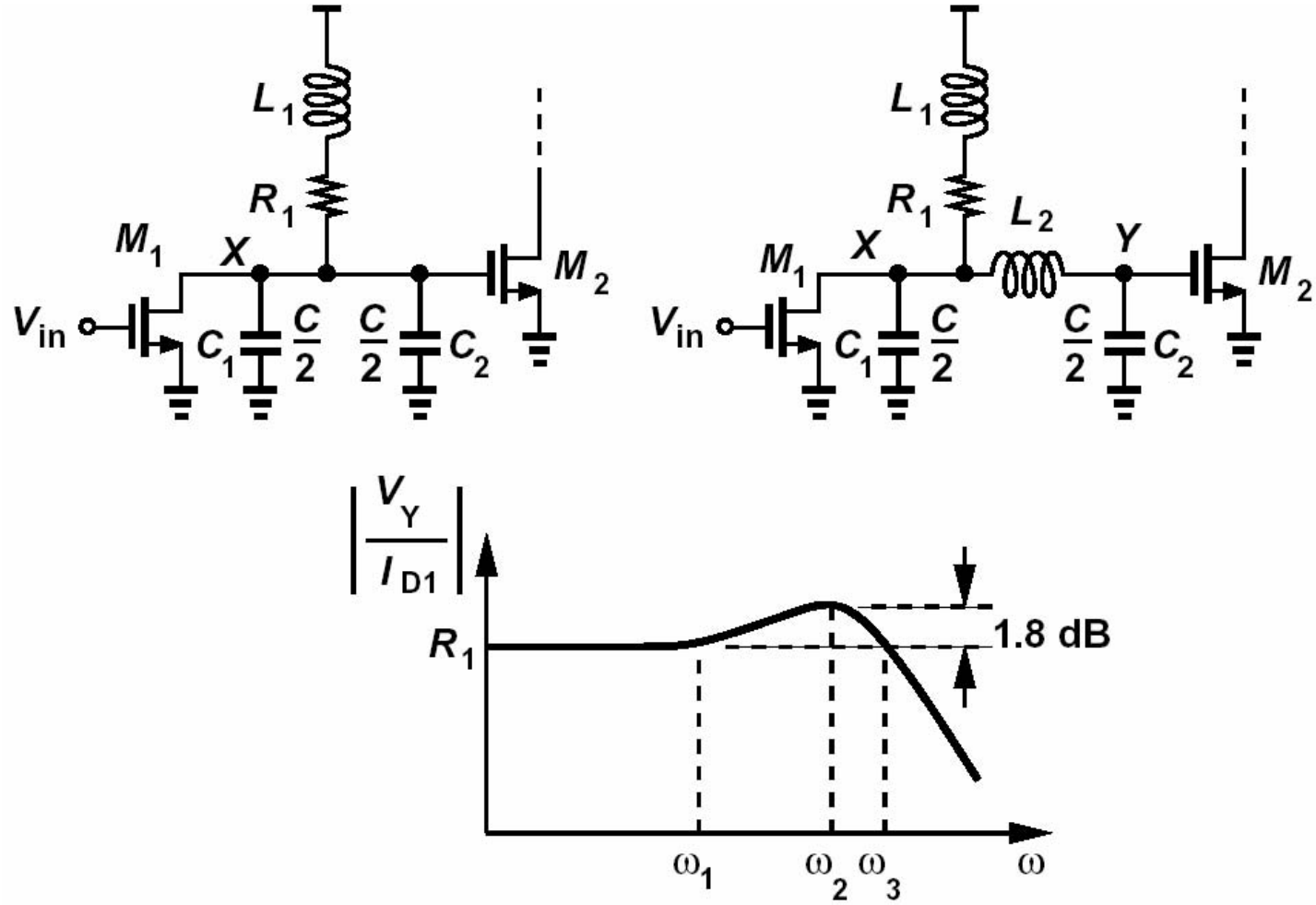

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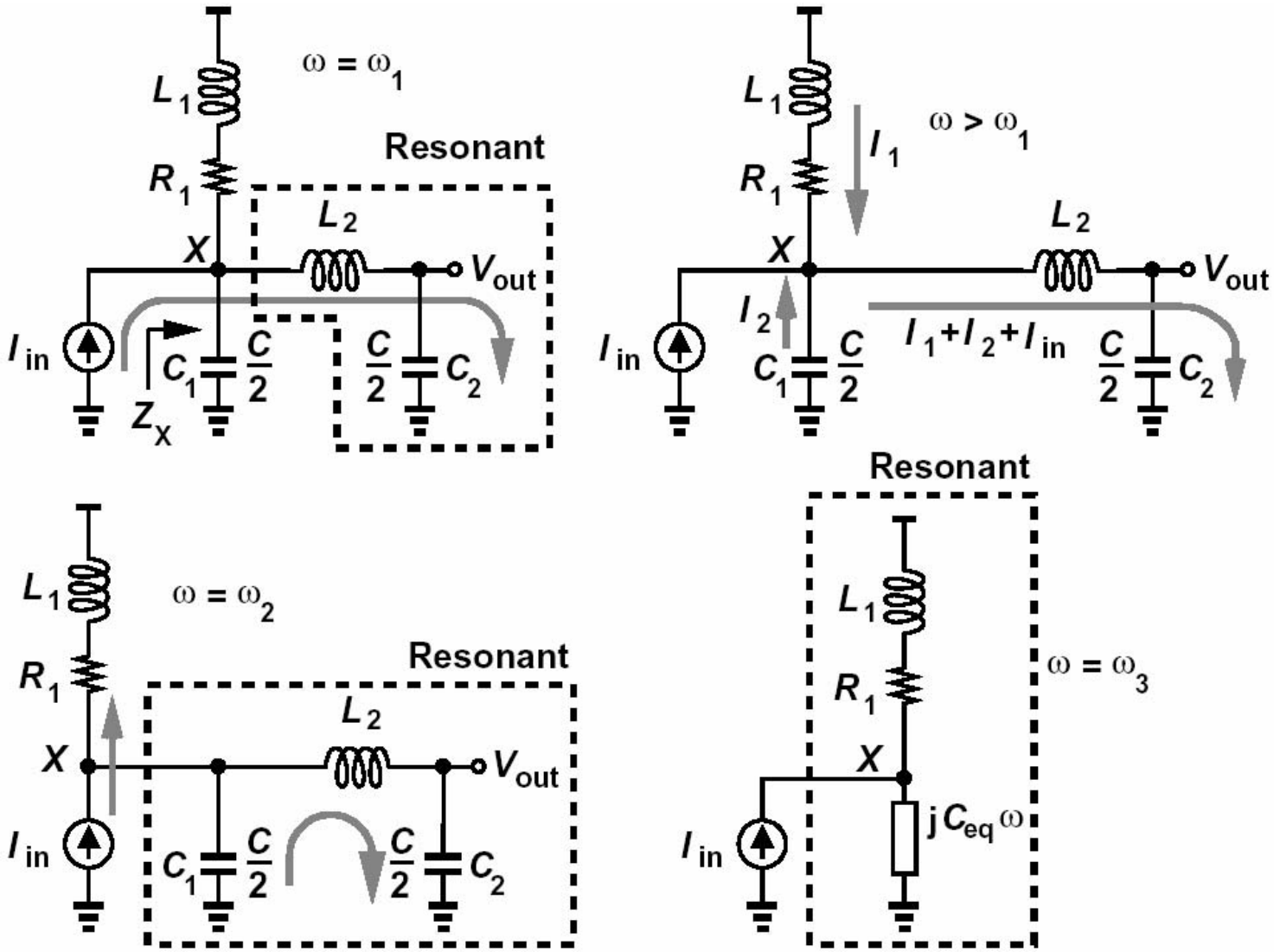

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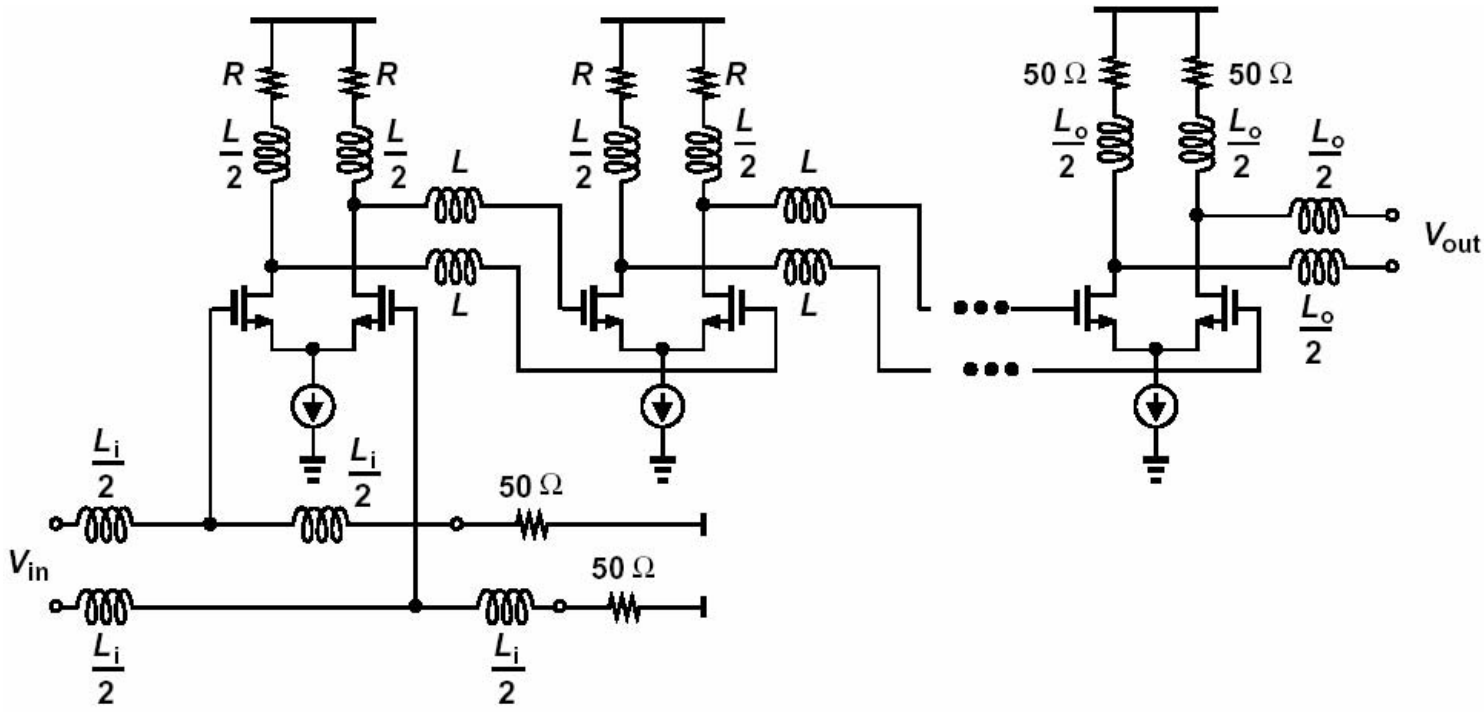

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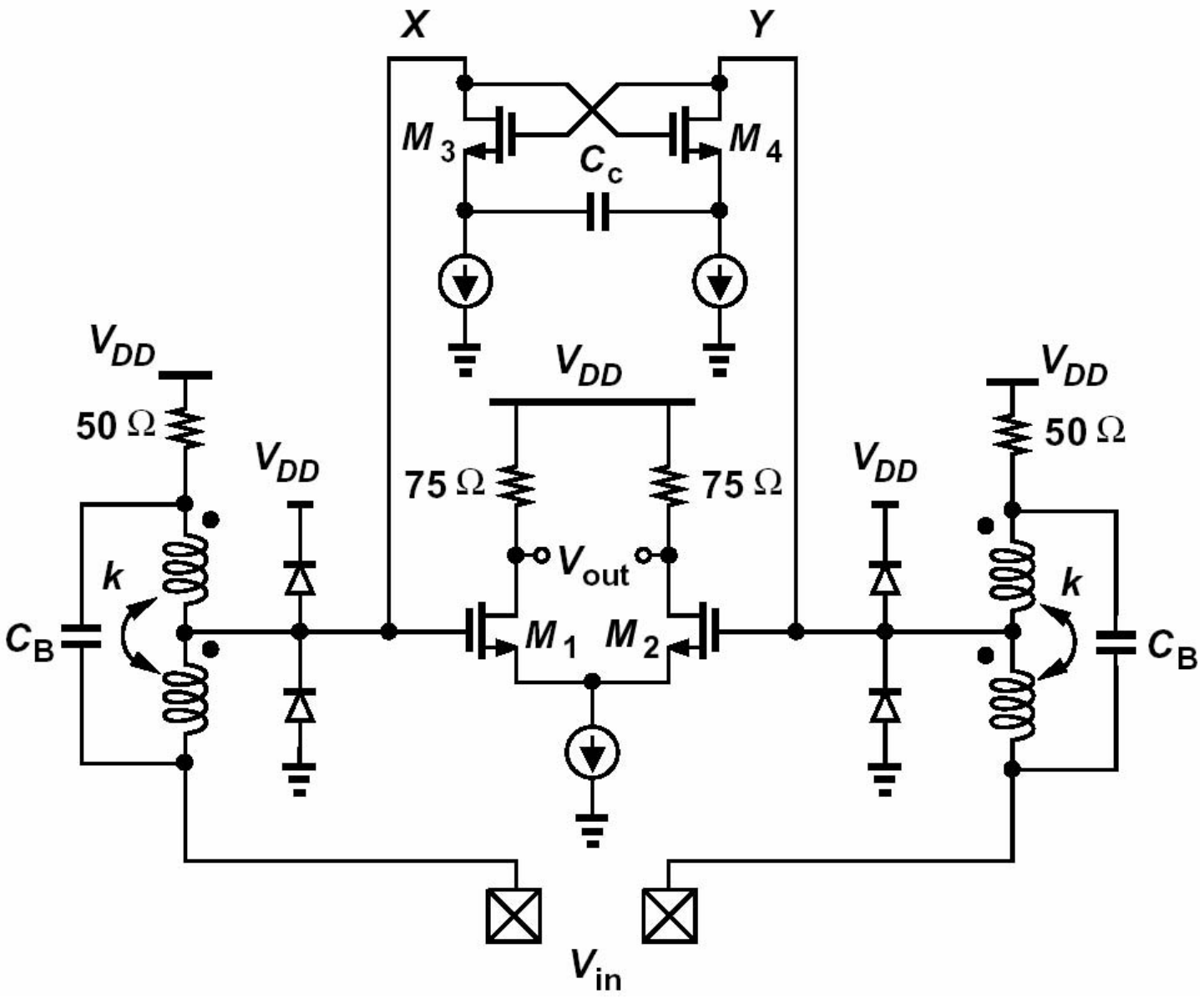

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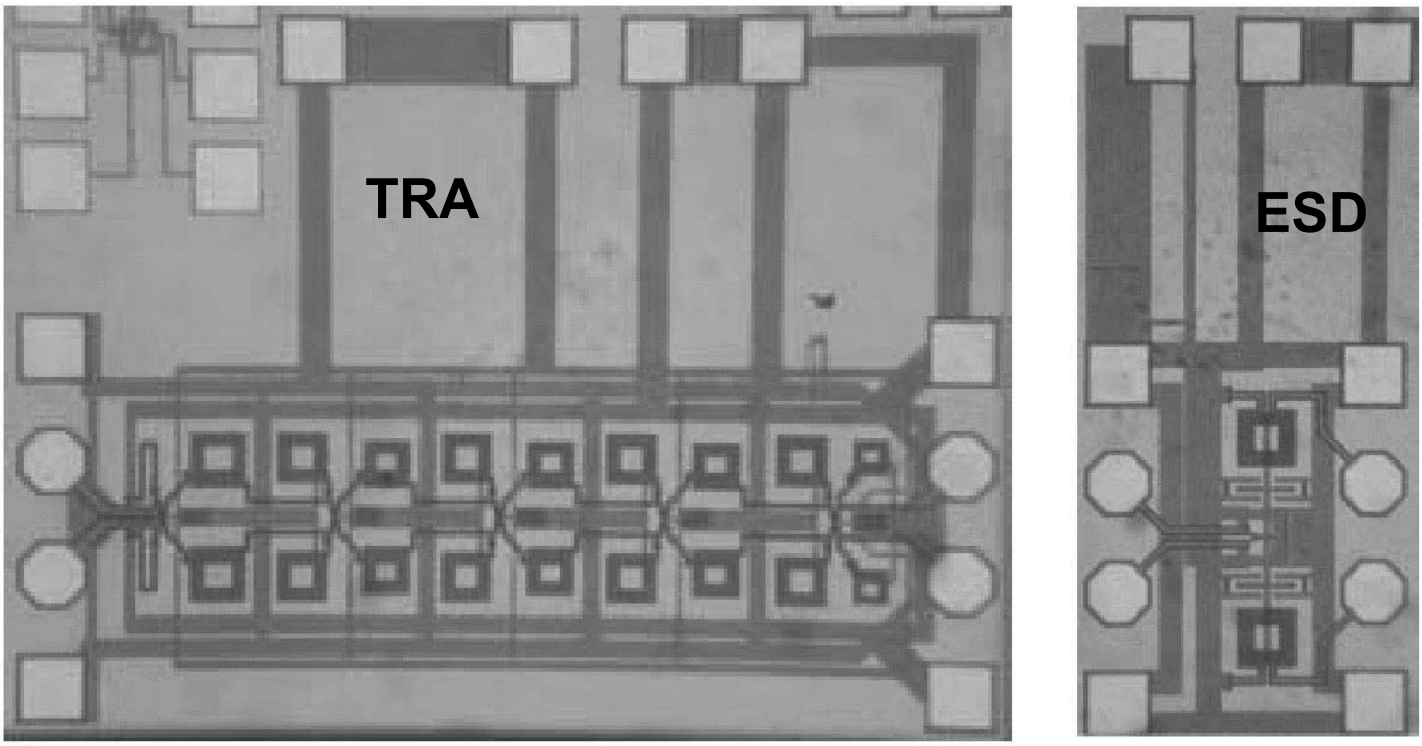

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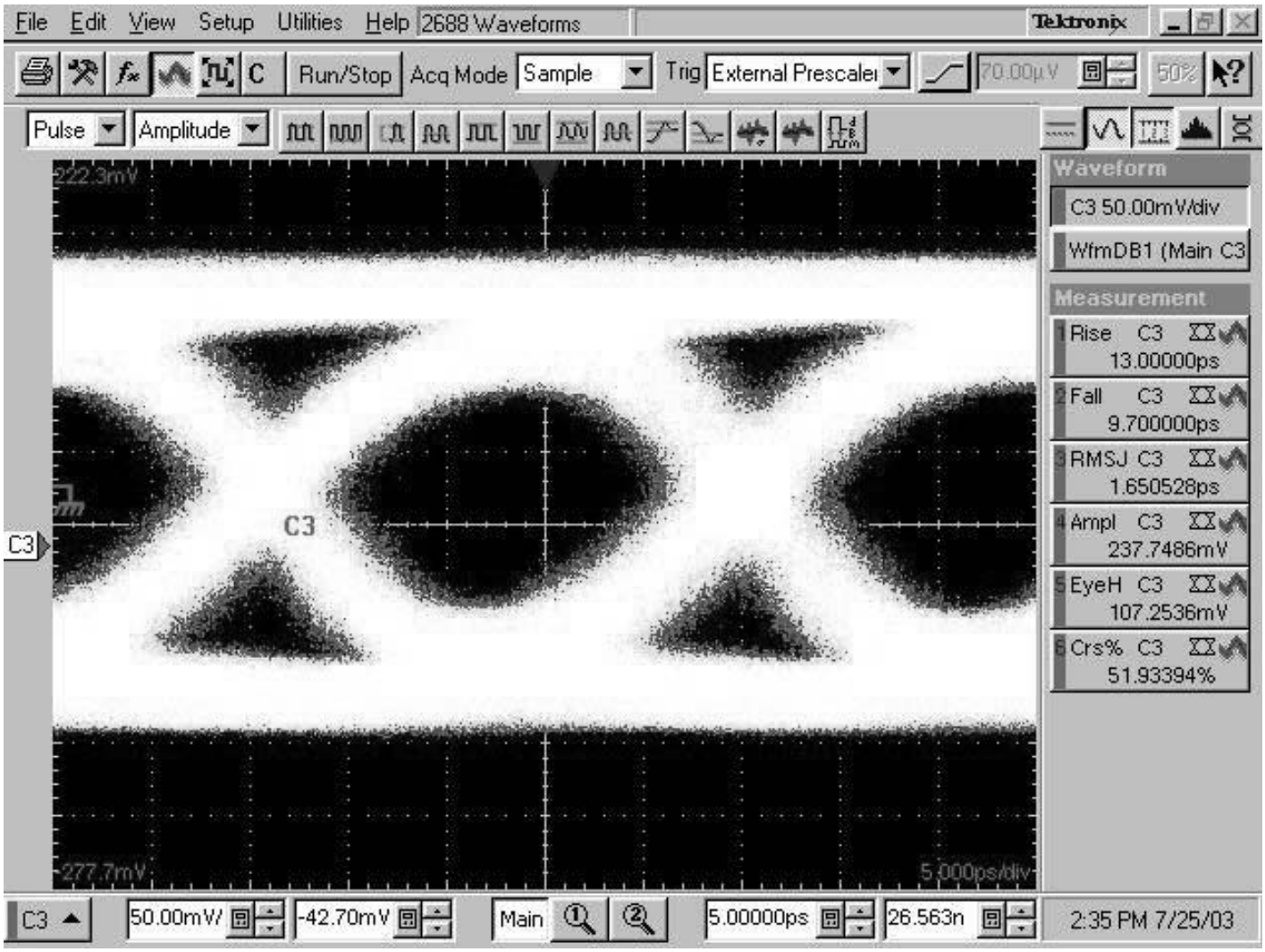

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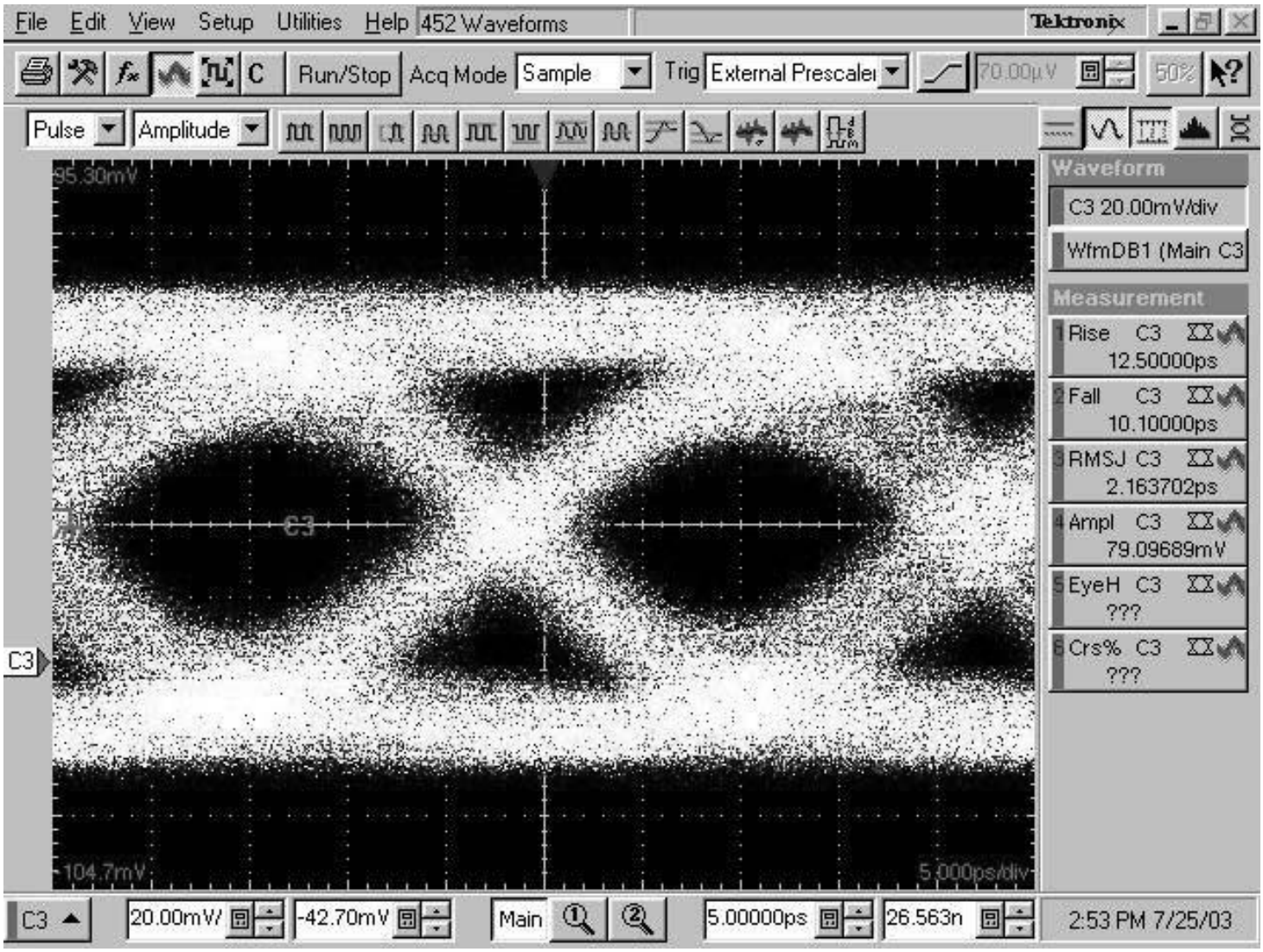

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