Oscillator Jitter Due to Supply and Substrate Noise

Frank Herzel[1]and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

Abstract

Oscillators used in digital systems experience substantial supply and substrate noise. This paper describes the timing jitter of oscillators in such applications, demonstrating that the contribution of device electronic noise is typically much less significant than that due to environmental noise. We utilize a frequency modulation model to predict the jitter, and study the effect of design parameters such as device dimensions and number of stages.

I. INTRODUCTION

Most high-speed microprocessors and memories employ phase locking at the board-chip interface to suppress timing skews between the on-chip clock and the system clock [1]-[3]. Fabricated on the same substrate as the rest of the circuit, the phase-locked loop (PLL) must typically operate from the global supply and ground busses, thus experiencing both substrate and supply noise. The noise manifests itself as jitter at the output of the PLL, primarily through various mechanisms in the voltage-controlled oscillator (VCO). As shown in this paper, the contribution of the supply and substrate noise to the jitter is typically much greater than that due to electronic noise of the oscillator's constituent devices.

This paper describes the effect of supply and substrate noise on the performance of differential ring oscillators, providing insights that prove useful in the design of other types of oscillators as well. Section II presents the simulation environment and the mechanisms giving rise to jitter in differential oscillators. Section III formulates the jitter with the aid of a simple model and Section IV relates phase noise and jitter for white noise sources. Section V studies the effect of oscillator design parameters on the jitter.

II. GENERAL CONSIDERATIONS

In this paper, we consider differential CMOS ring oscillators as a candidate for low-jitter operation. Shown in Fig. 1, the circuit is simulated in a 0.6-μm technology with the following values: $W = 80\,\mu$m, $L = 0.6\,\mu$m, $R_{\rm L} = 1$ kΩ, $I_{\rm SS} = 1$ mA, $C_{\rm L} = 0, V_{\rm DD} = 3$ V, unless otherwise stated. The voltage source ΔV_{DD} represents the supply noise and is modeled here by a sinusoid with variable frequency. The peak
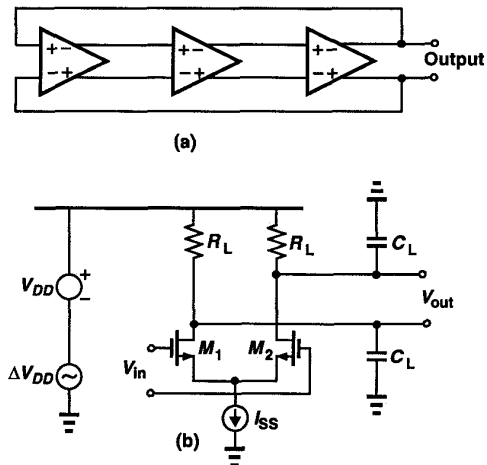
Fig. 1. Differential ring oscillator (DRO): (a) block diagram and (b) implementation of one stage.

amplitude of ΔV_{DD} is equal to 100 mV.

What mechanisms convert the supply and substrate noise to jitter in a fully differential oscillator? We identify two effects. First, as shown in Fig. 2, the drain junction capacitance of each transistor is a function of V_{DD} and V_{sub}, modulating
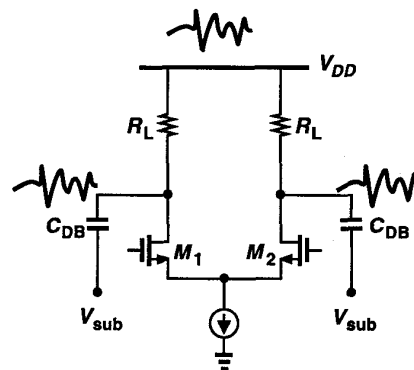

Fig. 2. Modulation of device junction capacitances by common-mode noise.

the delay of each stage as noise appears in either voltage. Second, the common-mode (CM) rejection of the differential pair degrades as the differential input deviates from zero. As illustrated in Fig. 3, the differential output is influenced by
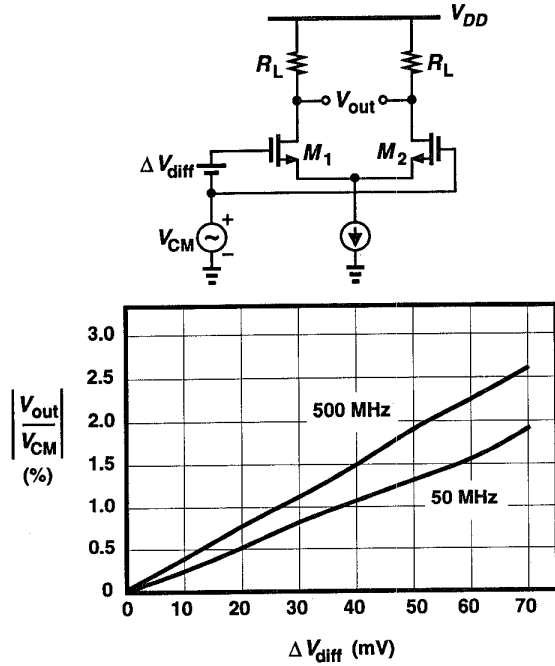
Fig. 3. Degradation of common-mode rejection with input imbalance.

input CM variations, even at low frequencies, if M_1 and M_2 carry unequal currents. Note, however, that the conversion of noise to jitter becomes less pronounced as the input differential voltage increases. Thus, the gain plot in Fig. 3 must be weighted by a sensitivity function.

III. JITTER ANALYSIS

Two parameters commonly used to quantify the time-domain purity of oscillations are long-term jitter and cycle-to-cycle jitter. Illustrated in Fig. 4(a), the former models the total phase error with respect to an ideal oscillator. This parameter is

(a)

Long-Term
Jitter

$\Delta T_2 - \Delta T_1$ = Cycle-to-Cycle Jitter
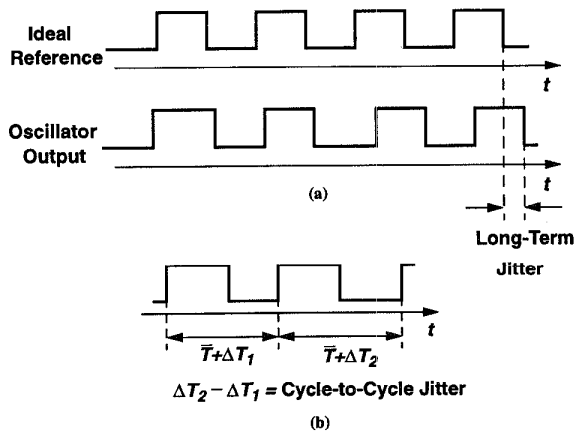
(b)

Fig. 4. Illustration of long-term jitter (a) and cycle-to-cycle jitter (b).

nonetheless ill-suited to describing the performance of a free-running oscillator because its variance approaches infinity. By

contrast, cycle-to-cycle jitter, depicted in Fig. 4(b) and given by

$$\Delta T_{\rm cc} = \lim_{N \to \infty} \sqrt{\frac{1}{N} \sum_{n=1}^{N} (T_{n+1} - T_n)^2}, \qquad (1)$$

formulates the short-term dynamics of the period and is bounded.

While useful for studying stand-alone oscillators, cycle-to-cycle jitter does not reflect the impact of modulation due to $1/f$ noise. However, the effect of this noise is typically negligible when a VCO is embedded in a wideband PLL.

An oscillator subject to supply and substrate noise may be considered a voltage controlled oscillator (VCO) with different "control" voltages each having a different sensitivity or "gain." Since this gain can be measured easily, it is useful to view the generation of jitter as frequency modulation. Suppose in an oscillator with center frequency f_0, the modulating control voltage is a small sinusoidal perturbation, $\Delta V_{\rm DD}(t) = V_{\rm m} \cos \omega_{\rm m} t$. The frequency then follows the control voltage according to

$$\Delta f_0(t) = V_{\rm m} K_j \cos \omega_{\rm m} t, \qquad (2)$$

where K_j is the sensitivity with respect to noise source number j (e.g., the supply node). The deviation of the period from the mean is

$$\Delta T(t) = \frac{1}{f_0 + \Delta f_0(t)} - \frac{1}{f_0} \qquad (3)$$

$$\approx -\frac{V_{\rm m} K_j}{f_0^2} \cos \omega_{\rm m} t. \qquad (4)$$

Multiplying this expression by $\Delta T(t + \tau)$ and averaging the result with respect to t, we obtain the autocorrelation function:

$$C(\tau) = \overline{\Delta T(t + \tau) \Delta T(t)} \qquad (5)$$

$$= \frac{V_{\rm m}^2 K_j^2}{2 f_0^4} \cos(\omega_{\rm m} \tau). \qquad (6)$$

It can be proved that $\Delta T_{\rm cc}^2 = 2C(\tau = 0) - 2C(\tau = 1/f_0)$. Thus,

$$\Delta T_{\rm cc} = \frac{V_{\rm m} K_j}{f_0^2} \sqrt{1 - \cos(\omega_{\rm m}/f_0)}. \qquad (7)$$

This equation is an important result in that it reduces the calculation of jitter to the calculation or measurement of K_j. For $\omega_{\rm m} \ll f_0$, we have

$$\Delta T_{\rm cc} \approx \frac{V_{\rm m} K_j \omega_{\rm m}}{\sqrt{2} f_0^3}. \qquad (8)$$

In order to verify the above results, the ring oscillator of Fig. 1 was simulated with supply and substrate noise. Plotted in Fig. 5 are the observed jitter values as a function of the noise frequency. Note the reasonable agreement between the analytical prediction developed above and the simulations.
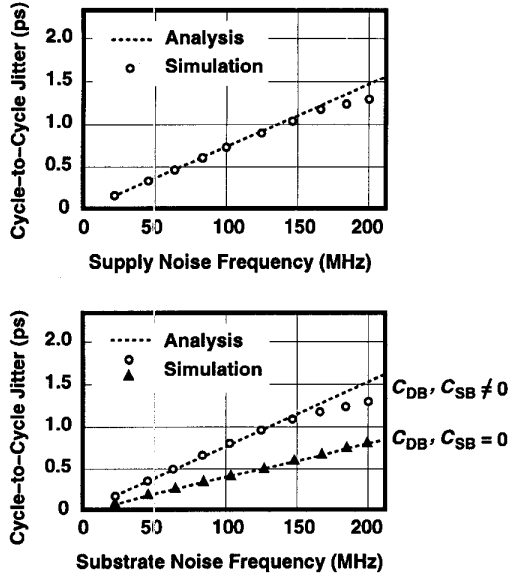
23.6.2

Fig. 5. Cycle-to-cycle jitter vs. supply and substrate noise frequency (oscillation frequency ≈ 2 GHz).

IV. JITTER DUE TO THERMAL AND SHOT NOISE

Thermal and shot noise of the devices in an oscillator loop leads to phase noise and jitter [4, 5, 6]. Our objective here is to express jitter in terms of phase noise and vice versa. These relationships are useful because they relate two measurable quantities.

As derived in the Appendix, the phase noise $S_\phi(\omega)$ (with respect to the carrier) can be expressed in terms of the cycle-to-cycle jitter as

$$S_\phi(\omega) \approx \frac{\left(\omega_0^3/2\pi\right) \Delta T_{cc}^2}{\left(\omega - \omega_0\right)^2}, \qquad (9)$$

where ω_0 is the oscillation frequency and $\omega - \omega_0$ is the offset frequency. Thus,

$$\Delta T_{cc}^2 \approx \frac{2\pi}{\omega_0^3} S_\phi(\omega) \left(\omega - \omega_0\right)^2. \qquad (10)$$

This result holds only if $S_\phi(\omega) \propto (\omega - \omega_0)^{-2}$, which is the case for white noise sources. To obtain an estimate of the thermal jitter, we consider the differential CMOS ring oscillator in [4]. For the 2.2-GHz oscillator with a phase noise of −94 dBc/Hz at 1 MHz offset, we obtain from (10) a thermal cycle-to-cycle jitter of 0.2 ps, i.e., less than 0.2°. In most timing applications, such a small value is negligible with respect to other sources of random jitter.

V. EFFECT OF DESIGN PARAMETERS

Ring oscillators have a wide design space: device size, voltage swings, power dissipation, and the number of stages influence the overall sensitivity to supply and substrate noise.

In this section, we study the jitter as a function of three parameters: transistor gate width, power dissipation, and the number of stages. To make meaningful comparisons, the circuit is modified in each case such that the frequency of oscillation remains constant.

A. Effect of Transistor Gate Width

The differential three-stage ring oscillator of Fig. 1 begins to oscillate for $W \geq 30\,\mu m$. Fig. 6 shows the effect of the gate width on the jitter, where the oscillation frequency is
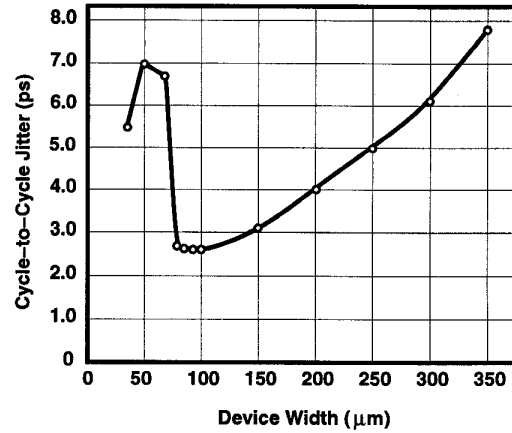

Fig. 6. Jitter of the differential oscillator vs. gate width (oscillation frequency ≈ 500 MHz).

kept constant by adjusting C_L in Fig. 1. The jitter reaches a minimum for $W \approx 80\,\mu m$. For large W the value of C_L must be reduced so as to maintain the same oscillation frequency, yielding a larger *voltage-dependent* fraction due to drain and source junctions of each device and hence a higher sensitivity to noise.

B. Effect of Power Consumption

The jitter resulting from device electronic noise generally exhibits an inverse dependence upon the oscillator power dissipation [7], [4]. By contrast, the effect of supply and substrate noise on the jitter of a given oscillator topology is relatively independent of the power drain. This can be understood as follows. If the output voltages of N identical oscillators are added in phase, the effect of random, *uncorrelated* noise decreases by a factor $\sqrt{N}$ [4]. With supply and substrate noise, on the other hand, all the oscillators experience the same disturbance, thus exhibiting completely correlated noise. That is, both the noise voltage and the signal voltage are increased by a factor of N. Simulations confirm that cycle-to-cycle jitter changes negligibly if device dimensions and bias currents scale proportionally and the voltage swings remain constant.

C. Effect of Number of Stages

In applications where the required oscillation frequency is considerably lower than the maximum speed of the technology, a ring oscillator may incorporate more than three stages. Thus, the optimum number of stages with respect to the jitter is of

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interest.

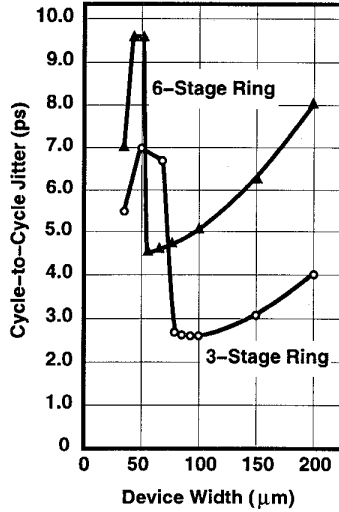Plotted in Fig. 7 is the jitter of three-stage and six-stage

Fig. 7. Jitter of the 3-stage and the 6-stage oscillators vs. gate width for an oscillation frequency of 500 MHz.

oscillators designed for a frequency of 500 MHz with constant tail current and voltage swings. We note that the minimum value of cycle-to-cycle jitter is smaller in a three-stage topology. This is because for the 3-stage oscillator, the reduction of the oscillation frequency to the desired value is obtained by means of the fixed capacitances C_L rather than by the voltage-dependent capacitances of the transistors. Hence, a smaller fraction of the total load capacitance is subject to variations with supply and substrate noise.

APPENDIX I.
RELATIONSHIP BETWEEN PHASE NOISE AND JITTER FOR WHITE NOISE SOURCES

The output voltage of an oscillator can be written as $V(t) = V_0 \cos[\omega_0 t + \phi(t)]$. The excess frequency is defined as $\Delta\omega(t) = d[\phi(t)]/dt$.

White noise in the feedback loop of the oscillator results in phase diffusion. We assume $\Delta\omega(t)$ is white noise with the autocorrelation

$$\overline{\Delta\omega(t+\tau)\Delta\omega(t)} = 2D_\phi \delta(\tau), \qquad (11)$$

where D_ϕ is the diffusivity and $\delta(\tau)$ the Dirac function. Under this condition, the autocorrelation of $V(t)$ is known [8]:

$$\langle V(t+\tau)V(t) \rangle = \frac{V_0^2}{2} \exp(-D_\phi|\tau|)\cos(\omega_0\tau). \qquad (12)$$

The probability density of $\phi(t)$ is a Gaussian distribution centered at $\phi(0)$ with the variance $\sigma_\phi^2 = 2D_\phi t$. Taking the Fourier transform of both sides of (12), normalizing the result to V_0, and assuming $\omega - \omega_0 \gg D_\phi$, we arrive at the single-sideband phase noise function:

$$S_\phi(\omega) \approx \frac{2D_\phi}{(\omega-\omega_0)^2}. \qquad (13)$$

Next, we will relate the cycle-to-cycle jitter and the phase noise to each other. From the variance of $\phi(t)$ derived above, we obtain the mean excess phase change during one cycle as $\Delta\phi_{cc} = \sqrt{2D_\phi \overline{T}}$. Thus, if the excess phase change during the n-th cycle is denoted by $\Delta\phi_n$, the n-th oscillation period satisfies the relation

$$2\pi f_0 T_n = 2\pi + \Delta\phi_n. \qquad (14)$$

For the deviation of the n-th period T_n from the mean period $\overline{T} = 1/f_0$, we then find

$$\begin{aligned} \Delta T_n &= \frac{\Delta\phi_n}{2\pi f_0} \\ &= \Delta\phi_n \frac{\overline{T}}{2\pi}. \end{aligned} \qquad (15)$$

Hence, the mean change ΔT_{cc} of the period during one cycle is related to $\Delta\phi_{cc}$ according to $\Delta T_{cc} = \Delta\phi_{cc}\overline{T}/2\pi$. That is,

$$\Delta T_{cc}^2 = \frac{4\pi}{\omega_0^3}D_\phi, \qquad (16)$$

where $\omega_0 = 2\pi/\overline{T}$. The cycle-to-cycle jitter can now be expressed in terms of the phase noise by inserting (16) in (13) to give

$$\Delta T_{cc}^2 \approx \frac{2\pi}{\omega_0^3}S_\phi(\omega)(\omega-\omega_0)^2. \qquad (17)$$

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23.6.4