A 0.4-6 GHz Receiver for LTE and WiFi

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Abstract — A universal receiver employs a feedback method to alleviate noise-linearity trade-offs and a new harmonic rejection (HR) method that does not require accurate phase matching. Realized in 28-nm CMOS technology, the prototype provides channel selection filtering at RF for channel bandwidths from 200 kHz to 160 MHz and exhibits a noise figure of 2.1-4.2 dB with HR > 60.8 dB while drawing 49 mW.

Today's mobile devices must support more than 15 cellular and WiFi brands. Radios serving in such an environment require many off-chip front-end filters, occupy a large chip area, and pose severe difficulties in generation and distribution of the local oscillator (LO) signals [1-4]. With a multitude of receive paths, either each path employs a dedicated synthesizer or the LO signals travel a long distance to reach all of the downconversion mixers. The former option further increases the area, while the latter consumes substantial power. It is therefore desirable to develop a single receiver path that can accommodate all of the bands.

Architecture The proposed receiver architecture is shown in Fig. 1. The main path consists of broadband gain stages G_{m1} and G_{m2}, downconversion mixers, baseband transimpedance amplifiers (TIAs), and baseband combining circuits. The blocks in red in fact include eight copies driven by 12.5%-duty-cycle LO phases. In addition, the receive path is loaded with three "harmonic traps" (H-Traps) so as to boost the rejection of harmonic blockers.

The first challenge to address relates to the conflicting requirements of LTE and WiFi. If the baseband transistors are large enough to provide low flicker noise for a 200-kHz channel, then they degrade the performance for a 160-MHz channel. We can create a greater gain at RF, but the chain then compresses at multiple ports in the presence of blockers. To our aid come the feedback impedances Z_1-Z_3, each containing a programmable N-path filter in parallel with a resistor.

A remarkable attribute that results is that the input-referred noise of the TIA is divided by the open-loop gain of the preceding stages, even though Z_1-Z_3 create low closed-loop gains. Breaking the trade-off between noise and non-linearity, the proposed concept is illustrated in Fig. 2 using simple baseband equivalent circuits. In Fig. 2(a) the TIA op amp noise, V_n, is divided by $G_{m2}R_2$ when referred to the input. Next, we apply feedback around the TIA [Fig. 2(b)], recognizing that V_n is still divided by $G_{m2}R_2$. Extending the idea to all three stages as shown in Fig. 2(c), we observe that V_n is divided by $G_{m1}R_1G_{m2}R_2$ when referred to the antenna. Thus, the feedback paths establish the requisite low impedance for blocker tolerance, but the noise of the TIA is still dramatically reduced. The feedback paths also increase the RF bandwidth to more than 7 GHz.

The receiver realizes blocker rejection by means of feedback impedances Z_{B1} and Z_{B2} in Fig. 1, which, by virtue of Miller multiplication, allow smaller capacitors and switches [6]. They also guarantee the stability of the closed-loop architecture. Impedances Z_1, Z_2 and Z_3 perform channel-selection filtering while Z_1 also provides input matching.

Harmonic Traps The broadband nature of the receiver implies that harmonic blockers can downconvert to the baseband. Harmonic rejection mixing [1-5] is an effective means to deal with this issue, but it has not addressed the problem of LO phase mismatches. A 60-dB rejection at $3f_{LO}$ or $5f_{LO}$ requires an LO phase mismatch of less than 0.03°[3] (42 fs at 2 GHz), which proves extremely challenging. In this work we propose the use of harmonic traps in Fig. 1 so as to reject the harmonic blockers in multiple, independent stages, thereby reducing the sensitivity to mismatches. As illustrated in Fig. 3(a), we wish to attach a trap to a port of the receiver such that it provides a low impedance at nf_{LO} where n>1. We note that the feedback capacitor yields a high Miller-multiplied capacitance at nf_{LO} if A_1 has a high gain only at these frequencies. We then configure A_1 as a common-source stage having a composite load, surmising that the circuit provides gain at nf_{LO} if Z_F assumes a high magnitude at such frequencies. This means that Z_F must be realized as a harmonic-enhancing impedance. As conceptually depicted in Fig. 3(b), if the RF signal provided by M_1 is copied with scaling factors equal to $1, \sqrt{2}$, and 1, commuted with – 45°, 0 and + 45° phases and injected into a capacitor, the voltages at X_a, X_b and X_c are free from third and fifth harmonics and contain highly attenuated higher harmonics. In the next step, we can place C_0 around a gain stage so as to benefit from Miller multiplication. This idea in fact requires three amplifiers, as shown in Fig. 3(c), each one delivering an RF output with rejected harmonics. To sum these outputs, we apply them to PMOS V/I converters, returning the final current I_{tot} to the drain of M_1. With various mismatches, the rejection of this trap is limited to 10 dB, but since it consumes only 7 mW, we apply this idea three times in Fig. 1. Another 30-40 dB rejection is offered by the four copies of the TIA, whose baseband outputs have 45° phase difference and are subsequently combined as in conventional harmonic rejection mixers.

LO Generation The channel selection, blocker rejection and harmonic rejection operations incorporate eight LO phases whose generation from 0.4 to 6 GHz poses formidable challenges. For LTE and WiFi bands up to 4 GHz, we apply $f_{ext}=4f_{LO}$ and use two cascaded divide-by-2 stages to generate LO_1-LO_8. For higher frequencies, we utilize a delay-locked-loop containing a 4-stage differential delay line. The overall clock generation circuit consumes its maximum power of 25 mW at 6 GHz, primarily in form of fCV_{DD}^2 for driving switches in Z_{B1}, Z_{B2}, Z_1-Z_3 and the interconnects.

Experimental Results The receiver die photograph in 28-nm technology is shown in Fig. 4(a) with an active area of 1380 µm × 1370 µm of which 70% is occupied by channel-select filters. The receiver has been characterized for different LTE and WiFi bands with various channel bandwidths. Fig. 4(b) plots the measured receiver NF for four RF channel examples: two-sided bandwidths of 200 kHz, 4 MHz, 40 MHz and 160 MHz at input frequencies of 1 GHz, 2 GHz, 5 GHz and 6 GHz respectively. Also shown in Fig. 5 are the measured signal constellations and EVM for two cases: (1) a 64-QAM LTE signal in a 20-MHz bandwidth at a carrier frequency of 2 GHz, exhibiting an EVM of – 22.15 dB for an RF input level of – 74 dBm and (2) a 256-QAM WiFi signal in an 80-MHz bandwidth at a carrier frequency of 5 GHz, exhibiting an EVM of – 25.21 dB for an RF input level of – 57 dBm. Illustrated in Fig. 4(c) is the harmonic rejection measured with no adjustment or calibration, demonstrating the efficacy of the "trap" concept. We should make four remarks regarding the work in [1]. First, it can provide high rejection at either $3f_{LO}$ or $5f_{LO}$ but not at both at the same time. Second, the digital harmonic rejection algorithm is implemented off-chip. Third, it requires external tones at the harmonics for calibration. Fourth, the noise figure with blocker is 5 to 7 dB higher than ours.

References

[1] B. van Liempd et al., *IEEE JSSC.*, pp. 1815-1826, Aug. 2014.
[2] H. Wu et al., *IEEE JSSC*, pp. 796-807, Mar. 2019.
[3] Z. Ru et al., *IEEE JSSC*, pp. 3359-3375, Dec 2009.
[4] D. Murphy et al., *IEEE JSSC*, pp. 1336-1350, June 2015.
[5] J. Weldon et al., *IEEE JSSC*, pp. 2003-2015, Dec. 2001.
[6] J. W. Park and B. Razavi, *ISSCC Dig.*, pp. 356-357, Feb. 2014.

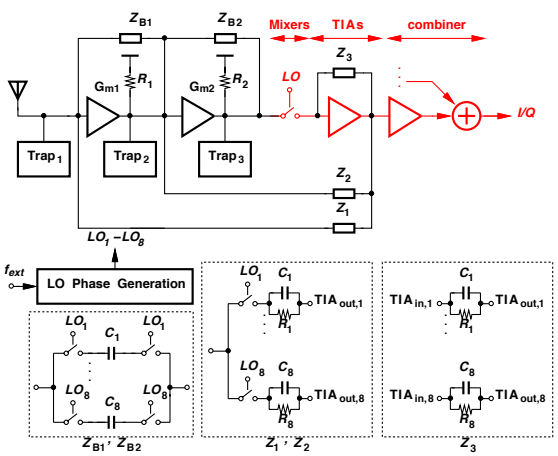


Fig. 1. Proposed receiver architecture

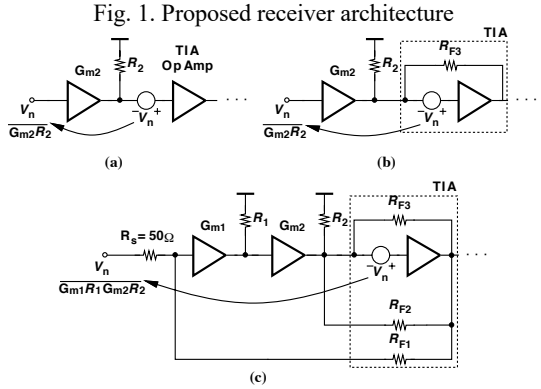


Fig. 2. (a) Gain stage before an open-loop TIA, (b) addition of feedback around the TIA, and (c) proposed multi-loop architecture

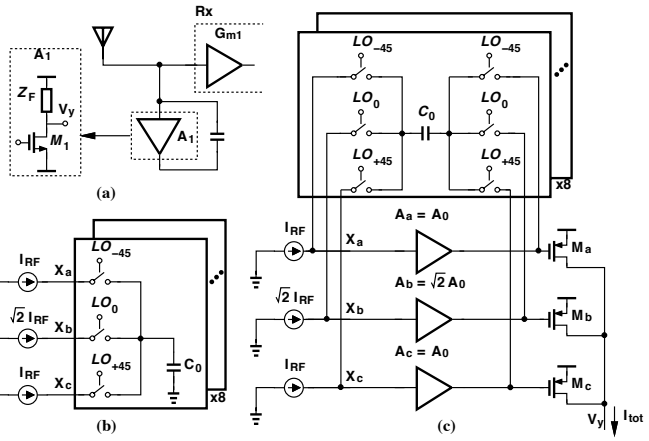


Fig. 3. (a) Harmonic trap concept, (b) basic harmonic rejection method, and (c) Implemented harmonic rejection amplifier

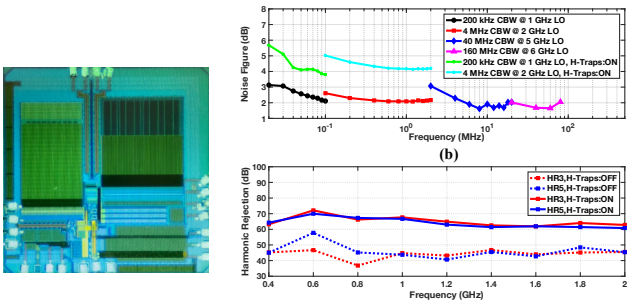
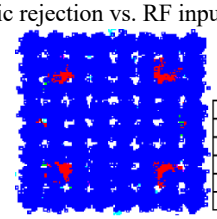
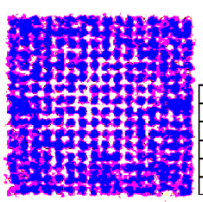


Fig. 4. (a) Receiver die photograph, (b) measured noise figure vs. baseband frequency for different configurations, and (c) measured harmonic rejection vs. RF input frequency



Standard	LTE
Modulation Scheme	64-QAM
Carrier Frequency [GHZ]	2
Channel Bandwidth [MHz]	20
Input Power [dBm]	-74
EVM [dB]	-22.15



Standard	802.11 ax
Modulation Scheme	256-QAM
Carrier Frequency [GHZ]	5
Channel Bandwidth [MHz]	80
Input Power [dBm]	-57
EVM [dB]	-25.21

Fig. 5 Measured constellation and EVM for LTE and WiFi standards

Table I. Performance summary

	[1]	[3]	[4]	This Work
RF Input	**Differential**	**Differential**	**Single-ended**	**Single-ended**
Input Frequency [MHz]	**400~6000**	**400~900**	**600~3000**	**400~6000**
Channel Bandwidth [MHz]	**1-100**	**24**	**0.4-6**	**0.2-160**
Gain [dB]	**70/58[1]**	**34.4**	**N/A**	**54**
NF [dB]	**2.4[2,6]/3.1[4,6]**	**4**	**1.8[2]/3[3]**	**2.1[2]/4.2[3]**
0-dBm OB-Blocker NF [dB]	**10[5,6]/14[4,6]**	**N/A**	**9[2]/13[3]**	**5.3[2]/7.1[3]**
OB-IIP3 [dBm]	**8[5]/3[4]**	**16**	**10**	**9.4/2.8[7]**
Harmonic Rejection [dB] $3f_{LO}/5f_{LO}$	**70/75**	**60/64**	**52/54**	**63/64[8]**
Power Consumption [mW]	**40**	**60**	**38.8-70**	**23-49**
Active Area [mm²]	**0.6**	**1**	**5.0**	**1.9**
CMOS Technology	**28 nm**	**65 nm**	**28 nm**	**28 nm**

[1]Above 3 GHz [2]Low noise mode [3]Harmonic rejection mode [4]Standard operation [5]LNA optimized [6]Balun loss not included [7]With Z_{B2} turned off and Z_{B1} using smaller switches for channel bandwidths more than 4 MHz with less stringent blocker requirements [8]Harmonic rejection up to 1 GHz for a fair comparison