A 12-Bit 200-MS/s 3.4-mW CMOS ADC with 0.85-V Supply

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Abstract—A SAR ADC incorporates two VCOs and a TDC as a multi-bit quantizer to improve the conversion speed. Using background calibration and realized in 45-nm technology, the ADC exhibits an SNDR of 68 dB and an FOM of 8 fJ/conv. step at Nyquist.

The conversion rate of SAR ADCs can be improved through the use of a multi-bit quantizer [1-3]. However, such an approach must employ either multiple DACs [1], incurring a large area penalty, a resistor ladder [2], suffering from a long response, or a time quantizer [3], facing resolution limitations. This paper proposes the use of VCOs as multi-bit quantizers in a SAR environment while avoiding these issues and achieving 3 bits of resolution per cycle. Another critical advantage of this method is that it allows shorter LSB conversion cycles by adjusting the VCO gain "on the fly." As a result, the last conversion can resolve three bits and the SAR DAC can have a resolution of only 10 bits – a substantial saving in DAC complexity. Two background calibration techniques are also introduced to reach a resolution of 12 bits.

Architecture Shown in Fig. 1, the ADC incorporates a 5-bit flash stage and a SAR loop consisting of two 3-GHz VCOs, a 3-bit time-to-digital converter (TDC) and a capacitor DAC. The ADC operates as follows. The analog input is sampled simultaneously by the flash stage and the 5-bit MSB DAC capacitors. The flash decision is then directed to this DAC, thus generating a residue, $V_{res} = V_{res}^{+} - V_{res}^{-}$. The two VCOs sense the residue with opposite signs [4], and their output phase difference is digitized by the TDC. The resulting LSBs are then fed back to the 5-bit LSB DAC, which couples to the MSB DAC through a bridge capacitor, C_B. The self-timed SAR loop runs for four cycles, resolving 2 bits in the first and 3 bits in each of the following three and allowing 1 bit of redundancy at the boundaries.

It is important to note that the flash stage reduces both the conversion time and the residue range presented to the VCOs, requiring only a moderate linearity in their control paths. Nonetheless, the gain of the VCOs (i.e., the ADC radix) must be calibrated against PVT variations. This is accomplished by adjusting the unit delay within the VCO (explained below).

Quantizer The quantizer begins with a cleared state every SAR cycle and accumulates phase in proportion to the residue level; after m VCO periods, the time difference reaches $\approx m(4\pi/\omega_0)K_{VCO}(V_{res}^{+} - V_{res}^{-})$, where ω_0 denotes the mean oscillation frequency. The TDC quantizes this edge spacing with a resolution of $T_{LSB} = 4$ ps, or, equivalently, $V_{LSB} = \omega_0 T_{LSB}/(4\pi m K_{VCO})$ volts. In our design, $m = (2/3, 1, 1, 2)$ in the four cycles. In order to change the quantizer resolution on the fly, we adjust the value of K_{VCO} and hence V_{LSB}.

The VCOs used in this work must satisfy several requirements: (1) Their gain must be adjustable precisely so that the quantizer resolution, V_{LSB}, can be changed on the fly; (2) they must generate enough cycles in unit time to provide a fine resolution; and (3) their phase noise must be sufficiently small especially because the residue is not amplified before reaching the VCOs. To this end, we propose a ring oscillator consisting of three comparator-based delay stages.

Configured as a variable-delay element [Fig. 2(a)], a comparator senses V_{CK} as an input and produces V_{out} with a delay, ΔT, proportional to V_{cont}; for $V_{cont} = 0$, the circuit is metastable and both ΔT and K_{VCO} are infinite. Figure 2(b) shows the resulting ring with an additional input, V_{OS}, to adjust K_{VCO}. In this design, V_{OS} begins from 150 mV in the MSB cycle and falls to about 8 mV in the LSB cycles, creating a roughly proportional increase in K_{VCO}. The important advantage of this VCO topology over conventional rings is that it can achieve nearly 20-fold change in K_{VCO} with only a small change in the oscillation frequency. The comparator is a modified version of the StrongArm latch.

With a power dissipation of 0.85 mW at 3 GHz, each VCO contributes significant phase noise (≈ -100 dBc/Hz at 10-MHz offset). The cycle-to-cycle jitter of both VCOs accumulates for $m = 2$ cycles, reaching a total of 700 fs (at $V_{OS} = 8$ mV). This value is quite smaller than the TDC resolution of 4 ps.

Calibration In addition to the VCO gain, the TDC thresholds must also be calibrated so as to obtain $T_{LSB} = 4$ ps. In this work, the two errors are calibrated simultaneously: V_{OS} in Fig. 2(b) adjusts the gain and the delay of each stage in TDC is controlled to change the thresholds.

An important difference between pipelined and SAR ADCs simplifies the calibration. In the former, the input signal information is lost after the first stage, requiring different calibration techniques for the gain and the thresholds. In the latter, on the other hand, the input remains on the capacitor DAC, allowing a single algorithm to correct for both types of errors. Our calibration defines a cost function as

$$E = (B_{ideal} \oplus B_{actual}) \times (V_{res,est} - V_{th,ideal}), \quad (1)$$

where B_{ideal} and B_{actual} denote the ideal and actual binary outputs of each TDC cell, $V_{res,est}$ is the estimated residue (i.e., the overall SAR ADC output), and $V_{th,ideal}$ represents each of the ideal equivalent threshold voltages against which the residue is quantized. This cost function is linearly proportional to gain and threshold errors if they are small, but still maintains correct polarity if they are large, guaranteeing convergence.

The above algorithm does not correct the gain error in the last SAR cycle. This error is calibrated by adding to this

step a ± 1 LSB pseudo-random value through the DAC and correlating it with the output of the last cycle.

Experimental Results The ADC of Fig. 1 has been fabricated in TSMC's 45-nm digital CMOS technology. Figure 3 shows the die photograph, whose active area measures 200 μm $\times$ 300 μm. The ADC draws 2.8 mW from a 0.85-V supply and 0.6 mW from a 0.85-V reference. The calibration is carried out off-chip and the results are returned to the chip through a serial bus. The measured results reported here are for a sampling rate of 200 MHz.

Plotted in Fig. 4, the DNL and INL reach a maximum of ± 0.6 LSB and ± 0.9 LSB, respectively. The measured output spectrum for an input frequency of 121 MHz is shown in Fig. 5, yielding an SNDR of 68 dB. The SNDR is plotted in Fig. 6 as a function of the input frequency, suggesting an FOM of 8 fJ/conv. step at Nyquist. Table I compares our performance to that of recent work in the resolution range of 12 to 14 bits and sampling rates of 160 MHz to 200 MHz.

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References

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[5] B. Verbruggen et al., *VLSI Symp.*, pp. 1-2, Jun. 2014.
[6] Yuan Zhou et al., *VLSI Symp.*, pp. 44-45, Jun. 2014.

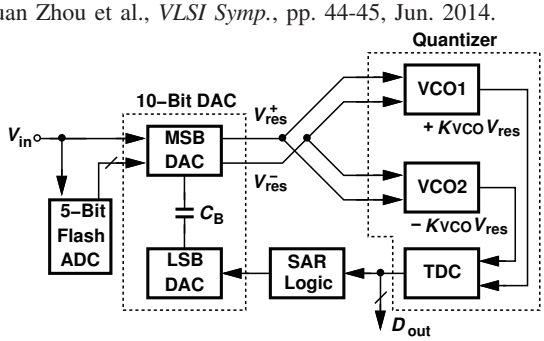

Fig. 1. ADC architecture.

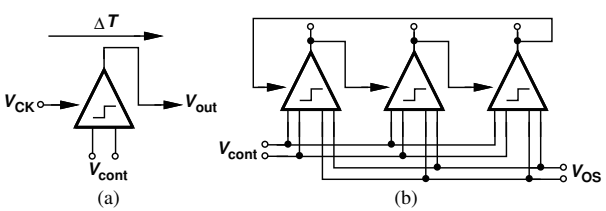

Fig. 2. (a) Comparator operating as variable-delay element, and (b) comparator-based ring oscillator.

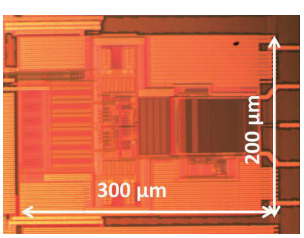

Fig. 3. Die photograph.

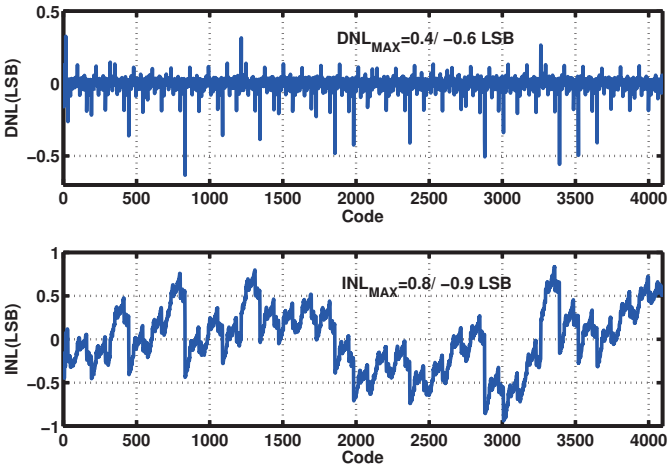

Fig. 4. Measured DNL and INL of the ADC.

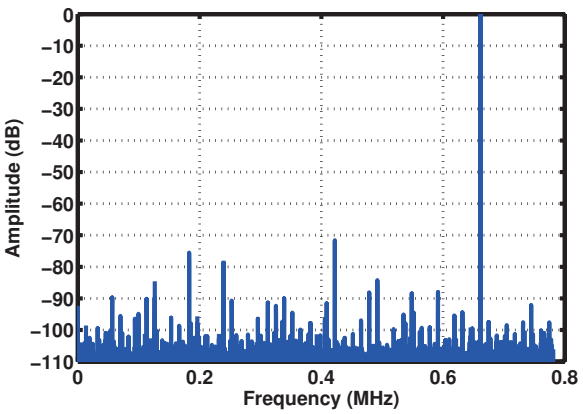

Fig. 5. Measured spectrum at $f_{in} = 121$ MHz (128x downsampled).

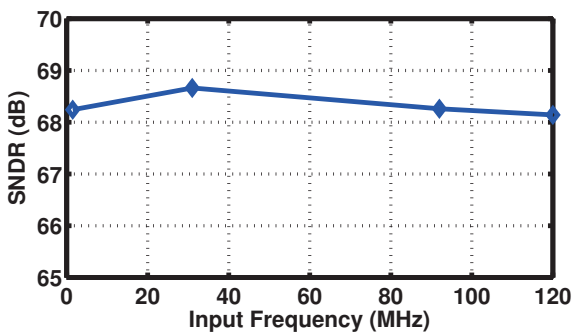

Fig. 6. Measured SNDR vs. input frequency.

TABLE I. Performance summary and comparison to prior art

	[5]	[6]	This Work
Technology (nm)	28	40	45
Area (mm^2)	0.35	.059	0.08
Supply Voltage (V)	0.9	1.2	0.85
Resolution	14	12	12
Sampling Rate (MS/s)	200	160	200
Power (mW)	2.3	4.96	3.4
INL (LSB)	± 2	–	± 0.9
DNL (LSB)	± 2	–	± 0.6
SNDR at Nyquist (dB)	60	60	68
FOM (fJ/conv. step)	12.8	20	8