25.7 A 2.4GHz 4mW Inductorless RF Synthesizer

Long Kong, Behzad Razavi

University of California, Los Angeles, CA

Recent developments in RF receiver design have eliminated all on-chip inductors except for that used in the local oscillator. This paper addresses this "last inductor" problem and proposes an integer-N synthesizer architecture that achieves a phase noise and a figure of merit (FOM) comparable to those of LC-VCO-based realizations.

The use of ring oscillators instead of LC implementations offers numerous advantages: smaller area, much less coupling to and from other circuits, a much wider tuning range, straightforward generation of multiple phases, and the ability to multiplex several small rings so as to cover multiple bands with minimal area penalty. However, the far inferior FOM of rings has discouraged their use in RF synthesis. The loop bandwidth of traditional type-II PLLs is bounded by "Gardner's limit" to $f_{REF}/10$, and typically less than $f_{REF}/20$ to suppress the reference spurs, thus failing to reduce the ring phase noise sufficiently.

The PLL architecture introduced here avoids Gardner's limit, achieving a loop bandwidth of approximately $f_{REF}/2$, and hence substantial reduction of the VCO phase noise. Shown in Fig. 25.7.1, the type-I synthesizer incorporates an XOR gate as a phase detector (PD), a master-slave sampling filter (MSSF), a programmable harmonic trap, a three-stage ring VCO, and a pulse-swallow feedback divider. The divider employs a new topology to allow a wide divide ratio, from 7 to 220, and hence operation with five octaves of VCO frequency range.

While the XOR PD is reminiscent of early type-I PLLs, it is the MSSF that accords this architecture two new properties. First, this filter transfer function exhibits notches at harmonics of the sampling frequency (= f_{REF} in the locked condition), considerably attenuating the large disturbance produced by the XOR. This property vanishes in traditional type-I PLLs due to their use of a continuous-time filter after the XOR. Second, the MSSF is clocked by the feedback signal, thereby providing a bandwidth roughly equal to $(C_1/C_2)(f_{VCO}/N)/(2\pi)$. Since the filter bandwidth scales with the VCO frequency, the synthesizer achieves a wide capture range (which is ultimately limited by the VCO). Absent in traditional type-I PLLs, this property obviates the need for a frequency detection loop.

The above properties distinguish the MSSF from the sampling loop filters used in [1] and [2], which employ a single sampler and are driven by PFD pulses rather than by the feedback signal. Another important attribute of the proposed synthesizer is that it eliminates the charge pump and its low-voltage design difficulties. While the ratio of C_1 and C_2 determines the loop bandwidth, the value of C_2 also plays a role in the performance; C_2 (= 2pF) is chosen so that $(kT/C_2)/f_{REF}$ contributes negligibly to the in-band phase noise as it is multiplied by N^2/K_{PD}^2.

In the presence of a ground bond-wire inductance in series with C_1, the transient current delivered by the XOR creates additional ripple on both C_1 and C_2, an error that is not removed by the nominal notch of the MSSF. To address this issue, the synthesizer employs a "harmonic trap", i.e., an impedance that approximates a short circuit at f_{REF} and $2f_{REF}$. The trap resonance frequencies are digitally tuned; a Δ-modulator monitors the ripple on the VCO control line and its output is full-wave rectified in the digital domain before adjusting the trap coefficients so as to minimize the ripple amplitude. The harmonic trap must exhibit a relatively sharp resonance so that it contributes both negligible phase shift and negligible noise at frequencies below $f_{REF}/2$.

Figure 25.7.2 shows the ring oscillator implementation. According to extensive simulations of various tuning mechanisms, varactor tuning poses the least phase-noise penalty, a point evidently not previously recognized. The transistor dimensions (W/L = 36µm/0.28µm for both NMOS and PMOS devices) are chosen so as to reduce their flicker noise to the point where the phase-locked phase noise beyond a few hundred kilohertz offset is dominated by white noise. The free-running 2.4GHz VCO produces a phase noise of -121dBc/Hz at 10MHz offset while consuming 3.1mW power.

The proposed architecture utilizes a Δ-modulator as a fast, low-power, and compact digitizer with an oversampling ratio of 30. Shown in Fig. 25.7.2, the modulator consists of a StrongArm comparator controlling a 1b DAC that returns a swing of $\pm\Delta V$ around the input CM level, V_{CM}. In contrast to conventional Δ-modulators, which return the entire output digital swing, this implementation saves considerable area for C_D, for a given sensitivity. With ΔV = 25mV, C_D is shrunk by a factor of 1V/50mV = 20. The Δ-modulator consumes 150uW.

The harmonic trap consists of two individual series-resonance branches at f_{REF} and $2f_{REF}$. Figure 25.7.3 depicts the implementation of one branch. Here, G_{m1} and G_{m2} form a gyrator, rotating C_L to create at X an equivalent inductance of $C_L/(G_{m1}G_{m2})$ = 70.8uH, which resonates with C_S at f_{REF}. The resonance frequency is adjusted by a digitally controlled G_{m2}. With a Q of 15, this circuit requires sufficiently fine tuning steps, hence the need for a coarse control (the tail currents) and a fine control (the degeneration resistance).

The integer-N synthesizer has been fabricated in TSMC 45nm digital CMOS technology. Shown in Fig. 25.7.7 is the die micrograph, whose active area measures 100um × 150um. The prototype has been tested with a 1V supply and operates from 2GHz to 3GHz, consuming 4mW at 2.4GHz. Plotted in Fig. 25.7.4, the measured phase noise reaches -114dBc/Hz within the loop bandwidth; Figure 25.7.5 shows the measured output spectrum with the harmonic traps turned off and on. The 1st-order spur falls from -47dBc to -65dBc, and the 2nd-order spur from -55dBc to -68.5dBc. Integrated from 1kHz to 200MHz, the integrated jitter is equal to $0.97ps_{rms}$. These results far exceed the specifications of wireless standards at 2.4GHz.

Figure 25.7.6 summarizes the performance of recently-reported synthesizers in the frequency range of 2.3GHz to 3.1GHz. We note that the proposed design achieves, with a lower power, 16-to-20dB lower phase noise than do ring-based topologies. If adjusted for the 2X difference in reference frequencies, our design also has a comparable phase noise to that of the LC-VCO-based PLL in [5] but at one-fourth of the power.

Acknowledgements:
This research was supported by the Qualcomm Innovation Fellowship Program and Realtek Semiconductor. The authors are grateful to the TSMC University Shuttle Program for chip fabrication.

References:
[1] S. E. Meninger et al., "A 1-MHz Bandwidth 3.6GHz 0.18-um CMOS Fractional-N Synthesizer Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise.," *IEEE J. Solid-State Circuits*, vol. 41, pp. 966-980, April 2006.
[2] K. J. Wang et al., "Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional-N PLL," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2787-2797, Dec. 2008.
[3] A. Sai et al., "A Digitally Stabilized Type-III PLL Using Ring VCO with $1.01ps_{rms}$ Integrated Jitter in 65nm CMOS", *ISSCC Dig. Tech. Papers*, pp. 248-249, Feb. 2012.
[4] Y. C. Huang et al., "A 2.4GHz ADPLL with Digital-Regulated Supply-Noise-Insensitive and Temperature-Self-Compensated Ring DCO," *ISSCC Dig. Tech. Papers*, pp. 270-271, Feb. 2014
[5] P. C. Huang et al., "A 2.3GHz Fractional-N Dividerless Phase-Locked-Loop with -112dBc/Hz In-Band Phase Noise," *ISSCC Dig. Tech. Papers*, pp. 362-363, Feb. 2014.

 978-1-4799-6224-2/15/$31.00

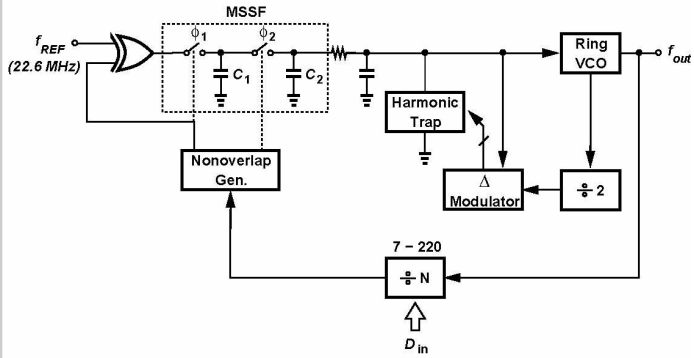

Figure 25.7.1: Proposed type-I synthesizer architecture.

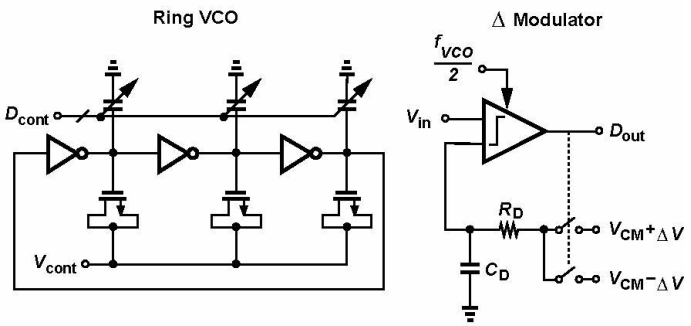

Figure 25.7.2: Ring oscillator and Δ-modulator implementations.

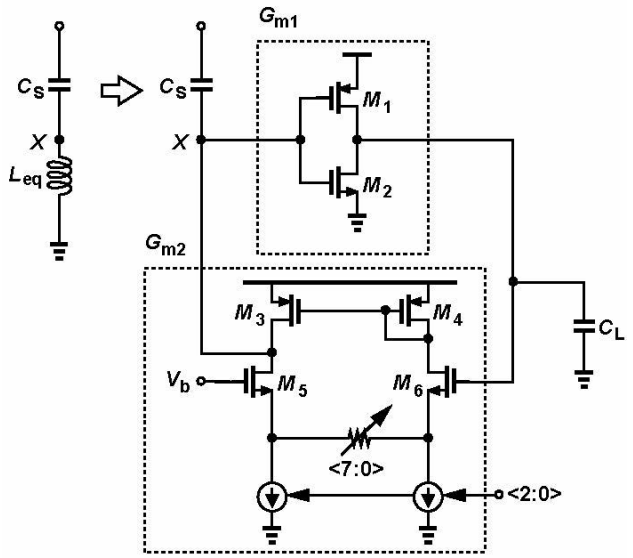

Figure 25.7.3: Implementation of one branch of the harmonic trap.

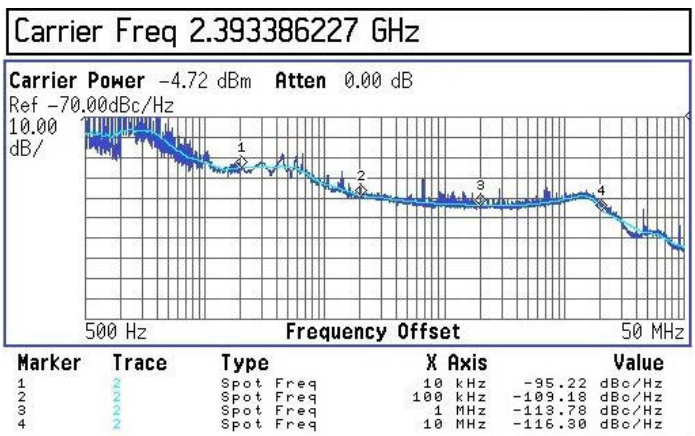

Figure 25.7.4: Measured phase noise.

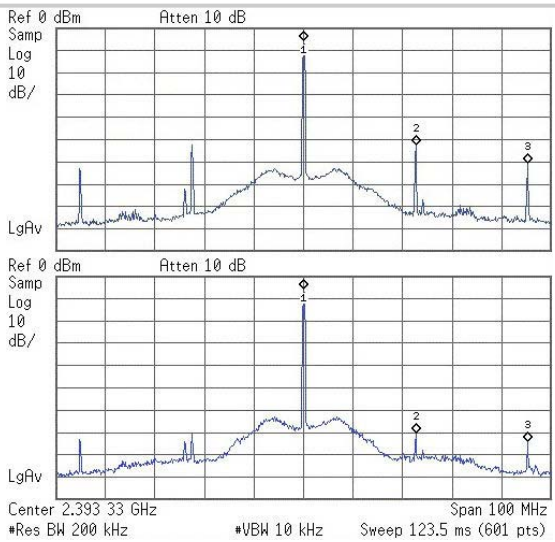

Figure 25.7.5: Measured output spectrum with harmonic traps turned off (top) and turned on (bottom).

	ISSCC'12 [3]	ISSCC'14 [4]	ISSCC'14 [5]	This Work
Oscillator Topology	Ring	Ring	LC	Ring
Reference Freq. (MHz)	36	26	48	22.6
Frequency Range (GHz)	1.4 ~ 3.2	2.42	2.2 ~ 2.4	2.0 ~ 3.0
Phase Noise @ 1MHz offset (dBc/Hz)	−98	−94	−117	−113.8
RMS Jitter (ps) Integ. range (MHz)	2.23 (N/A)	3.29 (0.01~40)	0.3 (0.01~30)	0.97 (0.001~200)
Ref. Spur (dBc)	N/A	−75	−55	−65
Power (mW)	25.8	6.4	17.3	4
Area (mm^2)	0.32	0.013	0.75	0.015
Tech. (nm)	65	40	180	45
FOM_1 (dB)	−218.9	−221.6	−238	−234.1
FOM_2 (dB)	153.7	153.6	171.9	175.4

$FOM_1 = 10\log_{10}[(\frac{Jitter}{1\ s})^2(\frac{Power}{1\ mW})]$ $FOM_2 = 10\log_{10}[(\frac{f_{osc}}{\Delta f})^2(\frac{1\ mW}{Power})] - Phase\ Noise\ (dBc/Hz)$

Figure 25.7.6: Performance summary and comparison with state-of-the-art.

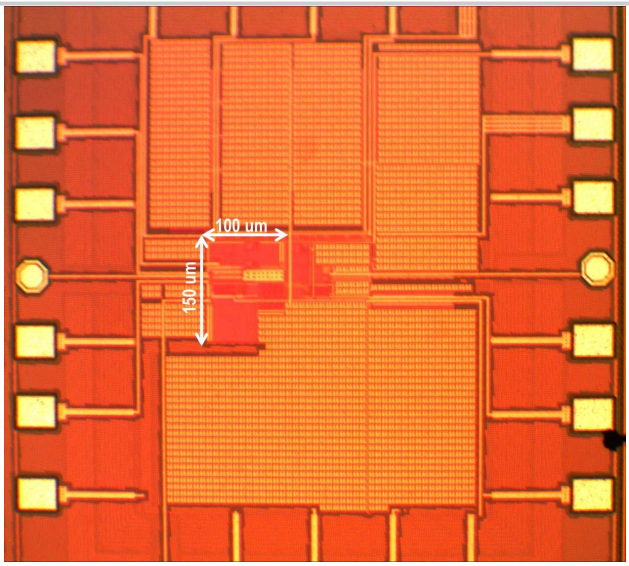

Figure 25.7.7: Die micrograph.

978-1-4799-6224-2/15/$31.00