A 6-bit 10-GS/s 17.6-mW CMOS ADC with 0.8-V supply

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SAR ADCs offer favorable resolution-power trade-offs but face severe limitations at high speeds. Asynchronous operation [1] has mitigated this issue to some extent. Also, techniques such as detecting more than 1 bit per cycle [2], or preceding the SAR loop with a flash stage [3]. In the gigahertz range, however, we face two challenges. (1) The overhead time associated with some of these methods becomes a substantial part of the clock cycle, limiting the conversion rate. (2) The overhead power associated with time interleaving proves serious.

This paper proposes a "look-ahead" SAR architecture that raises the speed by about a factor of 2 with minimal power penalty. In addition, a new approach to clock distribution for interleaving is presented that greatly reduces phase mismatches.

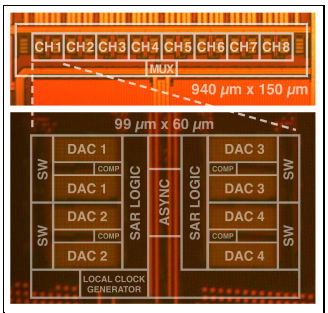
The timing budget for an asynchronous SAR consists of four components: comparator decision, asynchronous clock generation, SAR logic delay, and DAC settling. For resolutions around 6 bits, these quantities are comparable, except for one hard decision when the comparator's input difference is less than 1 LSB. To improve the speed, we break up this serial dependence by viewing the SAR binary search as follows: for a reference, V_{REF}, the DAC generates residues of the form $V_{in}-V_{REF}/2$, $V_{in}-3V_{REF}/4$ or $V_{in}-V_{REF}/4$, etc., in successive cycles and the comparator finds their polarities. In a given cycle, the *future* residues can also be precomputed. For example, while generating $V_{in}-V_{REF}/2$, our look-ahead architecture determines $V_{in}-3V_{REF}/4$ and $V_{in}-V_{REF}/4$ as well. Illustrated conceptually in Fig 1, the idea is to employ three DACs to produce these residues concurrently, and then utilize the decision made by $Comp_1$ to select $V_{in}-3V_{REF}/4$ or $V_{in}-V_{REF}/4$ for the next comparison. Neglecting the MUX delay for now, we note that the logic delay and DAC settling occur during comparator operation and asynchronous clock generation; the speed therefore doubles.

The basic architecture of Fig. 1 entails two issues. First, the MUX causes charge sharing between the DAC and node X, introducing memory effects and distortion. Second, the logic necessary for keeping track of residue generation and comparison becomes rather complex. The MUX can be simply omitted if DAC_2 and DAC_3 drive their own comparators, and the logic is greatly simplified if one more DAC is added. We thus obtain the complete architecture shown in Fig. 1, where four DAC/comparator slices participate in the conversion. The comparator outputs travel through selectors to clock the other comparators. We call this network the "digital loop". In addition, the comparator output drives the standard SAR logic block, which activates the DACs. We call this network the "analog loop". Each comparator includes a StrongArm latch and an RS latch.

To illustrate the operation, we turn to the snapshots of the architecture shown in Fig. 2. After the input signal is sampled on all four DACs, DAC_1 generates $V_{in}-V_{REF}/2$, CK_1 is activated, and the top comparator produces the MSB. At the same time, DAC_3 and DAC_4 respectively deliver $V_{in}-3V_{REF}/4$ and $V_{in}-V_{REF}/4$ while DAC_2 remains idle. As depicted in Cycle 2, if MSB=1, then the top clock selector routes this high level to CK_3 so that the sign of the residue $V_{in}-3V_{REF}/4$ is detected. Conversely, if MSB=0, then CK_4 is activated so as to find the sign of $V_{in}-V_{REF}/4$. The second bit, MSB_{-1}, is thus obtained from one of the two bottom comparators. In the meantime, DAC_1 or DAC_2 generates the next residue if MSB_{-1}=1 or MSB_{-1}=0, respectively. Also, the clock selector activates the corresponding clock (CK_1 if MSB_{-1}=1, or CK_2 if MSB_{-1}=0), initiating a new look-ahead cycle. This alternation continues until all 6 bits are obtained.

The proposed SAR architecture merits three remarks. First, except for the simple clock selectors, no logic is necessary to keep track of which DAC must be active during the look-ahead operation.The digital loop therefore incurs only the delay of one comparator and one clock selector.

Second, in contrast to prior 2-bit/cycle loops, which do not fully benefit from asynchronous operation [4], look-ahead prediction is naturally asynchronous and contains only one hard decision per conversion. Third, the need for four 6-bit DACs requires that their capacitance and footprint be minimized. This work employs a 1 µm x 1 µm unit having a value of 0.42 fF, with the bottom-plate switches placed underneath. Each DAC presents 32.3 fF, yielding a total of 4x32.3 fF ≈ 130 fF seen by the main input. The four differential DACs occupy about 27% of each interleaved channel.



Die micrograph.

The clock selectors in Fig. 3 must begin from reset, deliver proper clocks, and return to reset after each comparator decision is completed and a "ready" signal is generated for asynchronous clocking. This is accomplished by the compact implementation shown in Fig. 3, where CK_{ch} denotes the main clock. This circuit introduces a delay of only 25 ps.

The digital and analog loops in Fig. 1 exhibit their own delays, which should be approximately equal so that the two loops "converge" at about the same time. Nevertheless, the maximum analog loop delay must remain less than the minimum digital loop delay to ensure correct DAC settling. As shown in Fig. 3, this condition is guaranteed by bypassing the pointer register in the SAR logic, an improvement afforded by look-ahead action and not possible in conventional SAR converters.

The single SAR ADC channel described above can be designed, in 28-nm technology, with a linear speed-power trade-off up to a clock rate of about 1.25 GHz. Beyond this point, we resort to interleaving. The overall 10-GS/s ADC incorporates eight channels driven by nonoverlapping clocks, CK_{ch1}-CH_{ch8}, with a 12.5% duty cycle (DC) (Fig. 4), presenting the input capacitance of a single channel.

The need for a 12.5% DC poses daunting challenges in the distribution of clock phases across the channels. A pulse having a width of 100 ps deteriorates as it travels along a 1-mm interconnect. Moreover, distribution of phases introduces large deterministic and random mismatches. To resolve these, we propose a "local" phase generation concept. As depicted in Fig. 4, only a 5-GHz clock with 50% DC is distributed across the array and the phase necessary for each channel is generated by a local ring counter. The distribution is thus greatly simplified. The counter delivers outputs X_1, X_2, etc., with a 25% DC and the NAND gates shown at the bottom convert the DC to 12.5%.

The use of eight ring counters - rather than one – may appear to cause area and power penalties. In practice, however, the idea proves advantageous: the local ring counters in this work occupy a total area of 0.0012 mm^2 and draw 2 mW, which are *lesser* quantities than those necessary for distributing and buffering eight phases across the chip. For proper interleaving, the counters must begin from a known state at power-up. This is ensured by an external synchronization command, S_{ext}, that drives a cascade of a global flipflop, FF_G, and a local one, FF_L.

The proposed ADC has been fabricated in 28-nm CMOS technology. The channels' outputs are downsampled by a factor of 625.

Unless otherwise stated, all measurements are carried out at a sampling rate of 10 GS/s. Plotted in Fig. 5 are the DNL and INL. Also shown is the spectrum in response to a 4.96-GHz full-scale input (0.6 $V_{pp,SE}$), yielding an SNDR of 31.2 dB and a SFDR of 44.5 dB. The figure of merit is 59 fJ/cs at Nyquist. The bottom left plots show the SNDR and SFDR vs. the input frequency.

It is possible to operate the ADC up to 16 GS/s by raising the supply voltage to 0.85 V. The bottom right plots in Fig. 5 display the SNDR and power consumption for different supply voltages. The look-ahead architecture can therefore reach a sampling rate of 2 GS/s per channel. Fig. 6 compares the converter's performance.

References:

[1] Shuo-Wei Mike Chen and W. Brodersen, ISSCC, Feb. 2006.
[2] Zhiheng Cao *et al*., ISSCC, Feb. 2008.
[3] Ba Ro Saim Sung *et al.,* ISCAS, May. 2009.
[4] Chi-Hang Chan *et al*., JSSC, March. 2018.

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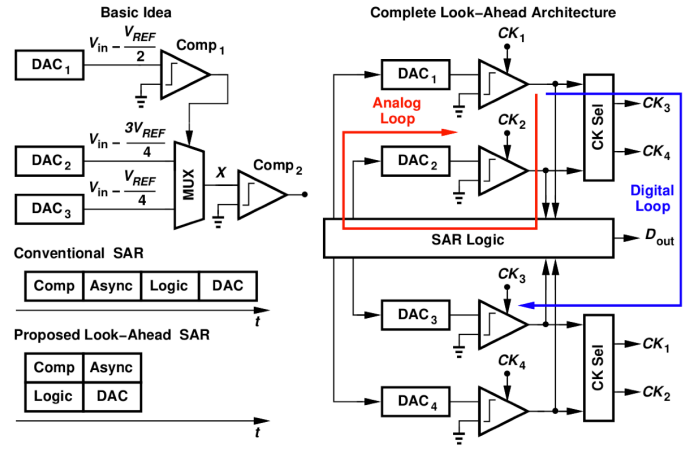

Fig. 1. Conceptual ADC architecture.

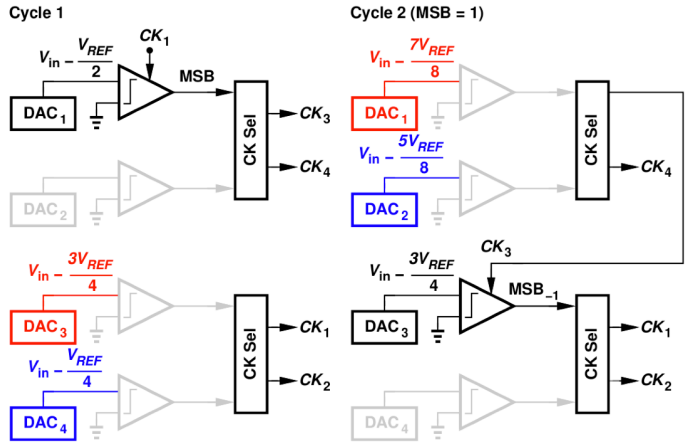

Fig. 2. Proposed look-ahead SAR operation.

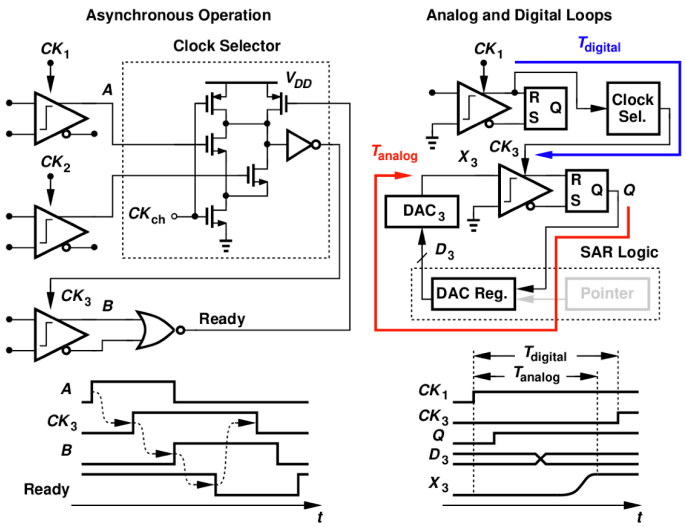

Fig. 3. Clock selection and look-ahead loops.

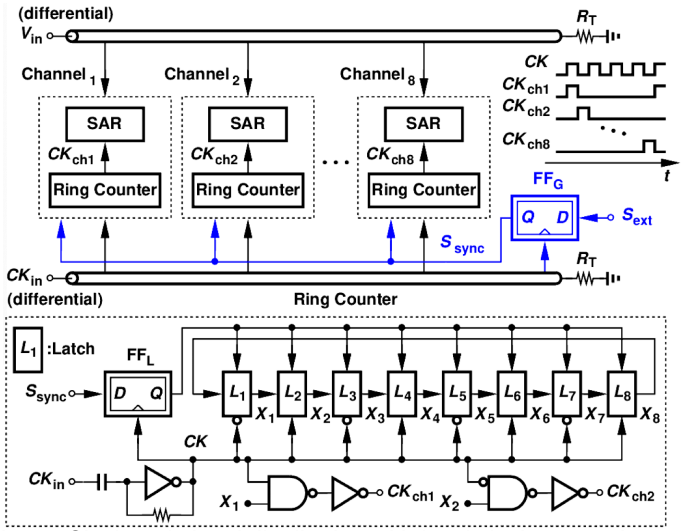

Fig. 4. Clock and signal distribution with local clock generation.

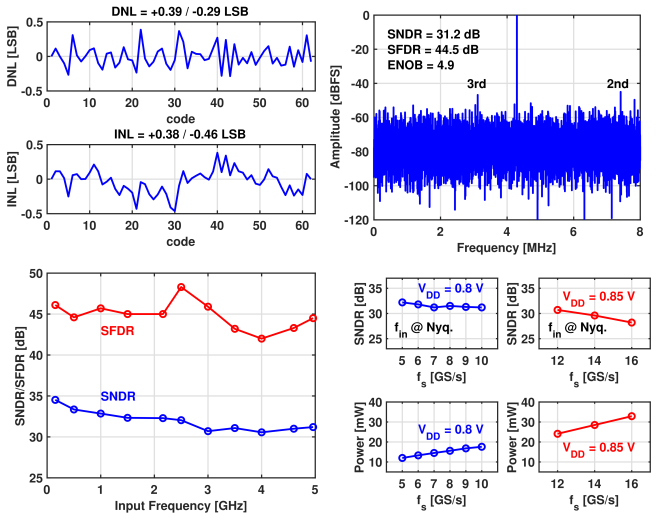

Fig. 5. Measured performance at 10 GS/s and beyond.

Reference	Le Tual ISSCC'14	Shafik ISSCC'15	Raghavan VLSI'16	Hassan–Purghadi CICC'19	This Work
Topology	TI–SAR	TI–SAR	TI–Flash	TI–TDC	TI–SAR
Resolution (bits)	6	6	6	7.3	6
Number of channels	8	32	2	2	8
SNDR @ Nyquist (dB)	33.8	30.3	29.4	32.5	31.2
Sampling rate (GS/s)	10.0	10.0	10.3	10.0	10.0
Power (mW)	32.0	79.0	95.0	29.7	17.6
FOM @ Nyquist (fJ/cs)	81	296	382	86	59
Technology (nm)	28*	65	28	65	28
Supply (V)	1	1	0.9	1	0.8
Area (mm^2)	0.009	0.81	—	0.015	0.14

* 28–nm UTBB FDSOI technology with Forward Body Biasing (FBB)

$$FOM = \frac{Power}{2^{ENOB} f_s} \qquad ENOB = \frac{SNDR - 1.76}{6.02}$$

Fig. 6. Peformance Summary and comparison with state of the art.