WP 2.4: A 12b 5MS/s Two-Step CMOS A/D Converter*

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The potential of two-step flash architectures for realizing fast high-resolution analog-to-digital converters (ADCs) has been demonstrated in a number of designs [1, 2]. This 12b 5MHz fully-differential two-step ADC is integrated in a 1μm CMOS technology, employs both analog and digital correction, and dissipates 200mW.

The ADC architecture and timing diagram are shown in Figure 1. The converter consists of a 7b coarse flash stage, a 7b digital-to-analog converter (DAC), a subtractor, and a 6b fine flash stage. One-of-n decoders and ROMs are used to convert the thermometer code outputs of the two flash stages to binary data, that is then corrected digitally to produce the final output. One bit of redundancy, or overlap, is utilized in this architecture to enable the second stage to correct for errors made in the first stage, thereby relaxing the performance required of the first-stage comparators. With the present design, an external sample-and-hold must be used in order to digitize high-frequency analog inputs.

Controlled by two clocks Φ1 and Φ2, the system of Figure 1 operates as follows. In the sampling/calibration mode, Φ1 and Φ2 are high, an external sample-and-hold samples the analog input, the comparators in the two flash stages are in the offset-cancellation mode, and the DAC and the subtractor are reset. When Φ1 goes low, the first-stage comparators are strobed to produce a digital estimate of the analog input, and the second-stage comparators begin to track the subtractor output. After the first stage, the DAC, and the subtractor have responded, Φ2 goes low to strobe the second-stage comparators and perform the fine conversion. This timing arrangement cancels offsets in every cycle, and thus eliminates flicker noise at the input of the comparators.

A simplified, single-ended functional diagram of the converter is shown in Figure 2. The first stage comprises 128 comparators and encodes the 7 most-significant bits. Although offsets as large as 30mV are permitted in the first-stage comparators, they nonetheless employ a simple offset cancellation to ensure reliable operation with small-geometry devices. With response time of 10ns and dissipation of 0.5mW, these comparators exhibit an input offset of 5mV and an input capacitance of 100fF.

The thermometer code output of the first stage is directly applied to the DAC to generate the analog estimate. This is in contrast with approaches wherein the thermometer code is converted to a binary code and then used to drive a binary-weighted capacitor DAC [2, 3]. The DAC used in this design consists of an array of equal capacitors with a common top plate and MOS switches connected to the bottom plate of each capacitor. Controlled by the first-stage comparators, the MOS devices switch the bottom plates between GND and the reference voltage. The DAC can be viewed as a capacitive voltage divider that causes the top plate voltage to change by an amount proportional to the number of ONEs in the thermometer code. The settling time of the DAC is determined by the unit capacitor value and the size of the switches driving the bottom plates and can be kept below 10ns by tapering the sizes of the transistors in the first-stage comparators and the DAC.

The design of Figure 2 employs a gain of 1 in the subtractor to achieve maximum speed. This approach places the 12b resolution requirement on the comparators in the second stage. The subtractor output drives the second, or fine flash stage, which is comprised of 64 comparators and two reference ladders.

As the comparators in the second stage must resolve 1LSB differences, they incorporate offset cancellation in both preamplifiers and latches. As illustrated in Figure 3, these comparators employ two transconductance amplifiers, G_{m1} and G_{m2}, that share their output nodes. Buffers B1 and B2 together with capacitors C1 and C2 can establish a positive feedback loop around G_{m2}. During offset cancellation, the inputs of G_{m1} and G_{m2} are grounded and the offsets of G_{m1}, G_{m2}, B1, and B2 are stored on C1 and C2. During comparison, first V_{in} is sensed and amplified by G_{m1}, and then S9 and S10 are closed to initiate regeneration in G_{m2}. The calibration technique of Figure 3 allows the second-stage comparators to achieve a response time of 15ns with an offset of 300μV and a dissipation of 1.8mW.

To establish reference voltages ranging from 1LSB to 64LSB for the second-stage comparators, the full-scale reference is divided into 64 equal segments by a primary ladder, and a secondary ladder subdivides one of these segments by another factor of 64. The loading of the secondary ladder on the primary one introduces an error of approximately 1LSB, that is canceled by replicating and injecting the current I1 at the junction of the ladders, node X. The accuracy of this correction is not critical because, even if I1 deviates from its ideal value by 10%, loading error is still reduced by a factor of 10, i.e., to 0.1LSB.

The ADC is fabricated in a 1μm CMOS process with poly-to-diffusion capacitors [4]. Figure 4 plots the measured differential nonlinearity (DNL) of a prototype for a 5kHz sinusoidal input at a sampling rate of 5MHz. Since the DNL remains below 0.7LSB, the ADC has no missing codes and exhibits 12b resolution. Figure 5 shows measured signal-to-noise+distortion ratio (SNDR) as a function of input level for the same input and clock frequencies, indicating a peak SNDR of 65dB. Table 1 summarizes the measured performance of the prototype and Figure 6 shows a die micrograph.

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References

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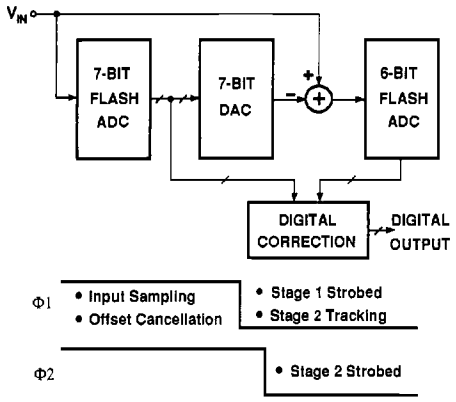

Figure 1: ADC architecture and timing

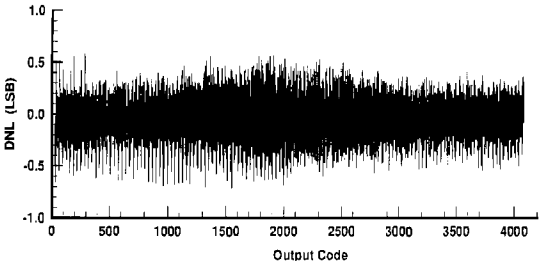

Figure 4: Measured differential nonlinearity.

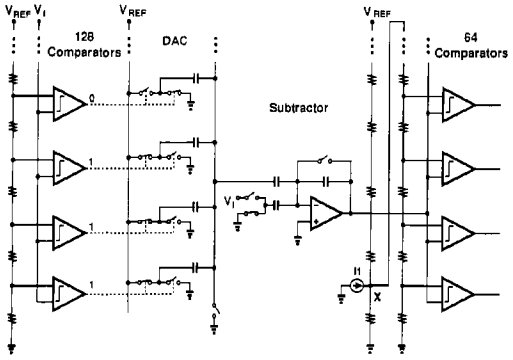

Figure 2: ADC single-ended functional diagram.

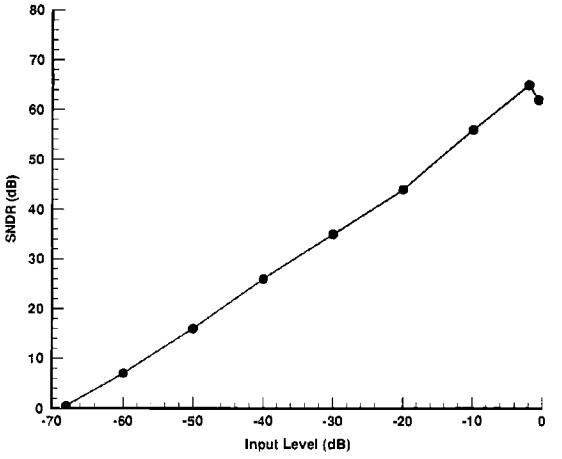

Figure 5: Measured signal-to-(noise+distortion) ratio.

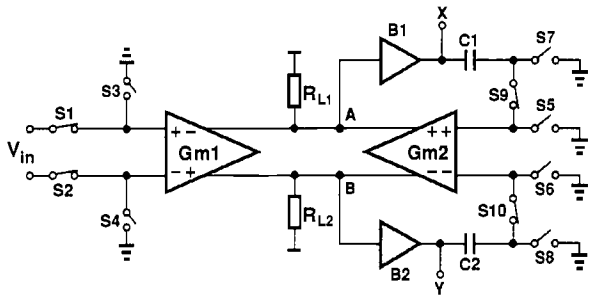

Figure 3: Second-stage comparator.

Resolution	12b
Conversion Rate	5MHz
Input Range	5V
Power	200mW
Power Supply	5V
Input Capacitance	15pF
Area	3.7x2.5mm^2
Technology	1μm CMOS

Table 1: ADC performance.

Figure 6: See page 236.

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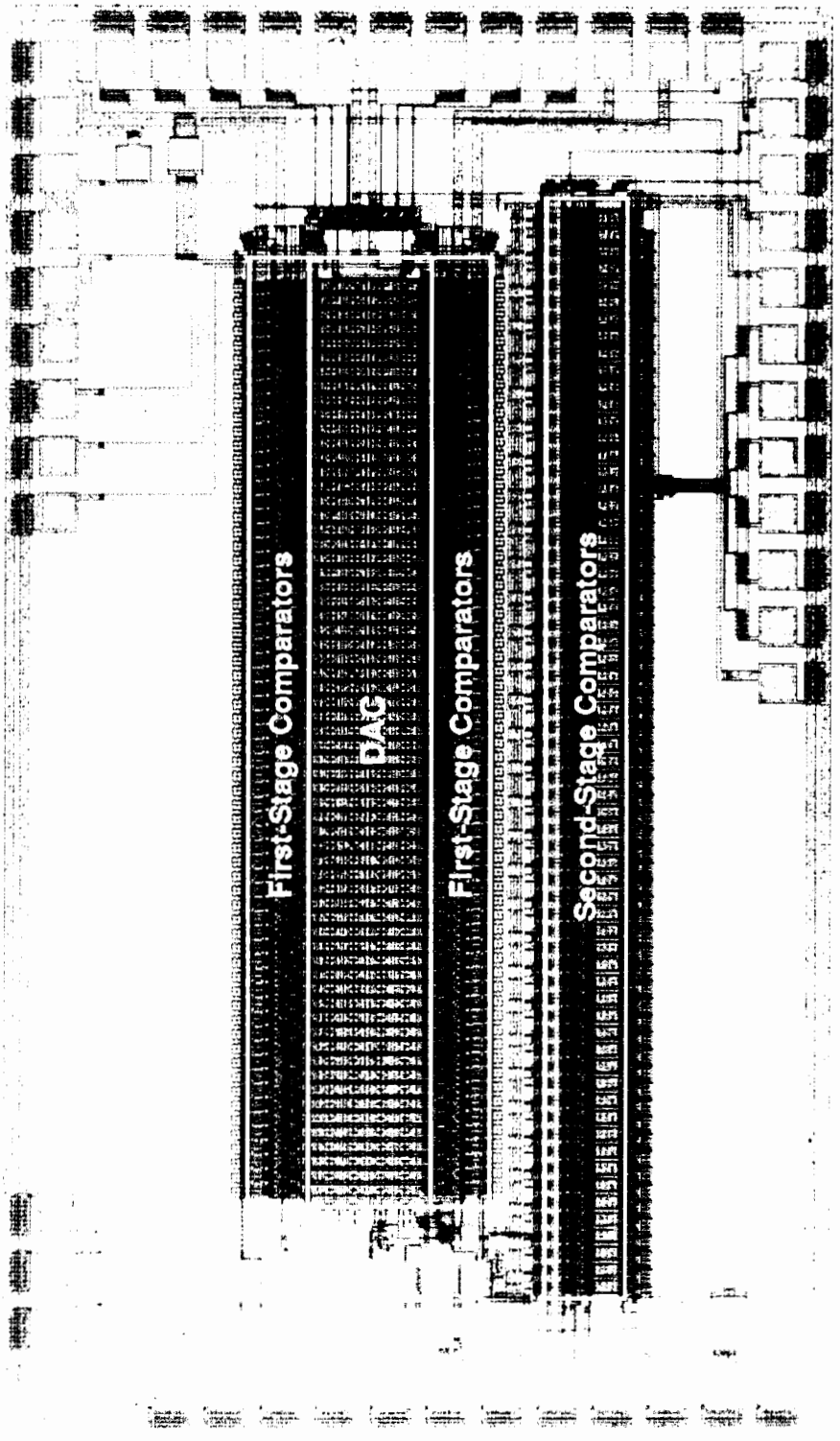

Figure 6: ADC die micrograph.